LP6274AQVF

14 Channel Level Shifter for GOP TFT-LCD Panel

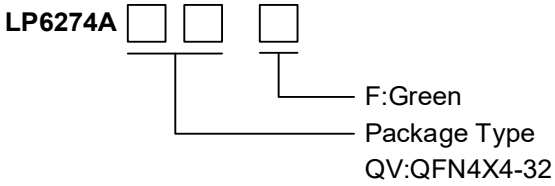
Features

- Input Supply Range: 2.5V ~ 5.5V
- 14-Channel Level Shifter
  - +40V Highest Voltage Level
  - -20V Lowest Negative Voltage level
  - Maximum 700ns Rising/Falling Time
- Level Shifter input logic
  - 2 STO input/output
  - Suitable for 4/6/8 Phase Applications
  - Support 1 clock input
  - 1 clock input 1/2 line turn on function
  - 1 clock input 0/1/2/3line pre-charge
- Protection Function
  - Input under voltage lockout (UVLO)
  - Thermal overload protection (OTP)
  - Over Current Protection (OCP)
  - CKI input stop protection (CISP)
  - Short Circuit Protection (SCP)
- XON Function
- RoHS Compliant and 100% Lead (Pb)-Free
- Compact Package: QFN4X4-32

Applications

- GOA TFT-LCD PANEL

Order Information



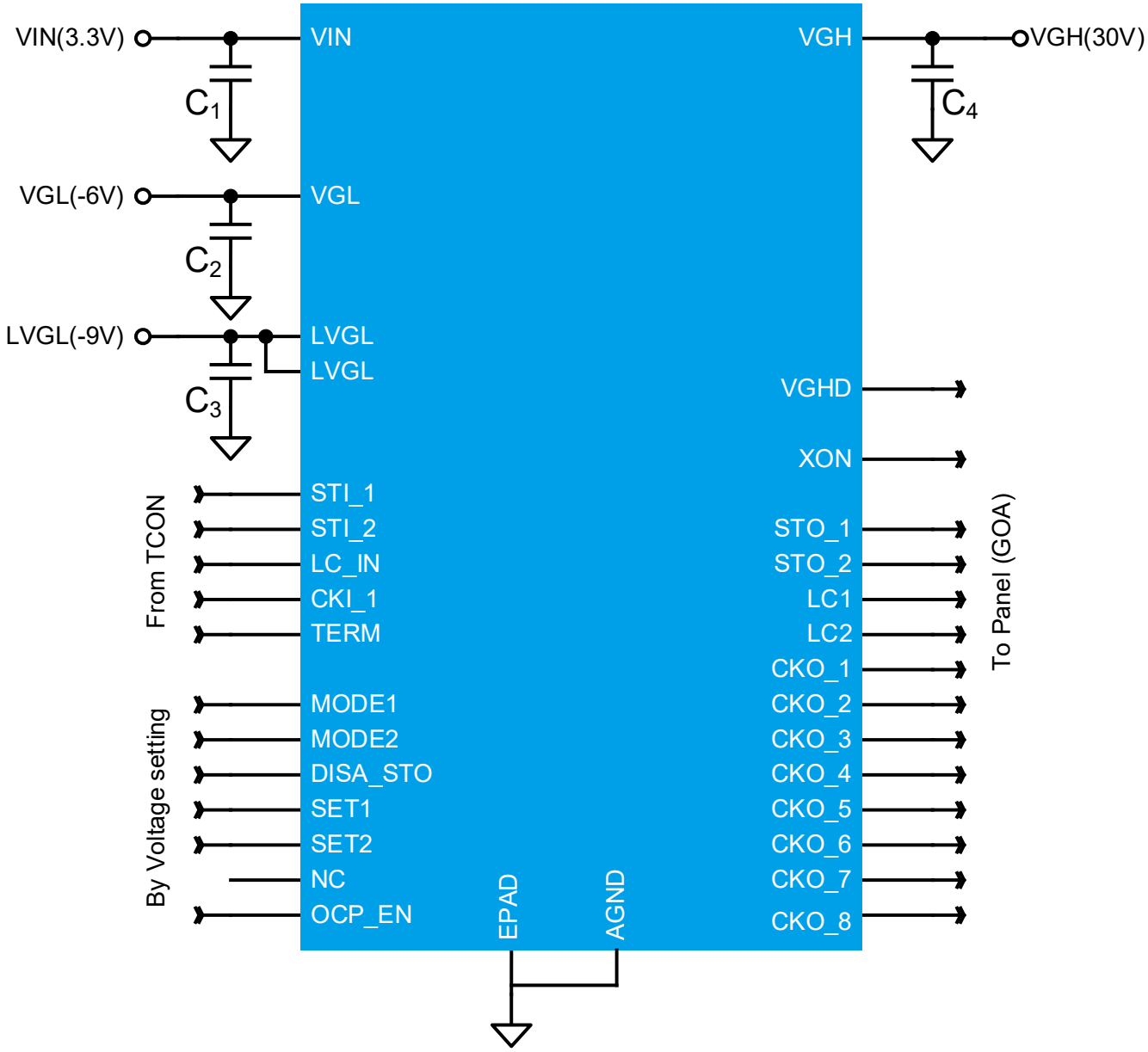
General Description

The LP6274A includes 12-channel high-voltage level shifter with adjustable gate pattern functions. This device is suitable for GOA TFT-LCD panel application.

The LP6274A transform the logic-level controlled signals, which are generated by the display timing controller (TCON), into the high-level signals needed by LCD panel. Different CKO_1~8 output patterns will be generated by different external settings. Each channel of level shifter output uses low impedance transistors to achieve fast rising and falling time, even when driving the capacitive loads present in LCD applications.

The LP6274A features extensive protection functions that include UVLO, TOP, SCP and OCP. The device operates over the -40°C to +85°C. It is available in 4mmx4mm, 32-lead QFN package.

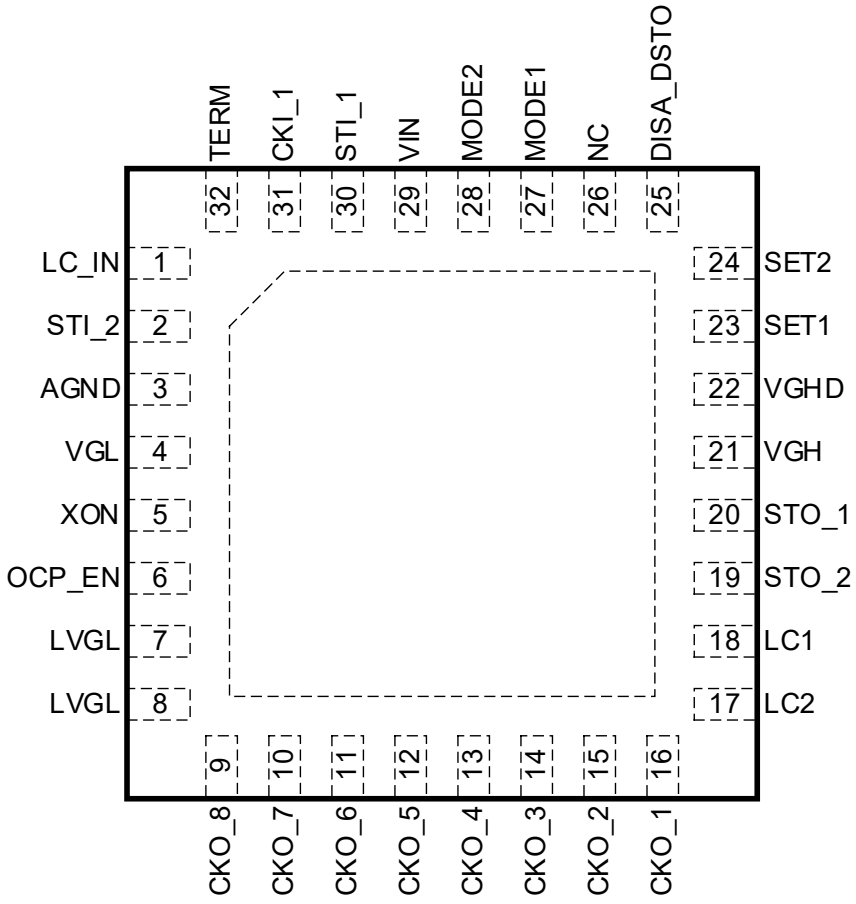
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6274AQVF	LPS LP6274A YWXXX	MSL3	QFN4X4-32	3K/REEL
Marking indication: Y: Year code. W: Week code. XXX: Batch numbers.				

Pin Diagram



LPQ6274AQVF QFN4X4-32

Pin Description

Pin#	Name	I/O	Description
1	LC_IN	I	Level Shifter Input Signal(Low frequency clock) The LC is the high / low level trigger. This pin is internally connected to a 400kΩ resistance to the GND.
2	STI_2	I	Level Shifter Input Signal. This pin is internally connected to a 400kΩ resistance to the GND.
3	AGND	--	Analog Ground for Logic Block.
4	VGL	P	XON pin negative power supply.
5	XON	O	Discharge function for Liquid Crystal capacitor when panel power off.
6	OCP_EN	I	Setting pin for disable OCP function High level(2.5V~3.6V) : Disable OCP function Floating level(1.2V~2.2V) : OCP Level2 function --- 60mA Low level(0V~0.8V) : OCP Level1 function --- 100mA This pin internal connection respectively 400kΩ resistance to VIN and GND
7	LVGL	P	Negative power supply. Please reference to function block and application circuit.
8	LVGL	P	Negative power supply. Please reference to function block and application circuit.
9	CKO_8	O	Level Shifter Output Signal.
10	CKO_7	O	Level Shifter Output Signal.
11	CKO_6	O	Level Shifter Output Signal.
12	CKO_5	O	Level Shifter Output Signal.
13	CKO_4	O	Level Shifter Output Signal.
14	CKO_3	O	Level Shifter Output Signal.
15	CKO_2	O	Level Shifter Output Signal.
16	CKO_1	O	Level Shifter Output Signal.
17	LC2	O	Level Shifter Output Signal (Low Frequency Clock 2)
18	LC1	O	Level Shifter Output Signal (Low Frequency Clock 1)
19	STO_2	O	Level Shifter Output Signal.
20	STO_1	O	Level Shifter Output Signal.
21	VGH	P	LC1/LC2, STO_1/STO_2, CKO_1~CKO_8, XON, VGHD Positive Power Supply.
22	VGHD	O	VGH Output
23	SET1	I	Setting Pin for Phase Selection. High Level (2.5V~3.6V) : 8 phase Low Level (0V~0.8V) : 6 phase Floating (1.2V~2.2V) : 4 phase Then setting will trigger & latch the phase selection function by first STI_1 rising edge. It is suggested that the pin is fixed by VIN or GND or Floating. The mean of floating is without external voltage or signal. (Don't connect anything) This pin internal connection respectively 400kΩ resistance to VIN and GND

Pin Description

Pin#	Name	I/O	Description
24	SET2	I	Setting Pin for Clocks Interval. High Level (1.5V~3.6V) : There is some time interval between CKO_s Low Level (0V~0.8V) or Floating : There is no time interval between CKO_s The setting will trigger & latch the clocks interval function by each STI_1 rising edge. It is suggested that the pin is fixed by VIN or GND or Floating The mean of floating is without external voltage or signal. (Don't connect anything) This pin is internally connected to a 400kΩ resistance to the GND.
25	DISA_DSTO	I	Setting Pin for STO_2 output. High Level (1.5V~3.6V) : STO_1 ON (follow STI_1), STO_2 keeps in LVGL Low Level (0V~0.8V) : STO_1 ON (follow STI_1), STO_2 ON (follow STI_2) It is suggested that the pin is fixed by VIN or GND. This pin is internally connected to a 400kΩ resistance to the GND.
26	NC		No Connect.
27	MODE1	I	Setting Pin for Pre-charge selection. Extra High level (3V~4V) : 3-line pre-charge High level (1.5V~2.5V) : 1-line pre-charge Middle level (0.9V~1.4V) : no pre-charge Low level (0V~0.8V) : 2-line pre-charge The MODE1 will trigger & latch by each STI_1 rising edge. This pin is internally connected to a 400kΩ resistance to the GND.
28	MODE2	I	Setting Pin for 1 line mode or 2 line mode selection. High level (1.5V~3.6V) : 2 line mode on Low level (0V~0.8V) : Keep 1 line mode on The MODE2 will trigger & latch by each STI_1 rising edge. It is suggested that pin is fixed by VIN or GND. This pin is internally connected to a 400kΩ resistance to the GND.
29	VIN	P	Supply voltage input.
30	STI_1	I	Level Shifter Input Signal (start pulse for GOA). The corresponding Level Shifter output channel is STO_1. The STI_1 is rising / falling edge trigger. This pin is internally connected to a 400kΩ resistance to the GND.
31	CKI_1	I	Level Shifter Input Signal (Condensed clock) The CKI_1 is the rising / falling level trigger. This pin is internally connected to a 400kΩ resistance to the GND.
32	TERM	I	Level Shifter Input Signal. Pull CKO_1 to CKO_8 low in blanking time The Terminate is the high level trigger This pin is internally connected to a 400kΩ resistance to the GND.
33	E-PAD	P	The E-Pad should be connected to ground.

Absolute Maximum Ratings (Note1)

VIN to AGND ---------- -0.3V to +7V
LC_IN, STI_2 to AGND ---------- -0.3V to +7V
VGL to AGND ---------- -20V to +0.3V
XON to AGND ---------- VGL+0.3V to VGH-0.3V
LVGL to AGND ---------- -20V to +0.3V
CKO_1~CKO_8 to AGND ---------- LVGL+0.3V to VGH-0.3V
LC1, LC2 to AGND ---------- LVGL+0.3V to VGH-0.3V
STO_1, STO_2 to AGND ---------- LVGL+0.3V to VGH-0.3V
VGH to AGND ---------- -0.3V to +45V
VGHD to AGND ---------- -0.3V to +45V
SET1, SET2, DISA_DSTO to AGND ---------- -0.3V to +7V
MODE1, MODE2 to AGND ---------- -0.3V to +7V
STI_1, CKI_1, TERM to AGND ---------- -0.3V to +7V
VGH to LVGL/VGL ---------- -0.3V to +55V
LVGL to VGL ---------- -20V to +0.3V

Note1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 3KV
CDM (Charge Discharge Model) ---------- 800V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ---------- 150℃
Operating Junction Temperature Range (TJ) ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range ---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 52℃/W
θ_{JA} (Junction-to-Case Thermal Resistance) ---------- 19℃/W

Recommended Operating Conditions

Over Operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	VIN Supply Range		2.5	3.3	5.5	V
VGH			7.0		40	V
LVGL			-18		-3.0	V
VGL			-18		-3.0	V
$SET1_{HIGH}$	SET1 Input Level voltage	VIN=2.5V to 5.5V	2.5		3.6	V
$SET1_{MIDDLE}$		VIN=2.5V to 5.5V	1.2		2.2	V
$SET1_{LOW}$		VIN=2.5V to 5.5V	0		0.8	V
OCP_EN_{HIGH}	OCP_EN Input Level voltage	VIN=2.5V to 5.5V	2.5		3.6	V
OCP_EN_{MIDDLE}		VIN=2.5V to 5.5V	1.2		2.2	V
OCP_EN_{LOW}		VIN=2.5V to 5.5V	0		0.8	V
$MODE1_{EXTRA\_H}$	MODE1 Input Level voltage	VIN=2.5V to 5.5V	3		4	V
$MODE1_{HIGH}$		VIN=2.5V to 5.5V	1.5		2.5	V
$MODE1_{MIDDLE}$		VIN=2.5V to 5.5V	0.9		1.4	V
$MODE1_{LOW}$		VIN=2.5V to 5.5V	0		0.8	V
$SET2_{HIGH}$	SET2 Input Level voltage	VIN=2.5V to 5.5V	1.5		3.6	V
$SET2_{LOW}$		VIN=2.5V to 5.5V	0		0.8	V
$MODE2_{HIGH}$	MODE2 Input Level voltage	VIN=2.5V to 5.5V	1.5		3.6	V
$MODE2_{LOW}$		VIN=2.5V to 5.5V	0		0.8	V
VIH	Input signal	VIN=2.5V to 5.5V	1.5			V
VIL	Input signal	VIN=2.5V to 5.5V			0.8	V

Electrical Characteristics

VIN = 3.3V, VGH=30V, LVGL=-10V, VGL = -6V, AGND= 0V, TA= 25℃

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VIN	Supply Voltage		2.5	---	5.5	V
V_{INUVLO_R}	VIN Under Voltage Lockout Threshold	VIN rising, hys=200mV	1.9	2.0	2.1	V
V_{INUVLO_F}	VIN Under Voltage Lockout Threshold	VIN falling	1.7	1.8	1.9	V
VGH_20V	VGH Voltage Recognition	VGH rising	19.5	20.0	20.5	V
VGH_{UVLO_R}	VGH Under Voltage Lockout Threshold	VGH rising	6.2	6.55	6.9	V
VGH_{UVLO_F}	VGH Under Voltage Lockout Threshold	VGH falling	6.0	6.35	6.7	V
VGH_{POR}	VGH Power off reset voltage	VGH falling	3	4	5	V
I_{VIN}	VIN Quiescent current	VIN=3.3V, VGH=30V LVGL=VGL=-10V		200	500	uA
I_{VGH}	VGH Quiescent current	VGH=30V LVGL=VGL=-10V Don't input control		1.2	1.8	mA
I_{LVGL}	LVGL Quiescent current	VGH=30V LVGL=VGL=-10V Don't input control		0.5	1.0	mA
I_{VGL}	VGL Quiescent current	VGH=30V LVGL=VGL=-10V Don't input control		100	300	uA
T_{SD}	Thermal Overload Shutdown	Junction Temperature	140	150	160	℃
$R_{PULL.UP}$	Internal Pull UP Resistor	Pull up to VIN	300	400	500	KΩ
$R_{PULL.DOWN}$	Internal Pull Down Resistor	Pull low to GND	300	400	500	KΩ
Level Shifter						
	VGH to AGND		7		40	V
	LVGL, VGL to AGND	LVGL must be earlier (or equal) and the voltage must be lower (or equal) than VGL	-18		0	V
	VGH- (LVGL or VGL)	VGH=40V LVGL/VGL=-15V			55	V
V_{OUT}	STO1~2, LC1~2		LVGL		VGH	V
	CKO_1~CKO_8		LVGL		VGH	V
	VGHD		---		VGH	V
VIH	CKI_1, TERM, STI_1, STI_2, LC_IN Input Level	V_{IN}=2.5V to 5.5V	1.5			V
VIL		V_{IN}=2.5V to 5.5V			0.8	V
VIW	CKI_1, TERM, STI_1, STI_2, LC_IN Input Signal pulse width	V_{IN}=2.5V to 5.5V	300			nS
	CKO_1~CKO_8, STO_1, STO_2, LC1, LC2, Positive Output Swing	I_O=10mA	VGH-0.5	VGH-0.2	VGH	V
	VGHD, XON Positive Output Swing	I_O=10mA	VGH-0.5	VGH-0.2	VGH	V

Electrical Characteristics

VIN = 3.3V, VGH=30V, LVGL=-10V, VGL = -6V, AGND= 0V, TA= 25℃

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level Shifter						
	STO_1, STO_2, LC1, LC2 Negative output swing	I_O=-10mA	LVGL	LVGL+0.2	LVGL+0.5	V
	XON Negative output swing	I_O=-10mA	VGL	VGL+0.2	VGL+0.5	V
$R_{HIGH-SIDE}$	STO_1/2, LC1/2, XON, VGHD High-side switch-on Resistance	I_O=10mA	8	10	15	Ω
$R_{LOW-SIDE}$	STO_1/2, LC1/2 Low-side switch-on Resistance	I_O=-10mA	6	8	12	Ω
$R_{LOW-SIDE}$	XON Low-side switch-on Resistance	I_O=-10mA	2.4	4	6	Ω
T_R	STO_1,STO_2,LC1,LC2 Rising Time	VGH=30V,LVGL=-10V,RL=50Ω , CL=4.7nF, 10%~90%	200	300		V/uS
T_F	STO_1,STO_2,LC1,LC2 Falling Time	VGH=30V,LVGL=-10V,RL=50Ω , CL=4.7nF, 90%~10%	200	300		V/uS
T_{RD}	STO_1,STO_2,LC1,LC2 Rising Edge Delay Time	VGH=30V, LVGL=-10V,50% input to 10% output		100	150	nS
T_{FD}	STO_1,STO_2,LC1,LC2 Falling Edge Delay Time	VGH=30V, LVGL=-10V,50% input to 90% output		100	150	nS
T_{XON}	XON Rising Time	VGH=30V, VGL=-6V,RL=51Ω , CL=4.7nF, 10%~90%	400	500		V/uS
Level Shifter Over current & time setting						
STO_{BT}	STO blanking time		8.1	9	9.9	uS
STO_{HDE}	STO high-side de-noise time		1.6	2	2.4	uS
STO_{LDE}	STO low-side de-noise time		460.8	512	563.2	uS
LC_{BT}	LC1/2 blanking time		8.1	9	9.9	uS
LC_{HDE}	LC1/2 high-side de-noise time		460.8	512	563.2	uS
LC_{LDE}	LC1/2 low-side de-noise time		460.8	512	563.2	uS
XON_{BT}	XON blanking time		8.1	9	9.9	uS
XON_{LDE}	XON low-side de-noise time		460.8	512	563.2	uS

Electrical Characteristics

VIN = 3.3V, VGH=30V, LVGL=-10V, VGL = -6V, AGND= 0V, TA= 25℃

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level Shifter						
	CKO_1~CKO_8 Negative output swing	I_O=-10mA	LVGL	LVGL+ 0.2	LVGL+ 0.5	V
$R_{HIGH-SIDE}$	CKO_1~CKO_8 High-side switch-on Resistance	I_O=10mA	8	10	15	Ω
$R_{LOW-SIDE}$	CKO_1~CKO_8 Low-side switch-on Resistance	I_O=-10mA	6	8	12	Ω
T_R	CKO_1~CKO_8 Rising Time	VGH=30V,LVGL=-10V,RL=50Ω , CL=4.7nF, 10%~90%	400	500		V/uS
T_F	CKO_1~CKO_8 Falling Time	VGH=30V,LVGL=-10V,RL=50Ω , CL=4.7nF, 90%~10%	400	500		V/uS
T_{RD}	CKO_1~CKO_8 Rising Edge Delay Time	VGH=30V, LVGL=-10V,50% input to 10% output		100	150	nS
T_{FD}	CKO_1~CKO_8 Falling Edge Delay Time	VGH=30V, LVGL=-10V,50% input to 90% output		100	150	nS
T_{VGHD_DLY}	VGHD Power on delay time		60	66	72	mS
T_{VGH_SS}	VGHD power on soft start time	Co=4.7uF	3	5	8	mS
T_{VGHD_MASK}	VGH power on mask time		128	148	168	mS
Level Shifter Over current & time setting						
CKO_{BT}	CKO blanking time		8.1	9	9.9	uS
CKO_{HDE}	CKO high-side de-noise time		1.6	2	2.4	uS
CKO_{LDE}	CKO low-side de-noise time		1.6	2	2.4	uS
STO_{BT}	STO blanking time		8.1	9	9.9	uS
STO_{HDE}	STO high-side de-noise time		1.6	2	2.4	uS

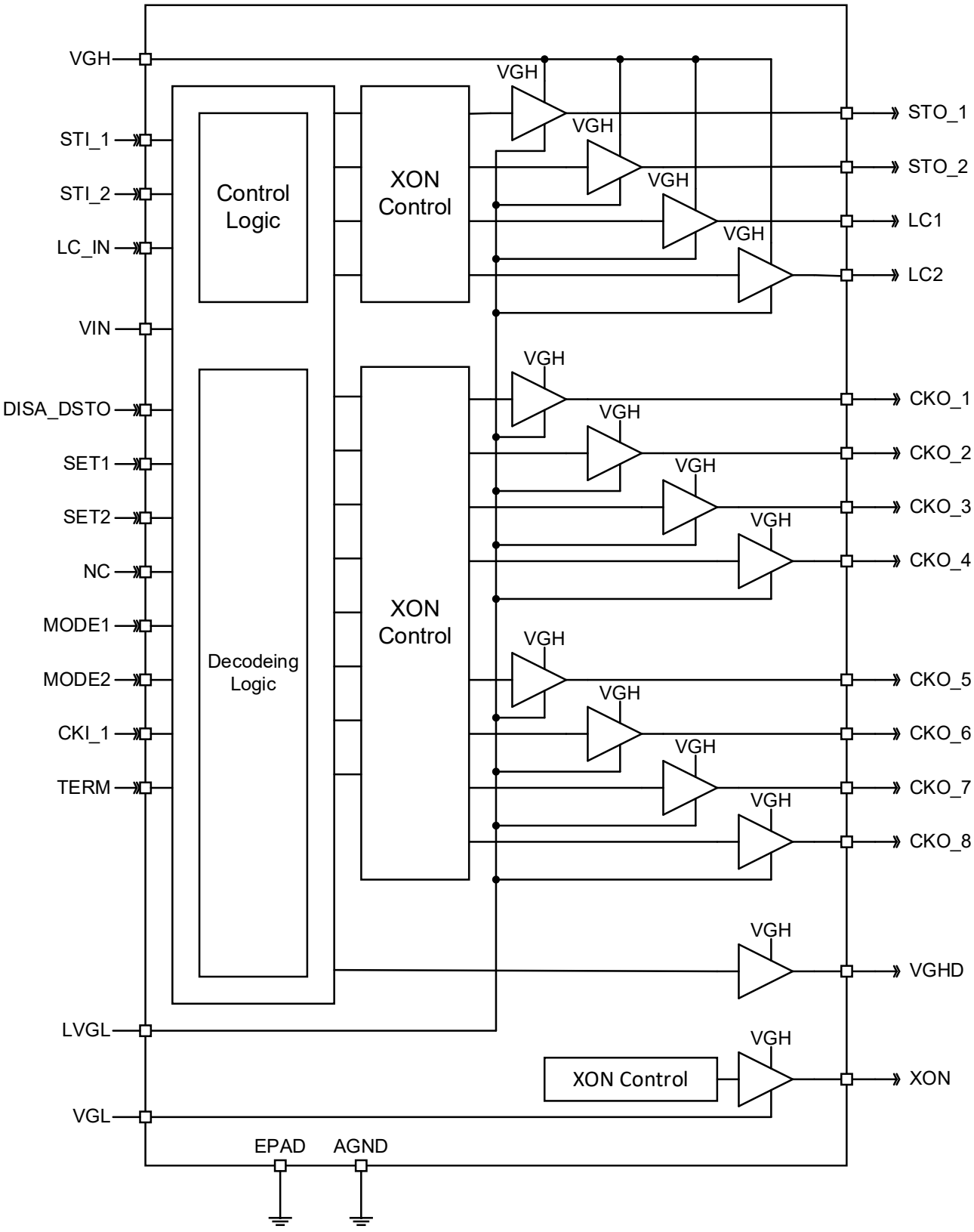
Electrical Characteristics

VIN = 3.3V, VGH=30V, LVGL=-10V, VGL = -6V, AGND= 0V, TA= 25℃

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level Shifter Over current & time setting						
$STO_{H-LIMIT}$	STO high-side OCP level	OCP_EN=LOW	100	120	140	mA
$STO_{L-LIMIT}$	STO low-side OCP level	OCP_EN=LOW	100	120	140	mA
$LC_{H-LIMIT}$	LC high-side OCP level	OCP_EN=LOW	100	120	140	mA
$LC_{L-LIMIT}$	LC low-side OCP level	OCP_EN=LOW	100	120	140	mA
$CKO_{H-LIMIT}$	CKO high-side OCP level	OCP_EN=LOW	100	120	140	mA
$CKO_{L-LIMIT}$	CKO low-side OCP level	OCP_EN=LOW	100	120	140	mA
$XON_{L-LIMIT}$	XON low-side OCP level	OCP_EN=LOW	100	120	140	mA
$STO_{H-LIMIT}$	STO high-side OCP level	OCP_EN=MIDDLE	60	80	100	mA
$STO_{L-LIMIT}$	STO low-side OCP level	OCP_EN=MIDDLE	60	80	100	mA
$LC_{H-LIMIT}$	LC high-side OCP level	OCP_EN=MIDDLE	60	80	100	mA
$LC_{L-LIMIT}$	LC low-side OCP level	OCP_EN=MIDDLE	60	80	100	mA
$CKO_{H-LIMIT}$	CKO high-side OCP level	OCP_EN=MIDDLE	60	80	100	mA
$CKO_{L-LIMIT}$	CKO low-side OCP level	OCP_EN=MIDDLE	60	80	100	mA
$XON_{L-LIMIT}$	XON high-side OCP level	OCP_EN=MIDDLE	60	80	100	mA
Level Shifter Short current & time setting						
CKO_{HDE}	CKO SCP high-side de-noise time		16	20	24	uS
CKO_{LDE}	CKO SCP low-side de-noise time		16	20	24	uS
STO_{HDE}	STO SCP high-side de-noise time		16	20	24	uS
STO_{LDE}	STO SCP low-side de-noise time		16	20	24	uS
LC_{HDE}	LC1/2 SCP high-side de-noise time		16	20	24	uS
LC_{LDE}	LC1/2 SCP low-side de-noise time		16	20	24	uS
XON_{LDE}	XON SCP low-side de-noise time		16	20	24	uS
STO_{H-SCP}	STO high-side SCP level		200	300		mA
STO_{L-SCP}	STO low-side SCP level		200	300		mA
LC_{H-SCP}	LC1/2 high-side SCP level		200	300		mA
LC_{L-SCP}	LC1/2 low-side SCP level		200	300		mA
CKO_{H-SCP}	CKO high-side SCP level		200	300		mA
CKO_{L-SCP}	CKO low-side SCP level		200	300		mA
XON_{L-SCP}	XON high-side SCP level		200	300		mA
$VGHD_{H-SCP}$	VGHD high-side SCP level		200	300		mA

Functional Block Diagram



Typical Application Circuit

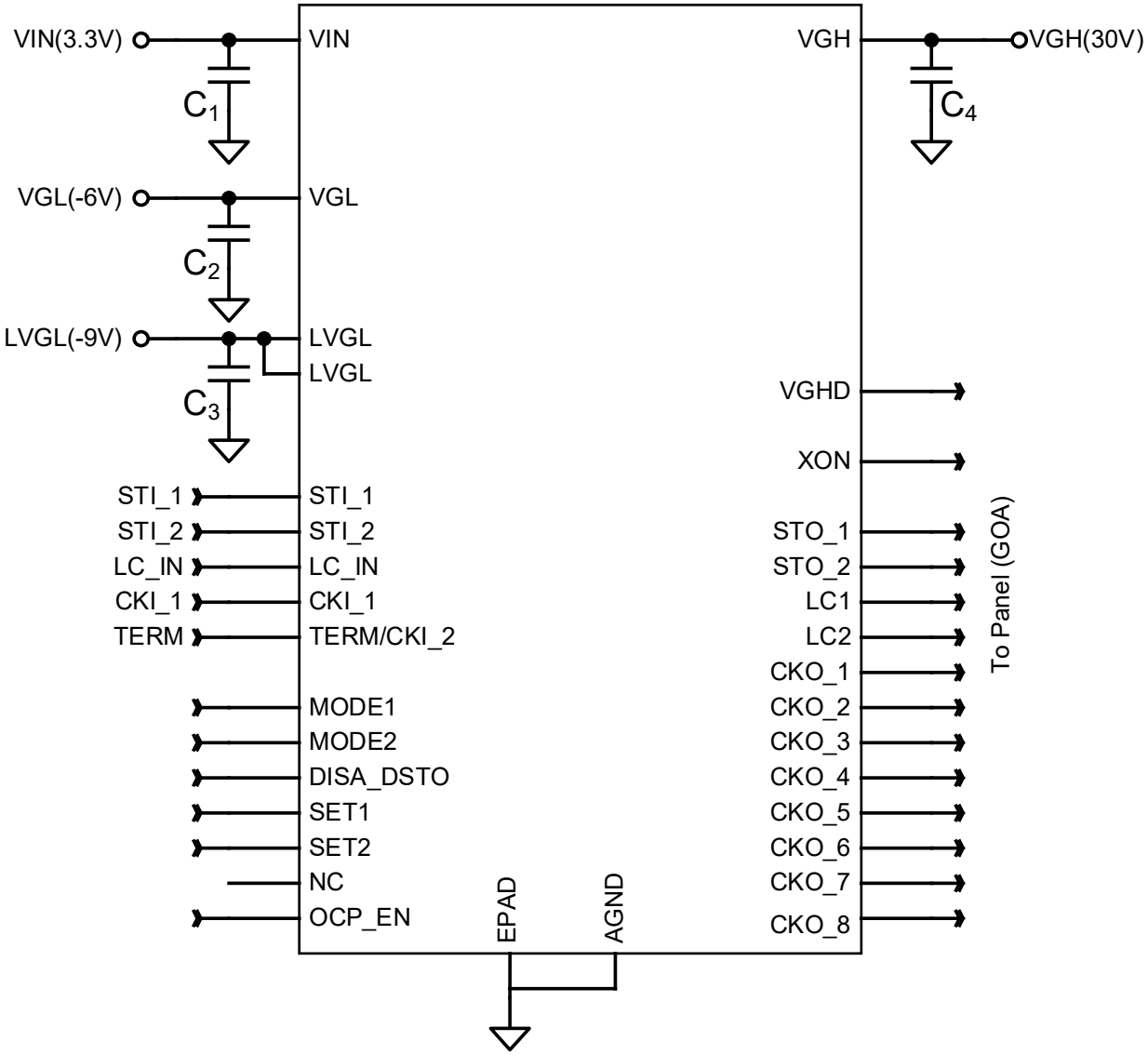


Figure 1. Typical Application Circuit with one in Multi-out

Component List of Figure Recommended

Components	Part Number	Description	Package	Supplier
C1	CL10A106KP8NNNC	10uF/10V, X5R	C0603	SAMSUNG
C2	CL21A106KOQNNNE	10uF/16V, X5R	C0805	SAMSUNG
C3	CL21A106KOQNNNE	10uF/16V, X5R	C0805	SAMSUNG
C4	CL21A475KBQNNNE	4.7uF/50V, X5R	C0805	SAMSUNG

Resistors are set according to application requirements

General Description

The LP6274AQVF provides 14-channel level shifter designed to drive the GOA panel. This device converts the logic-level signals generated by the Timing Controller (T-CON) to high-level signals required by GOA panel.

Power On Sequence

When the VIN exceeds VIN_UVLO, the internal signal ENA for condensed GOA logic will be high. The outputs of Level Shifter STO_1, STO_2 should follow LVGL, CKO_1~CKO_8 should follow LVGL, and XON should follow VGL. The outputs of Level Shifter LC1 and LC2 should follow LC transient one VGH the other LVGL since VIN exceeds UVLO. After ENA high, CKO_1~CKO_8 do not output since receiving the first STI_1 rising edge. After ENA high, LC1 and LC2 will follow LC true table transient.

LC true table		
LC_IN(from TCON)	0	1
LC1	0	1
LC2	1	0

The recommended power-on sequence is
VIN(2.5V~5.5V)→LVGL→VGL→VGH or VIN(2.5V~5.5V)→LVGL//VGL→VGH
The concern of IC design is focus on LVGL and VGL ESD diode. The most negative voltage must be ready before the other two negative voltage.

Power On Condition Table

Case	Analog Power Input			Logic Input			Analog Output			
	VIN	VGH	LVGL VGL	STI_1/2	CKI_1	LC_IN	STO_1/2	CKO_1 ~8	LC1/2	XON
1	>UVLO	>UVLOGH	Don't care	w/i signal	w/i signal	w/i signal	Normal Operation	Normal Operation	LC1=LC LC2=/LC1	VGL
2	>UVLO	>UVLOGH	Don't care	w/i signal	w/o signal	w/i signal	Normal Operation	LVGL	LC1=LC LC2=/LC1	VGL
3	>UVLO	>UVLOGH	Don't care	w/o signal	w/i signal	w/i signal	LVGL	LVGL	LC1=LC LC2=/LC1	VGL
4	>UVLO	>UVLOGH	Don't care	w/i signal	w/i signal	w/o signal	Normal Operation	Normal Operation	LC1=LC LC2=/LC1	VGL
5	>UVLO	>UVLOGH	Don't care	w/o signal	w/i signal	w/o signal	LVGL	LVGL	LC1=LC LC2=/LC1	VGL
6	>UVLO	<UVLOGH >POR	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LC1=LC LC2=/LC1	VGL
7	>UVLO	<POR	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	VGL
8	<UVLO	>POR	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	Hi-Z	VGL
9	<UVLO	<POR	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	VGL

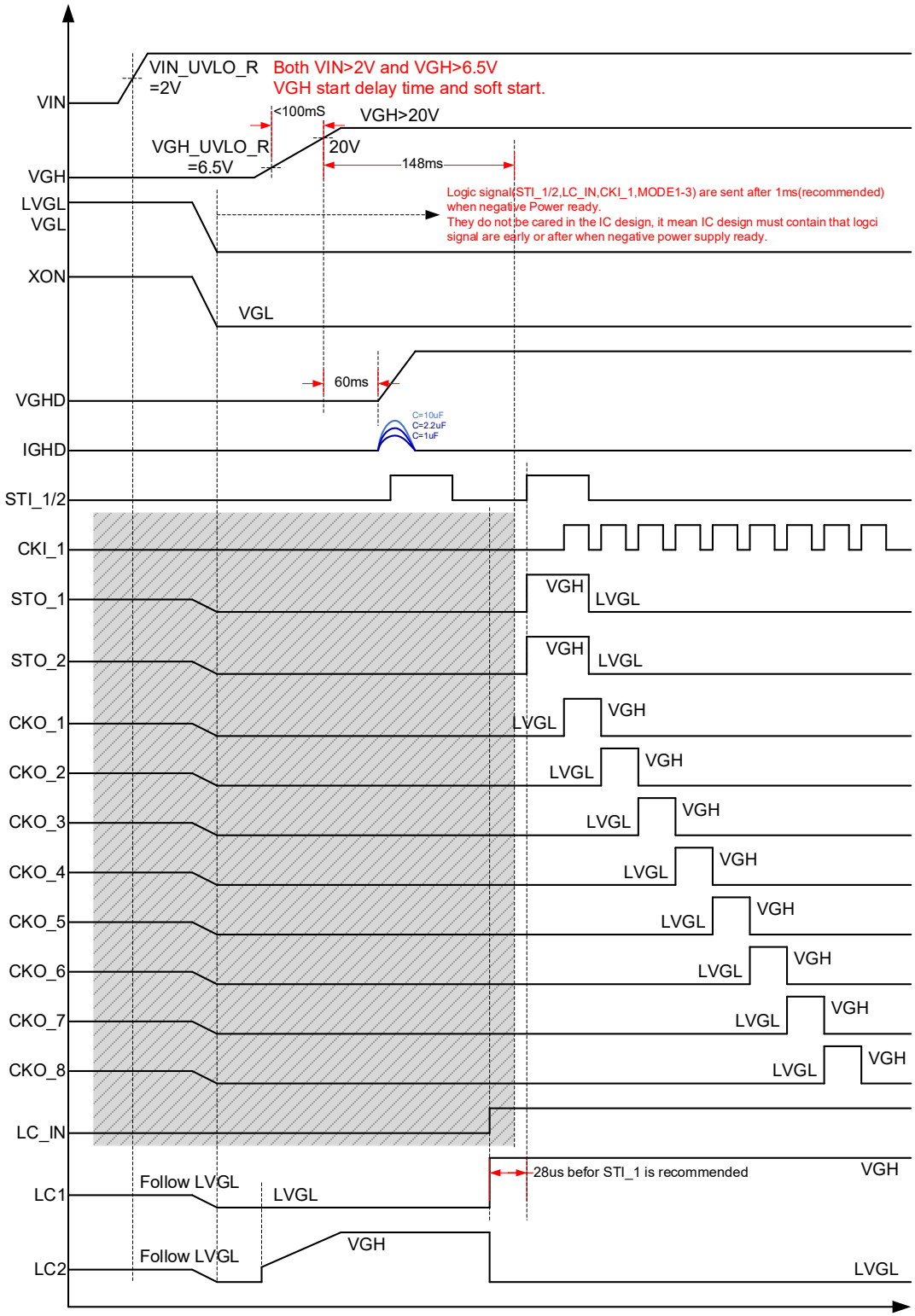
Power on (from 0 to VIN) Condition list-1

Case	Analog Power Input			Logic Input		Analog Output	
	VIN	VGH	LVGL VGL	STI_1	STI_2	STO_1	STO_2
1	>UVLO	>UVLOGH	Don't care	w/i signal	w/i signal	Normal Operation	Normal Operation
2	>UVLO	>UVLOGH	Don't care	w/i signal	w/o signal	Normal Operation	LVGL
3	>UVLO	>UVLOGH	Don't care	w/o signal	w/i signal	LVGL	Normal Operation
4	>UVLO	>UVLOGH	Don't care	w/o signal	w/o signal	LVGL	LVGL
5	>UVLO	<UVLOGH	Don't care	Don't care	Don't care	LVGL	LVGL
6	<UVLO	<UVLOGH	Don't care	Don't care	Don't care	LVGL	LVGL
7	<UVLO	>UVLOGH	Don't care	Don't care	Don't care	LVGL	LVGL

Power on (from 0 to VIN) Condition list-2

Power On Sequence

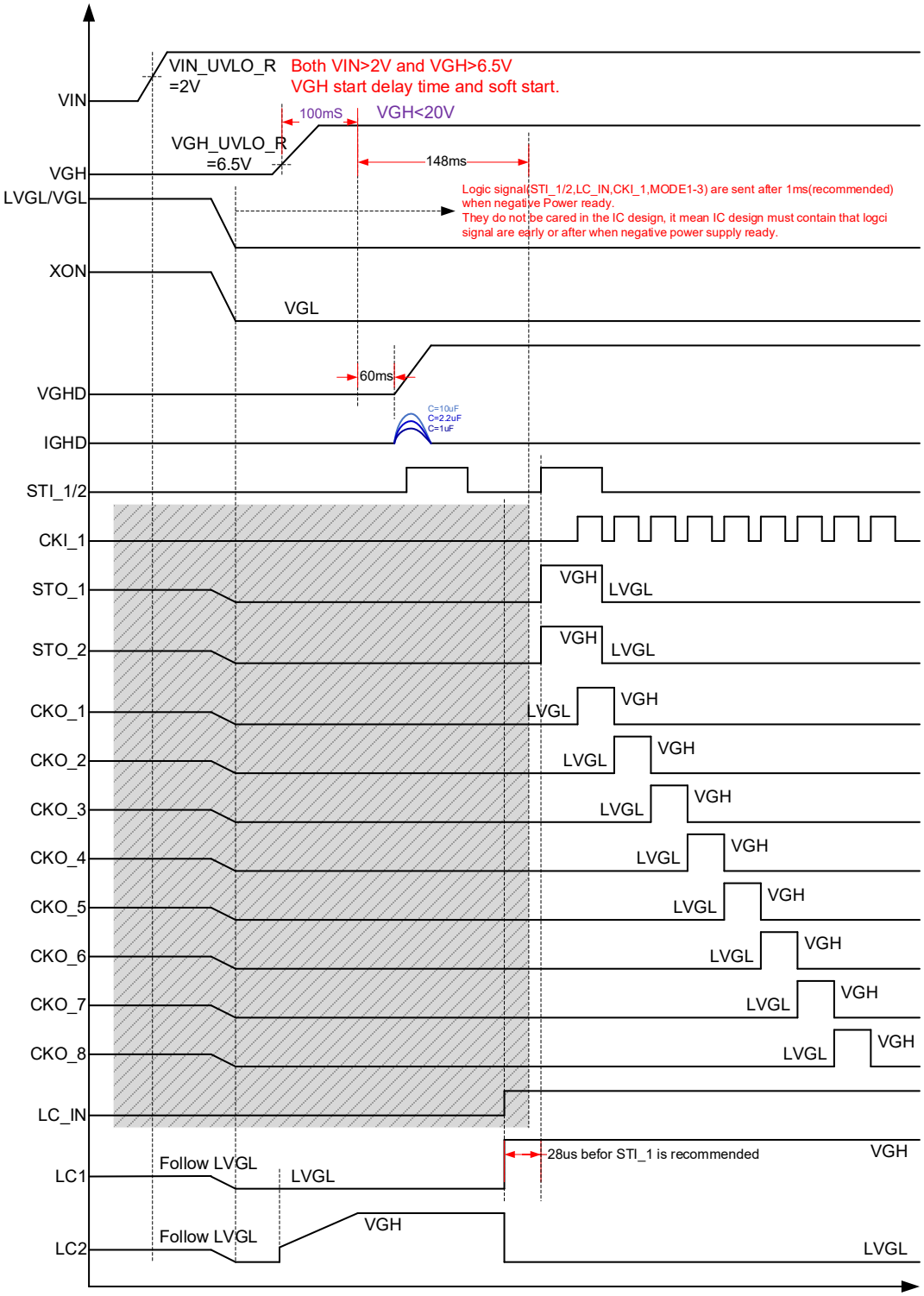
Condition 2: VGH>20V
VIN>LC_IN/STI_2>VGH (20V)>Mask STO_1, STO_2, CKO_1~CKO_8 148ms



Power-On Sequence 1

Power On Sequence

Condition 2: VGH<20V
VIN>LC_IN/STI_2>VGH_UVLO_R>100ms>Mask STO_1, STO_2, CKO_1~CKO_8 148ms



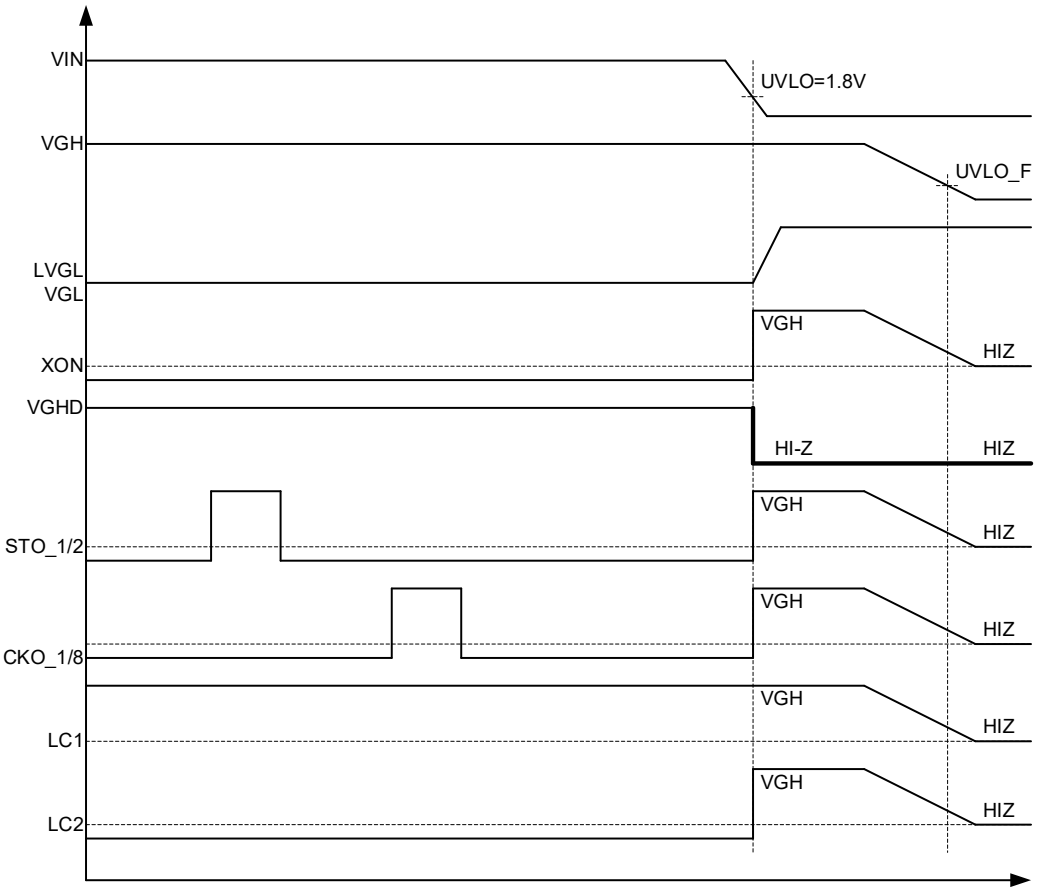
Power-On Sequence 2

Power Off Sequence:

Once the VIN falls below the UVLO_F threshold, LP6274AQVF will have the following actions. Pulling all level shift output as high level (including XON, VGHD, STO_1, STO_2, LC1, LC2 and CKO_1~CKO_8)

Case	Analog Power Input			Logic Input			Analog Output				
	VIN	VGH	LVGL VGL	STI_1	CKI_1	LC_IN	STO_1	CKO_1 ~8	LC1/2	XON	VGHD
1	>UVLO	<UVLO_F >POR	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LC1=LC LC2=/LC1	VGL	Hi-Z
2	>UVLO	<POR	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	VGL	Hi-Z
3	<UVLO	>UVLO_F	Don't care	YES	Don't care	Don't care	Follow VGH	Follow VGH	Follow VGH	Follow VGH	Hi-Z
4	<UVLO	>UVLO_F	Don't care	NO	Don't care	Don't care	LVGL	LVGL	LC1=LC LC2=/LC1	VGL	Hi-Z
5	<UVLO	<UVLO_F	Don't care	YES	Don't care	Don't care	Follow VGH	Follow VGH	Follow VGH	Follow VGH	Hi-Z
6	<UVLO	<UVLO_F	Don't care	NO	Don't care	Don't care	LVGL	LVGL	LC1=LC LC2=/LC1	VGL	Hi-Z
7	<UVLO	<VGH_POR	Don't care	YES	Don't care	Don't care	LVGL	LVGL	LVGL	VGL	Hi-Z

Power off (from VIN to 0) Condition list



Power off sequence (A) VIN UVLO output waveform

Level Shift Function

The LP6274AQVF contains 12 channels level shifter. It is for GOA (Gate On Array) tech. There are 4 signals to generate STO_1~2, LC1~2, and CKO_1~8.VGL is the low voltage level for XON. LVGL is the low voltage level for CKO_1~8. LVGL is the low voltage level for STO_1~2 and LC1~2. Settings about level shifter output are listed below.

Function Setting:

PIN	Status	Level Shifter output
SET1	High level	8 phases. CKO_1~CKO_8 output
	Low level	6 phases. CKO_1~CKO_6 output CKO_7~CKO_8 keep in LVGL
	Floating	4 phases. CKO_1~CKO_4 output CKO_5~CKO_8 keep in LVGL
SET2	High level	There is some time interval between CKO.
	Low/Floating	There is no time interval between CKO.
MODE1	Extra High	3 line pre-charge
	High	2 line pre-charge
	Low	1 line pre-charge
	Middle	No pre-charge
MODE2	High level	CKO 2 line mode phase output
	Low/Floating	CKO 1 line mode phase output
DISA_DSTO	High level	STO_2 follow LVGL
	Low/Floating	STO_2 follow STI_2
OCP_EN	High level	OCP disable
	Floating	100mA
	Low level	60mA

TERM

This is a terminate input pin. Then Terminate input pin is used to pull low the CKO_1~CKO_8 and no more CKI_1 edges can trigger them before next STI_1. CKO_1~CKO_8 can be terminated by next STI_1 if the terminate pin isn't stimulated.

LC_IN

For GOA circuit. Tow low frequency and complementary signals are needed. LC1 will follow LC_IN and LC2 will be the inverting of LC1.

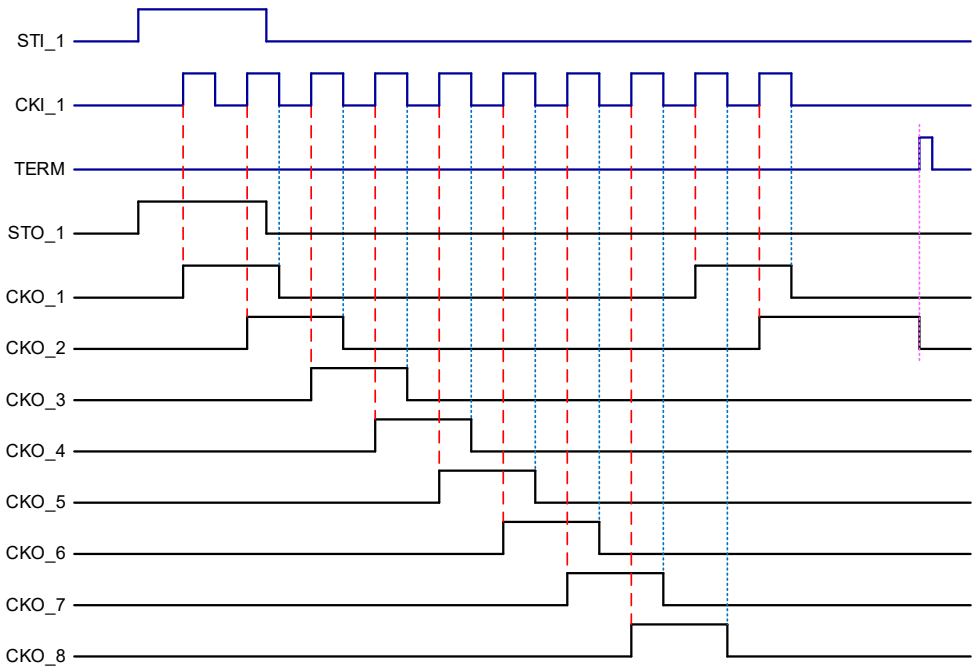
Setting

Level shifter output will be 1-line CKO_S,4-phase, some time interval, and no pre-charge if the settings are not supported. For example, 4-phase with 2-line pre-charge, 2-line CKO_s, some time interval or no time interval, those settings will be led to 1-line CKO_s, 4-phase, time interval, and no pre-charge. The MODE1~2, SET 1~3, OCP_EN will trigger & latch the function by each STI_1 rising edge. The entire setting table is listed on appendix.

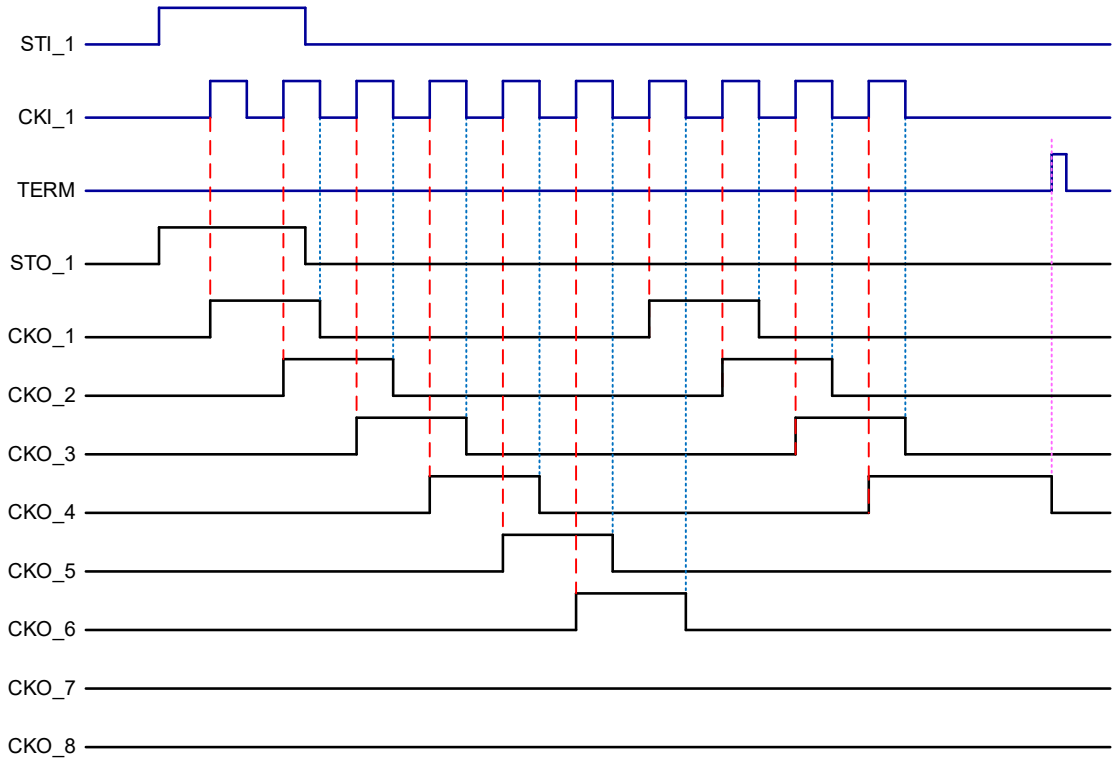
SET1:

SET1 pin is to set the phase number of CKO_s.

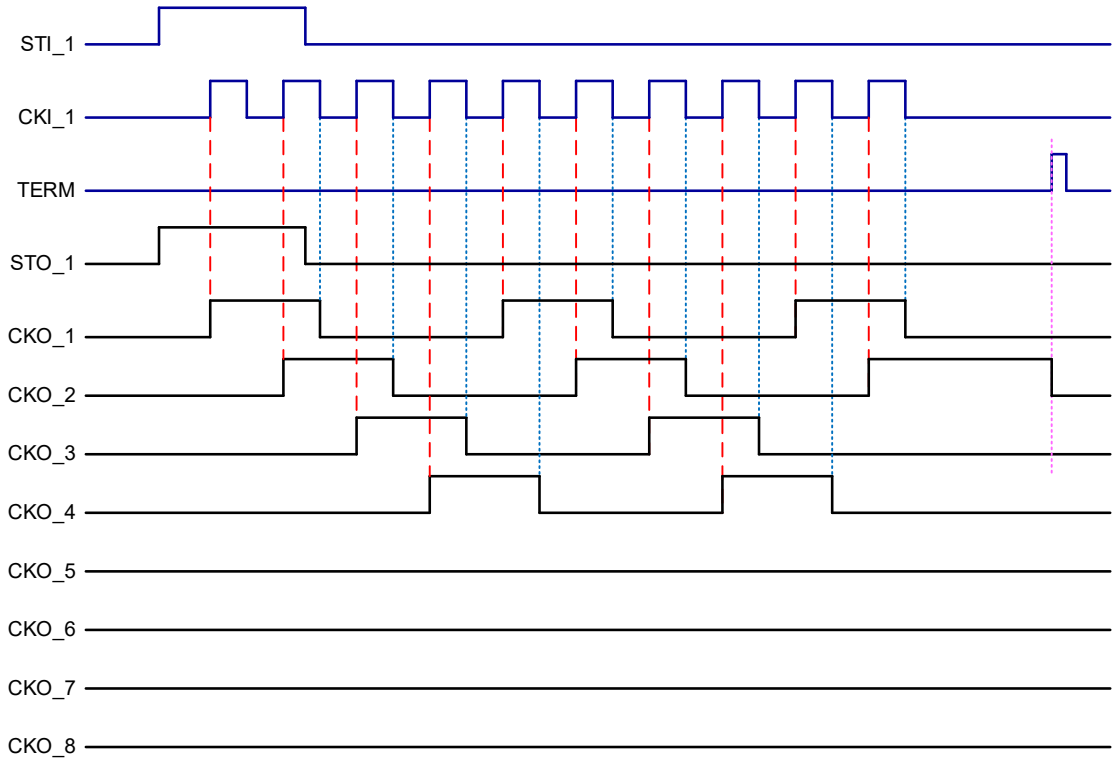
PIN	Status	Level Shifter output
SET1	High level	8 phases. CKO_1~CKO_8 output
	Low level	6 phases. CKO_1~CKO_6 output CKO_7~CKO_8 keep in LVGL
	Floating	4 phases. CKO_1~CKO_4 output CKO_5~CKO_8 keep in LVGL



SET1=High: 8 phase



SET1=Low: 6 phase

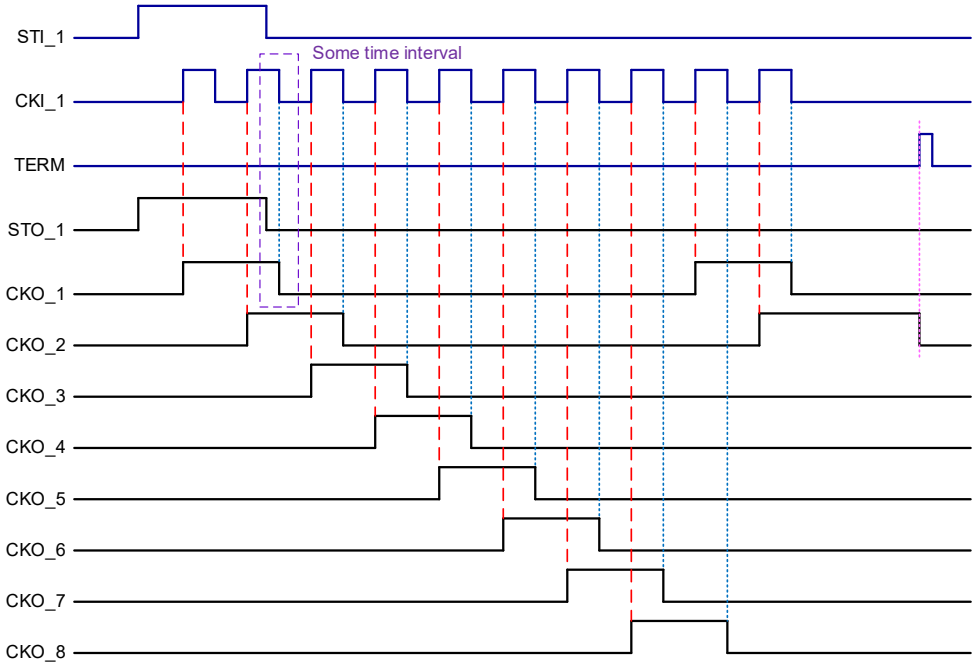


SET1=Floating: 4 phase

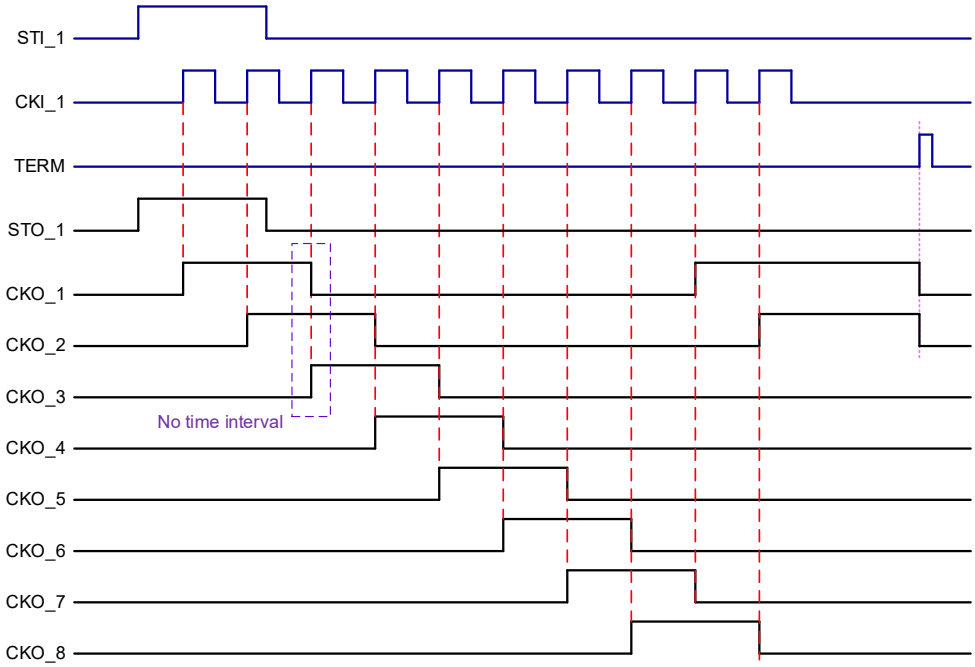
SET2:

SET2 pin is to set some time / no time interval between CKO_s.

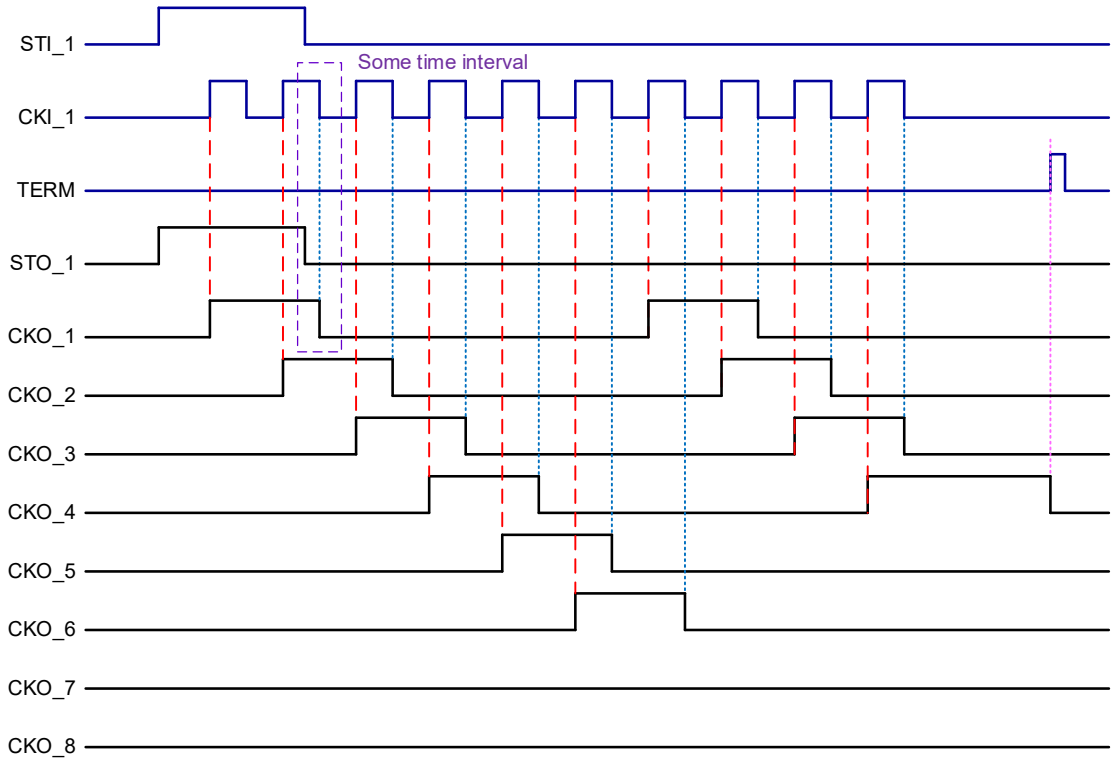
PIN	Status	Level Shifter output
SET2	High level	Some time interval
	Low/Floating	No time interval



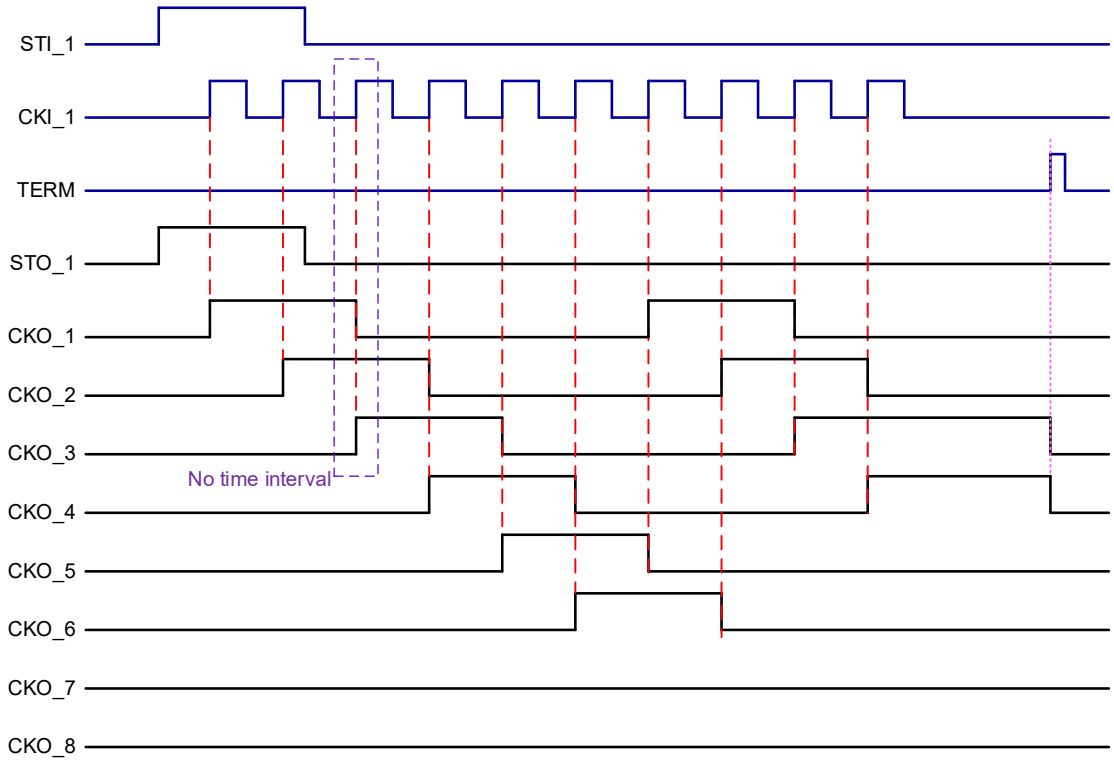
SET1=High: 8 phase ; SET2=High: Some time



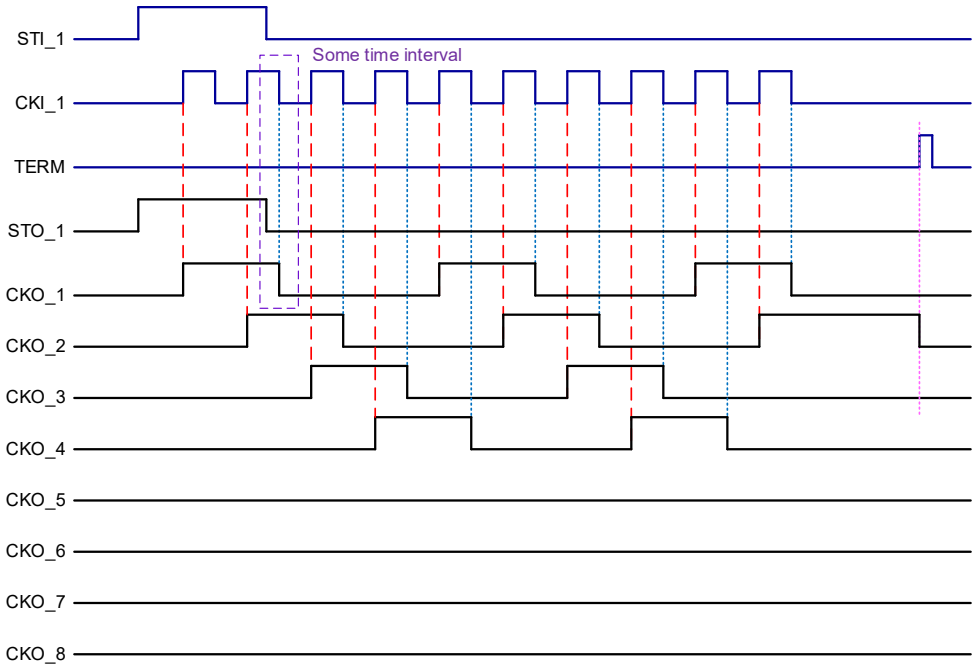
SET1=High: 8 phase ; SET2=Low: No time



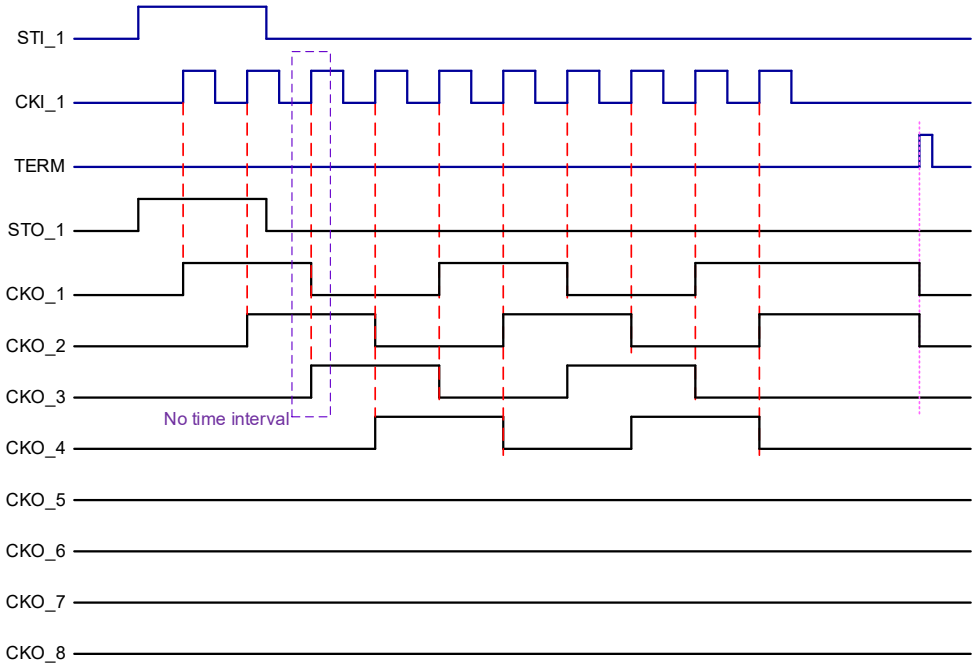
SET1=Low: 6 phase ; SET2=High: Some time



SET1=Low: 6 phase ; SET2=Low: No time



SET1=Floating: 4 phase ; SET2=High: Some time

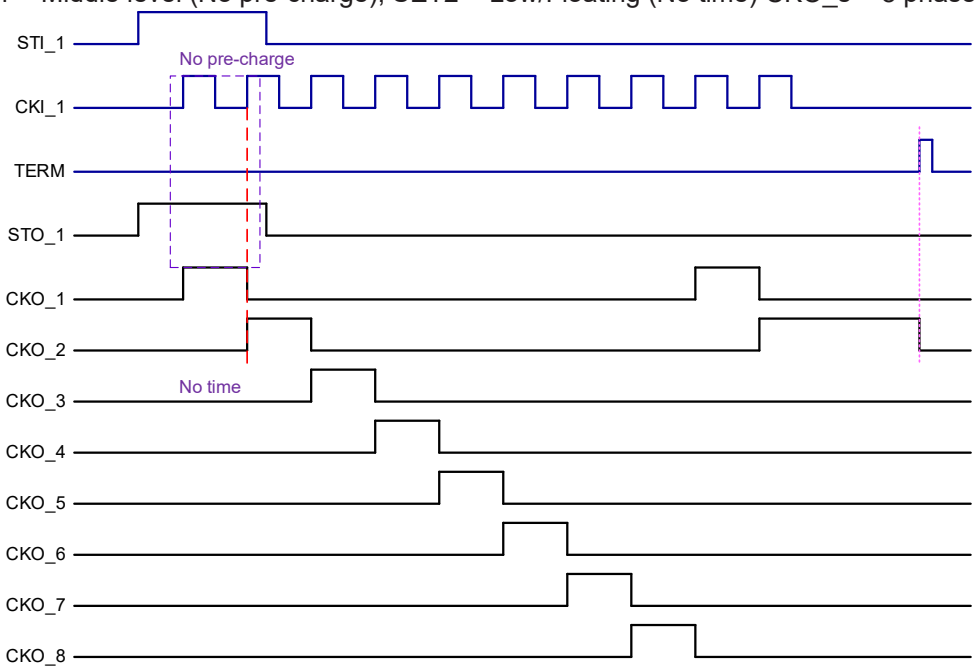


SET1=Floating: 4 phase ; SET2=Low: No time

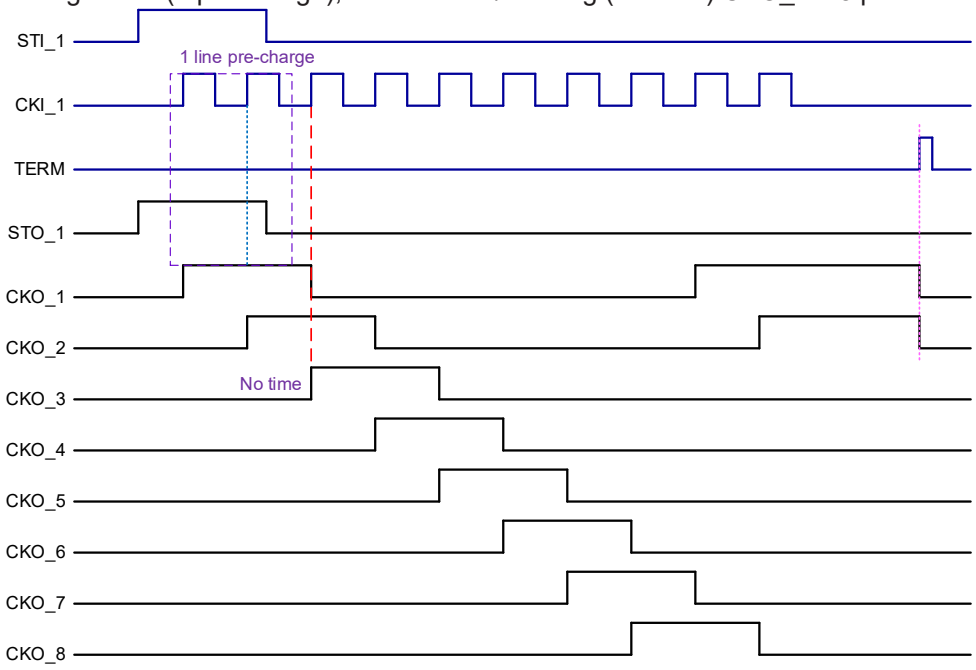
MODE1:
MODE1 is the function of pre-charge type. Mode1 function is list below.

PIN	Logic Level	Logic Level	Logic Level	Logic Level	Logic Level	Logic Level	Logic Level	Logic Level
MODE1	Extra-H	H	M	L	Extra-H	H	M	L
SET2	0	0	0	0	1	1	1	1
Function	3 line pre-No time	1 line pre-No time	No pre-No time	2 line pre-No time	3 line pre-some time	1 line pre-some time	No pre-some time	2 line pre-some time

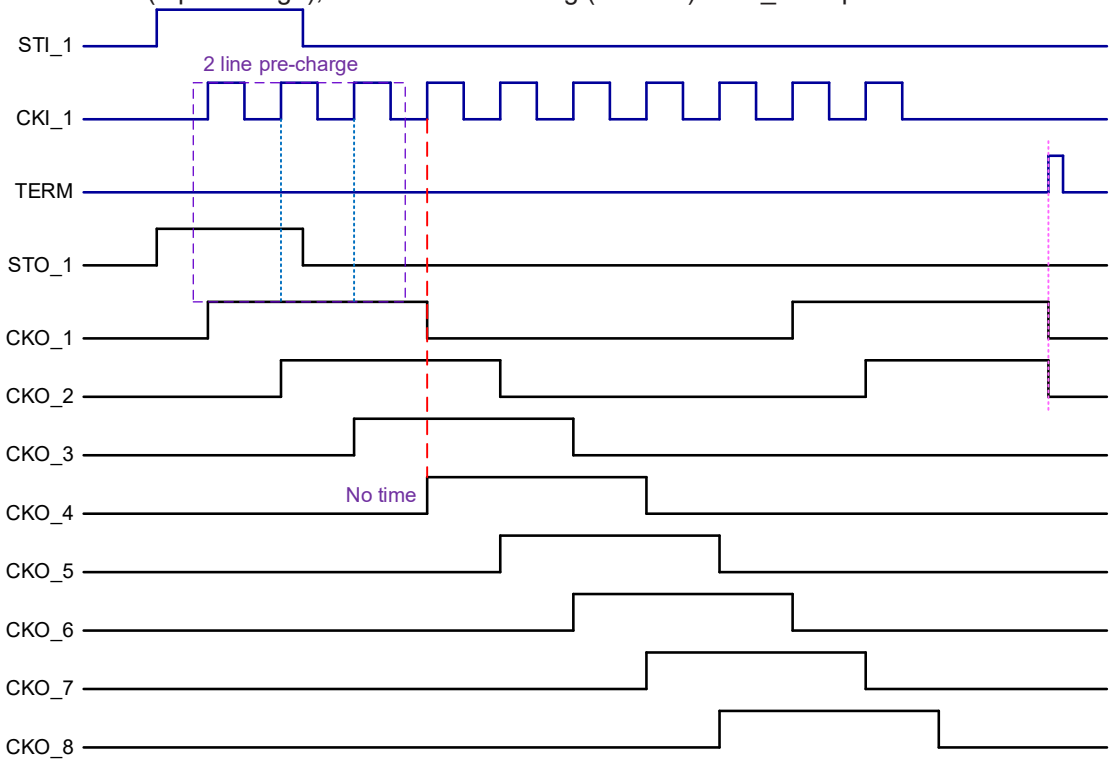
MODE1 = Middle level (No pre-charge); SET2 = Low/Floating (No time) CKO_s = 8 phase



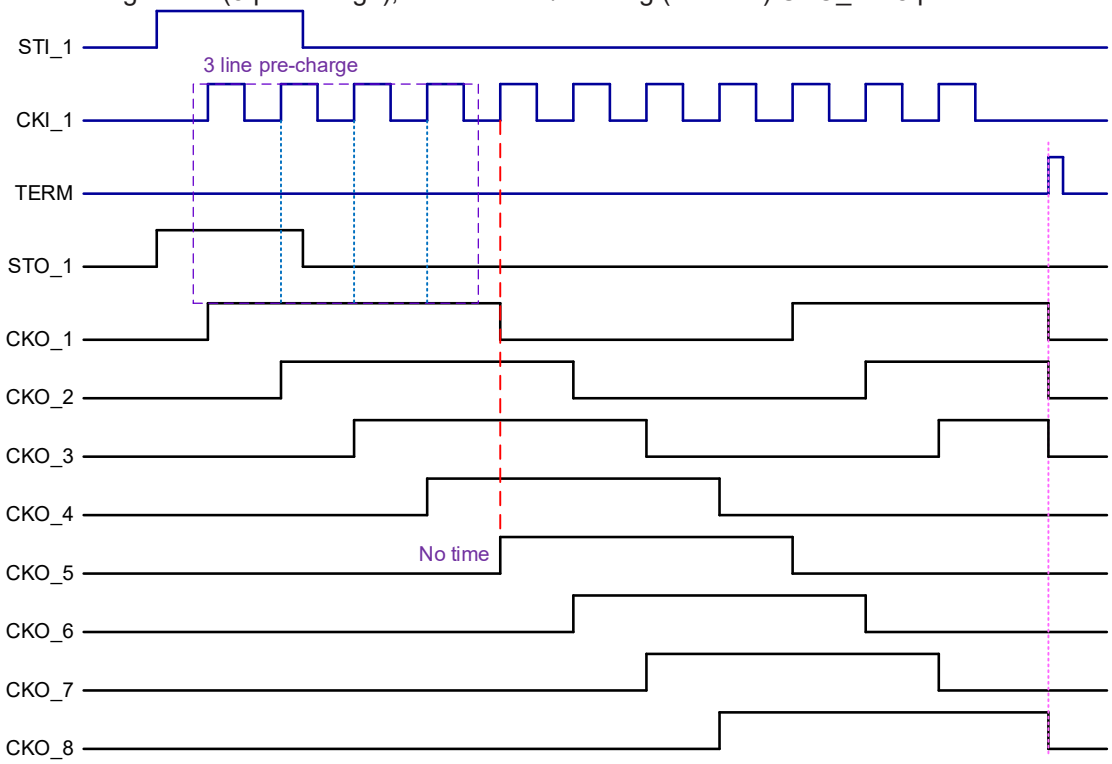
MODE1 = High level (1 pre-charge); SET2 = Low/Floating (No time) CKO_s = 8 phase



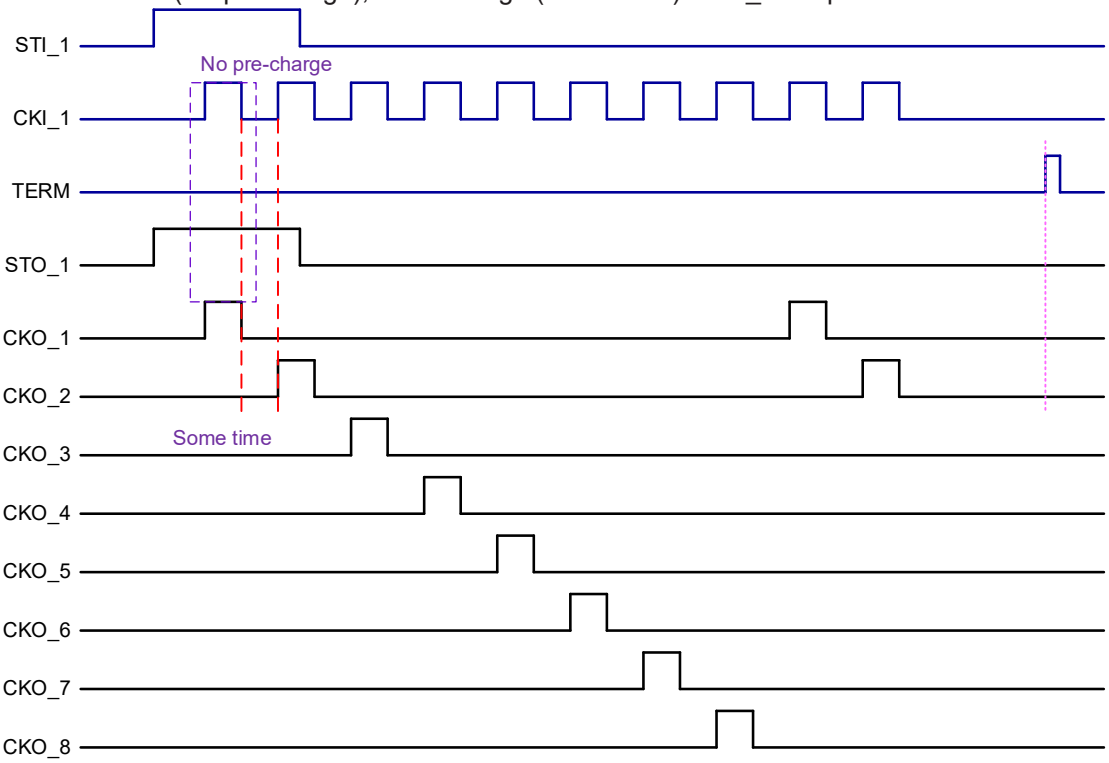
MODE1 = Low level (2 pre-charge); SET2 = Low/Floating (No time) CKO_s = 8 phase



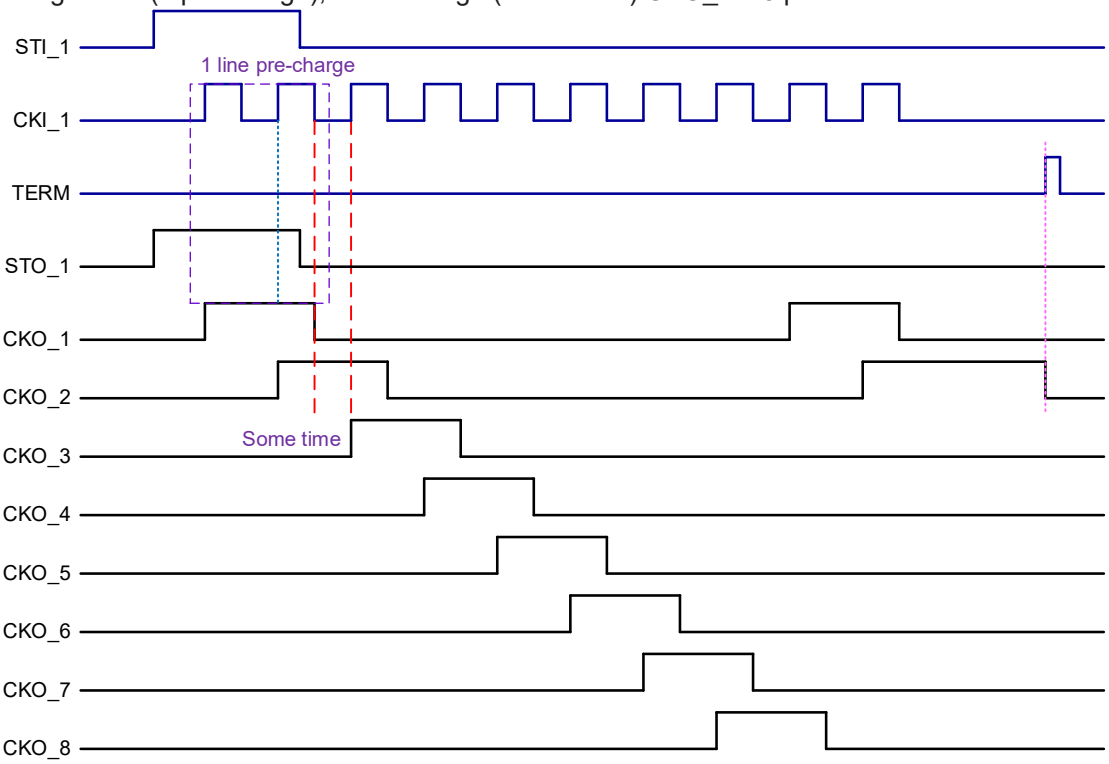
MODE1 = Extra High level (3 pre-charge); SET2 = Low/Floating (No time) CKO_s = 8 phase



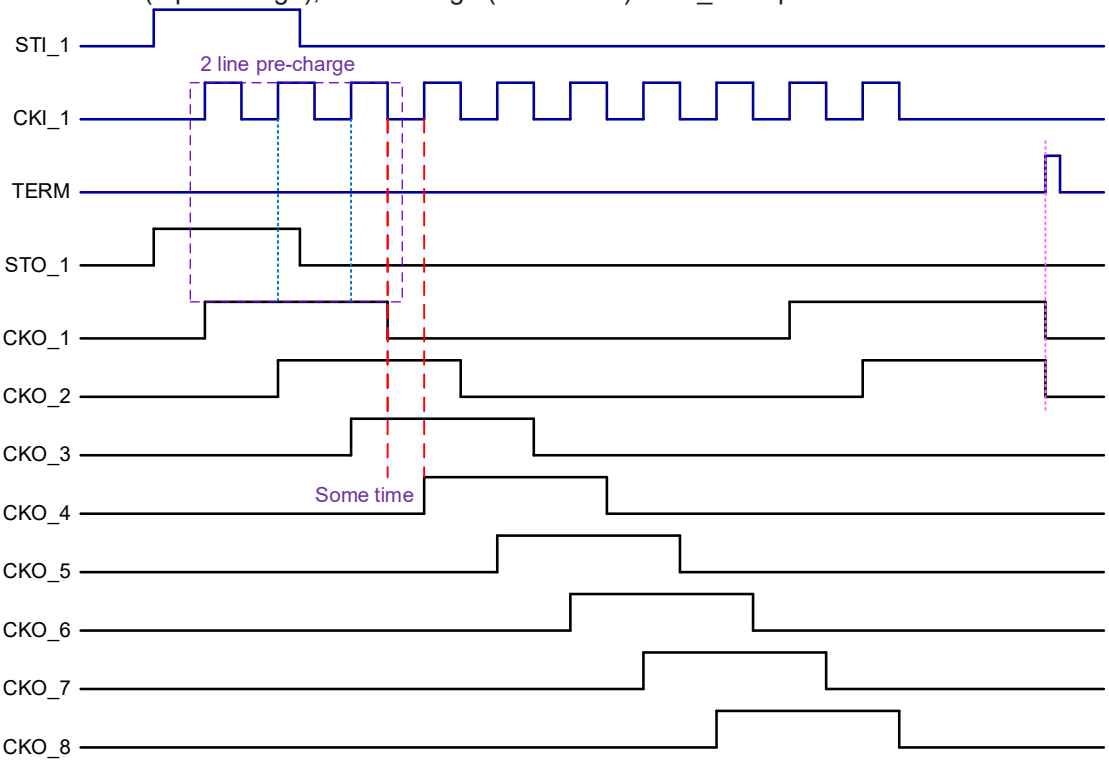
MODE1 = Middle level (No pre-charge); SET2 = High (Some time) CKO_s = 8 phase



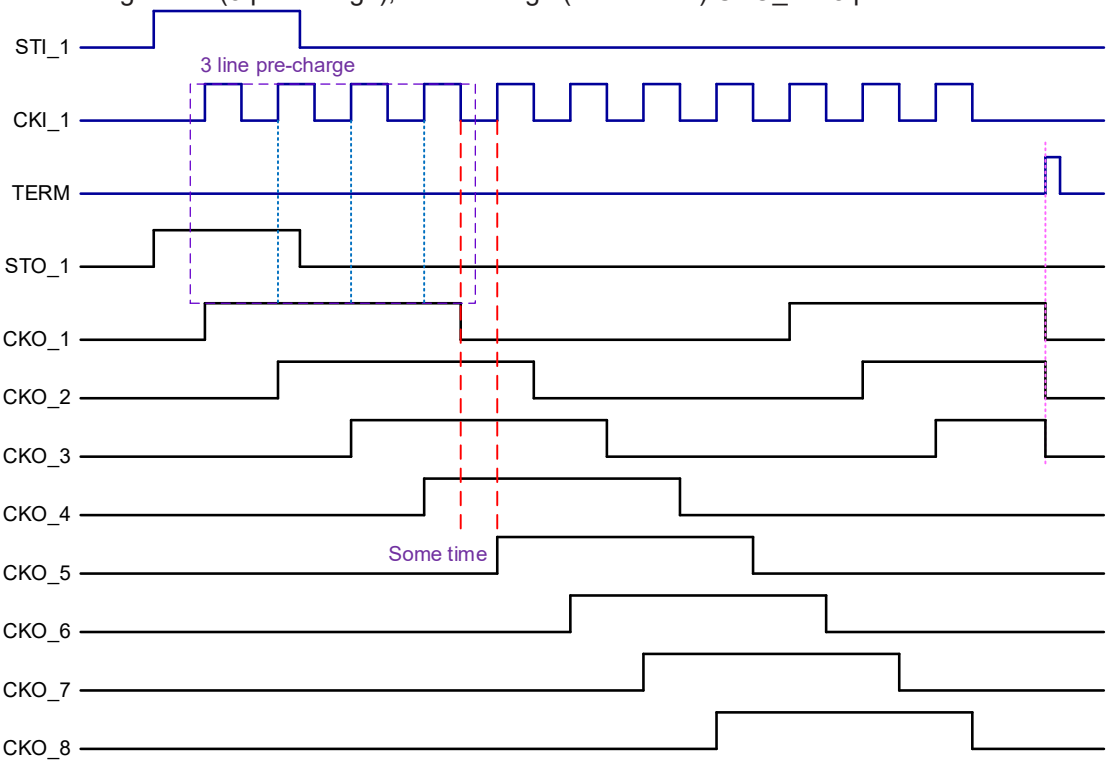
MODE1 = High level (1 pre-charge); SET2 = High (Some time) CKO_s = 8 phase



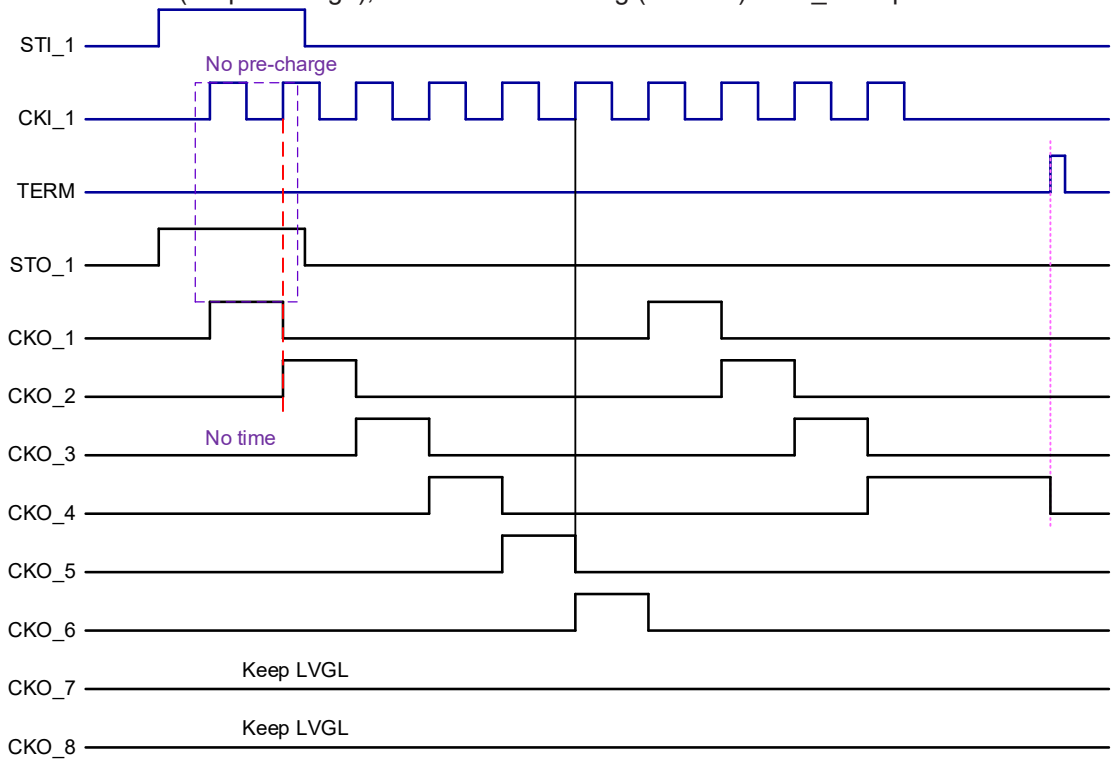
MODE1 = Low level (2 pre-charge); SET2 = High (Some time) CKO_s = 8 phase



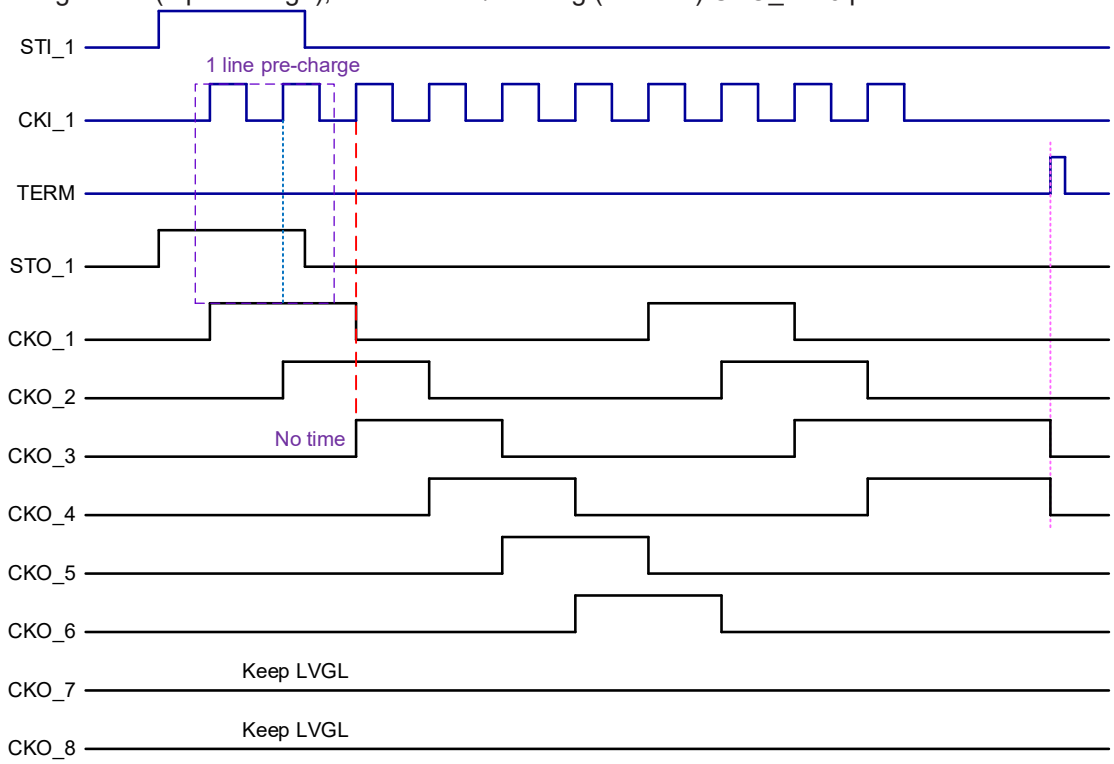
MODE1 = Extra High level (3 pre-charge); SET2 = High (Some time) CKO_s = 8 phase



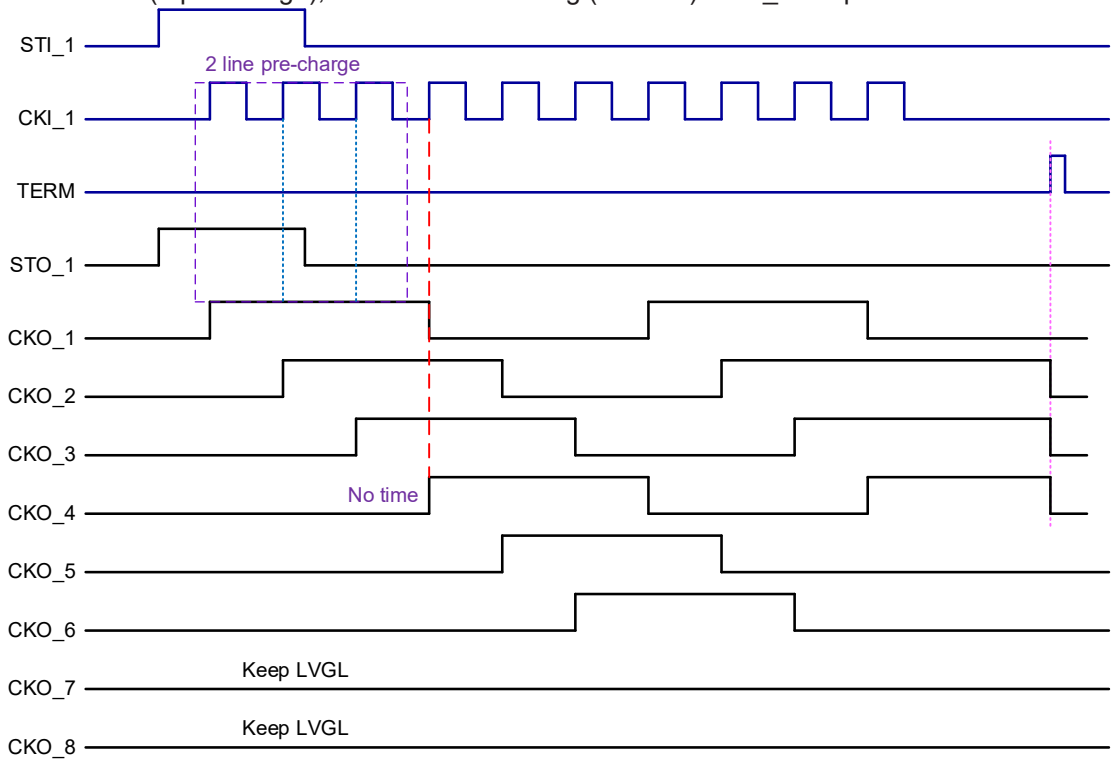
MODE1 = Middle level (No pre-charge); SET2 = Low/Floating (No time) CKO_s = 6 phase



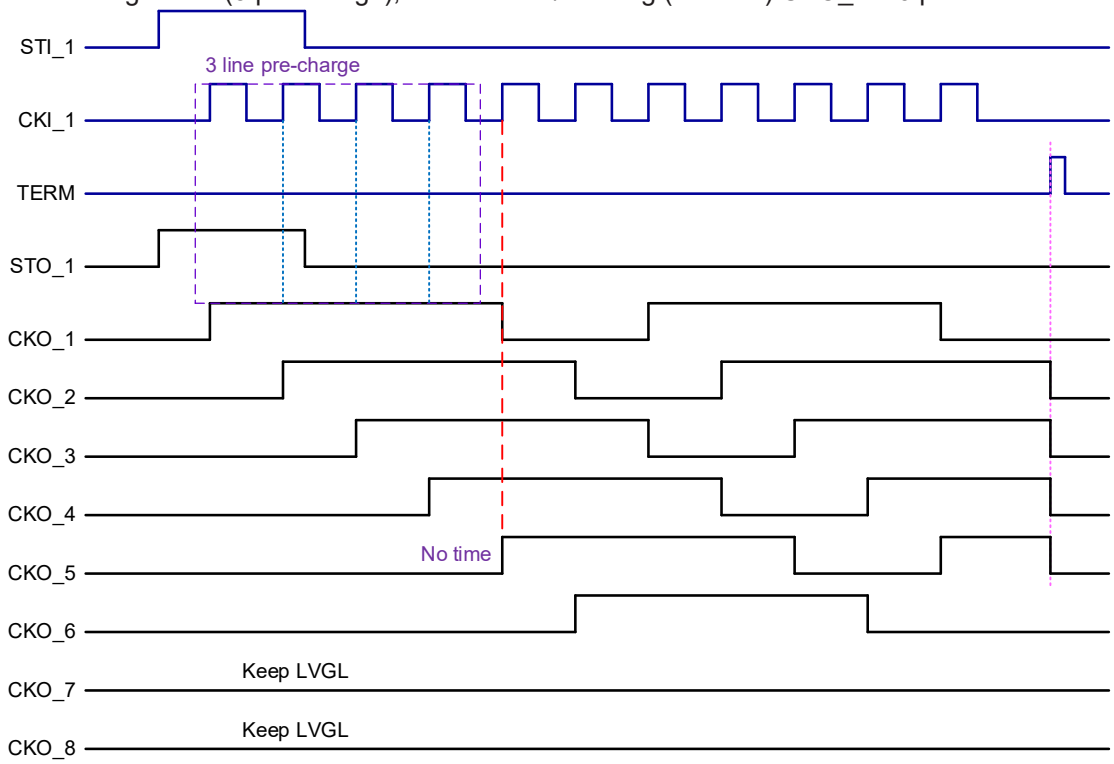
MODE1 = High level (1 pre-charge); SET2 = Low/Floating (No time) CKO_s = 6 phase



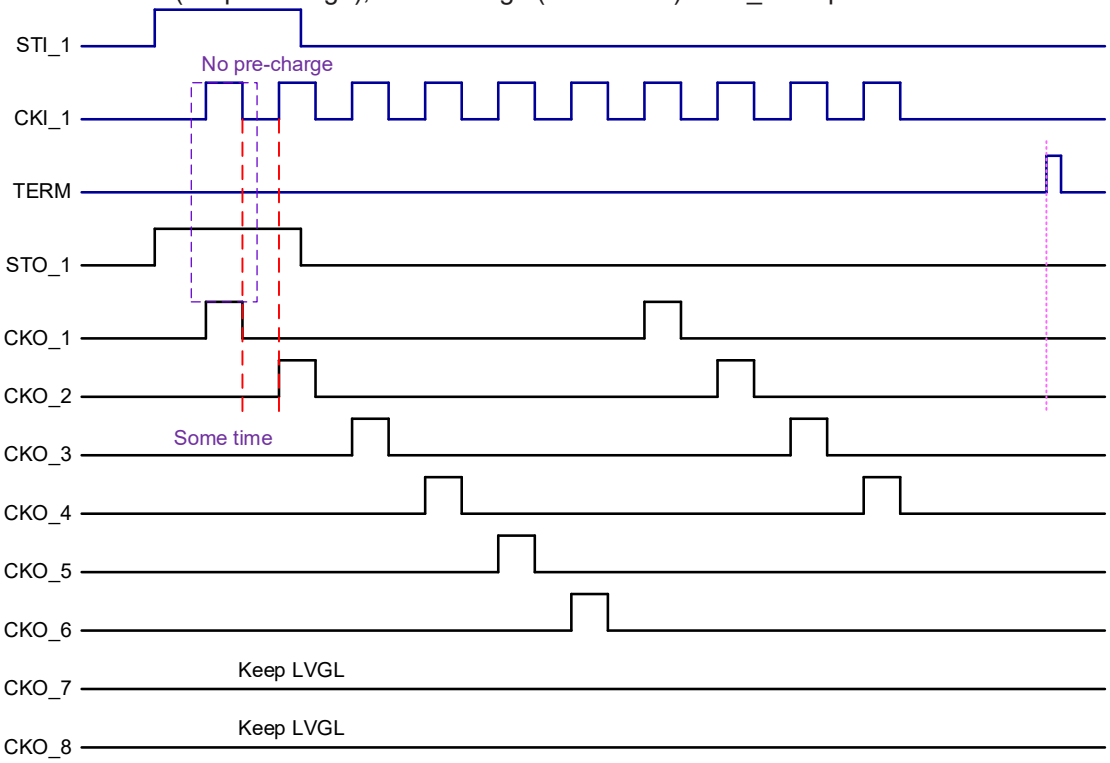
MODE1 = Low level (2 pre-charge); SET2 = Low/Floating (No time) CKO_s = 6 phase



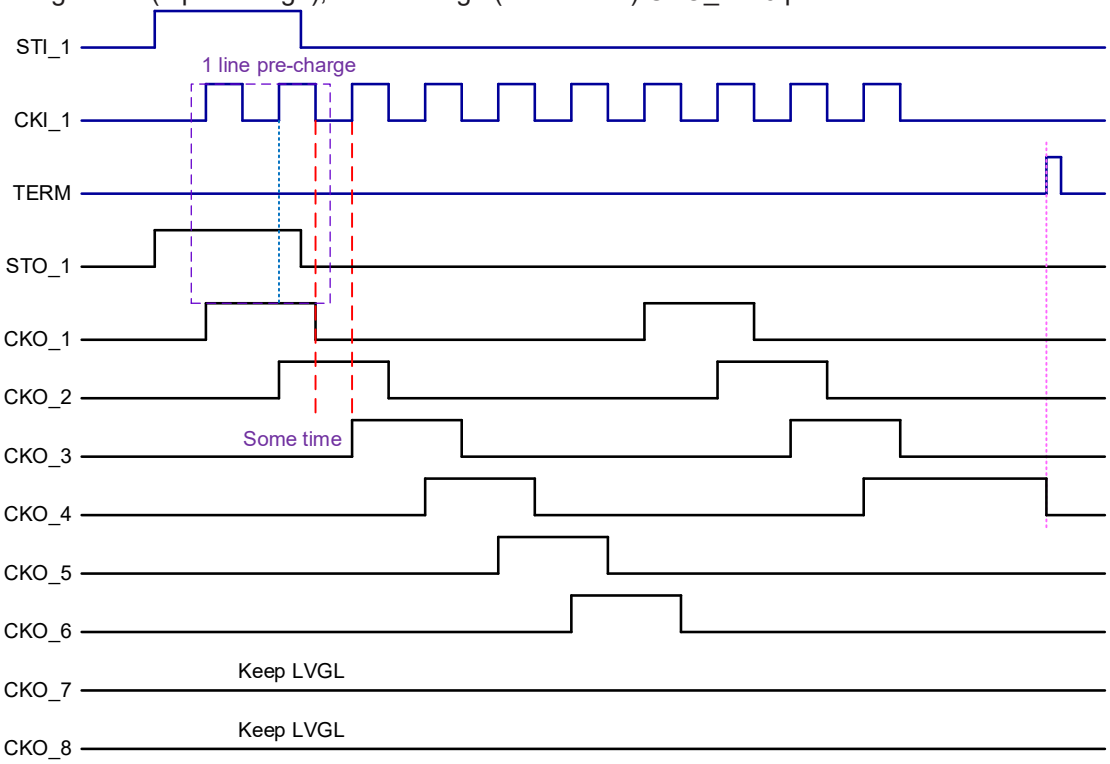
MODE1 = Extra High level (3 pre-charge); SET2 = Low/Floating (No time) CKO_s = 6 phase



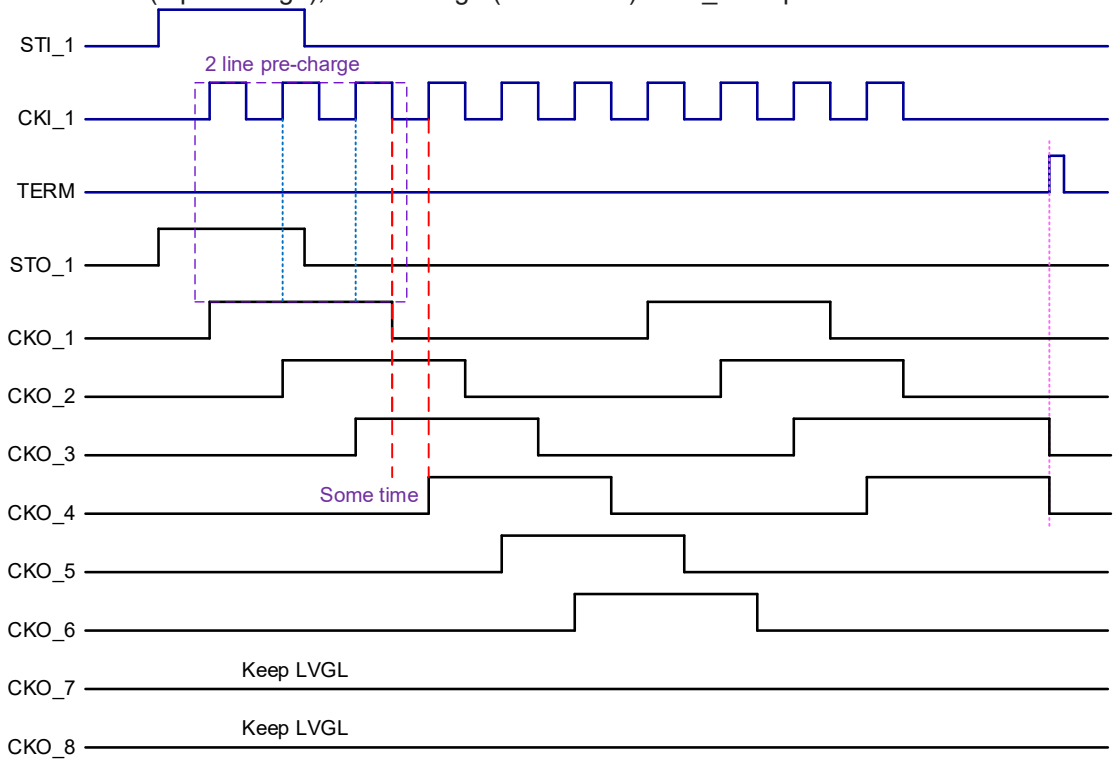
MODE1 = Middle level (No pre-charge); SET2 = High (Some time) CKO_s = 6 phase



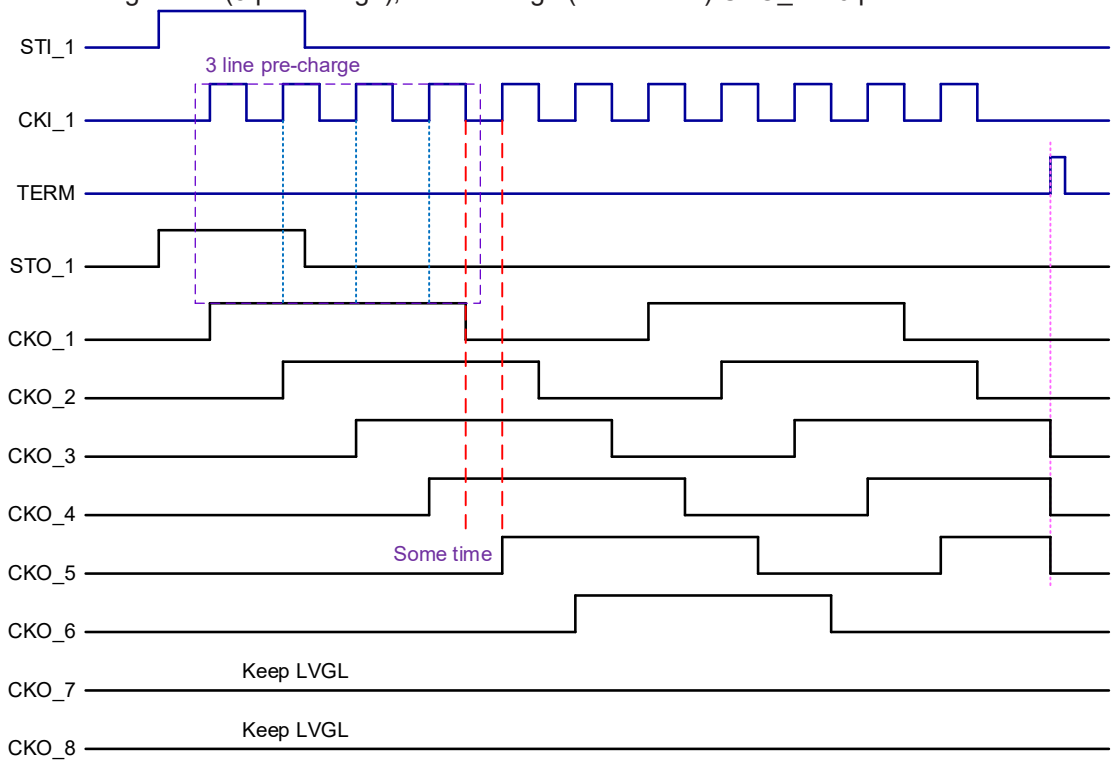
MODE1 = High level (1 pre-charge); SET2 = High (Some time) CKO_s = 6 phase



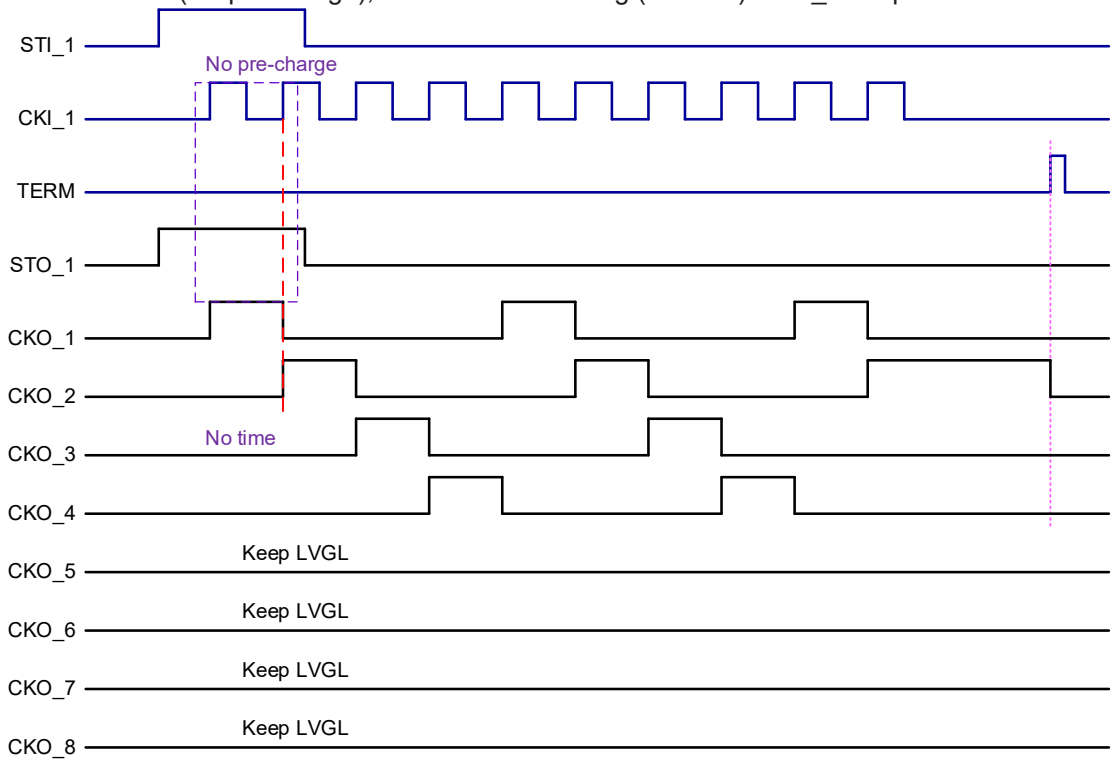
MODE1 = Low level (2 pre-charge); SET2 = High (Some time) CKO_s = 6 phase



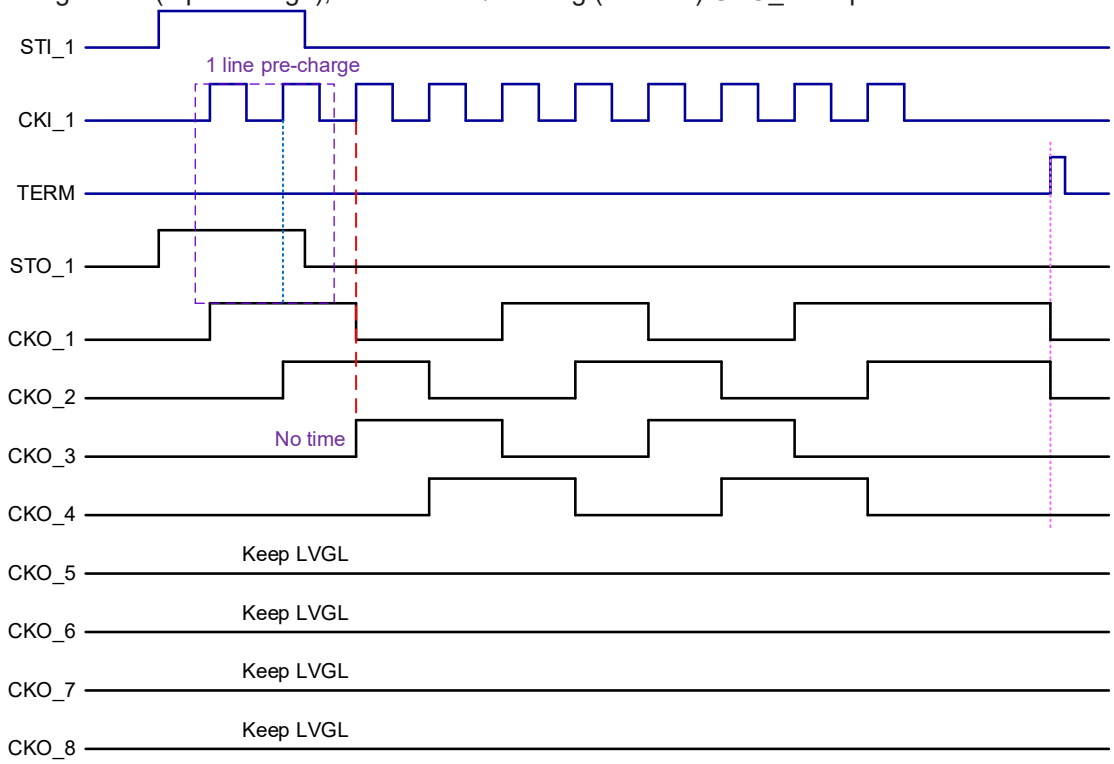
MODE1 = Extra High level (3 pre-charge); SET2 = High (Some time) CKO_s = 6 phase



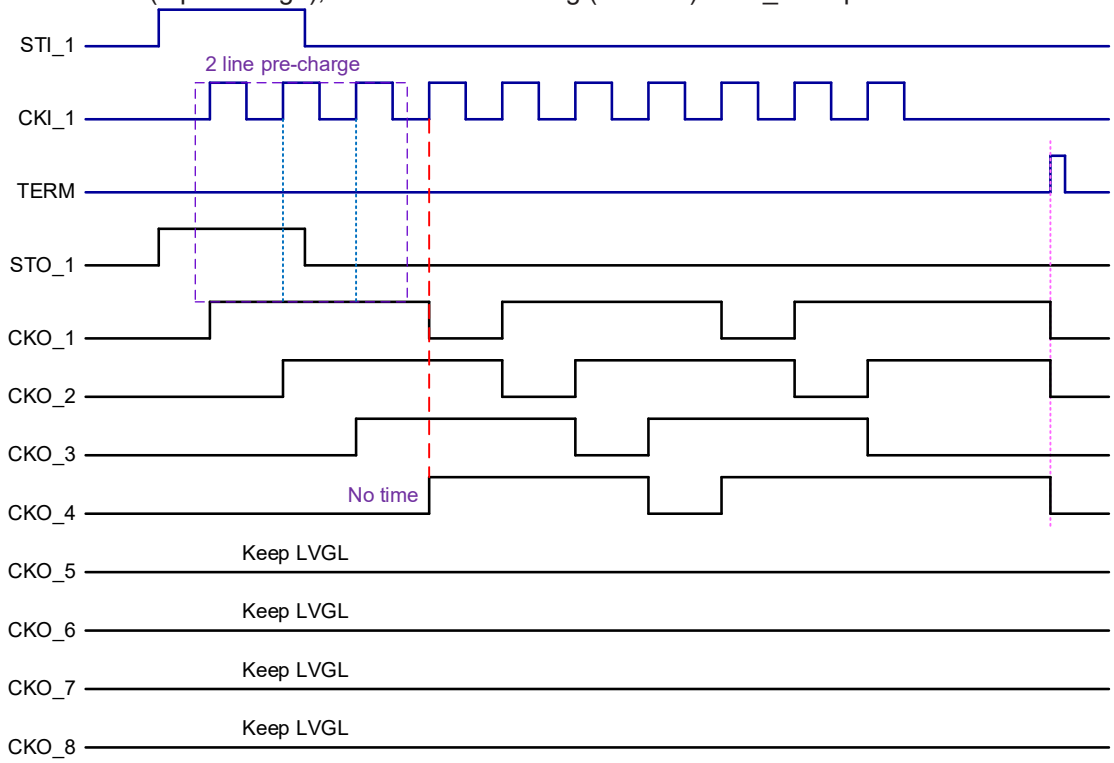
MODE1 = Middle level (No pre-charge); SET2 = Low/Floating (No time) CKO_s = 4 phase



MODE1 = High level (1 pre-charge); SET2 = Low/Floating (No time) CKO_s = 4 phase



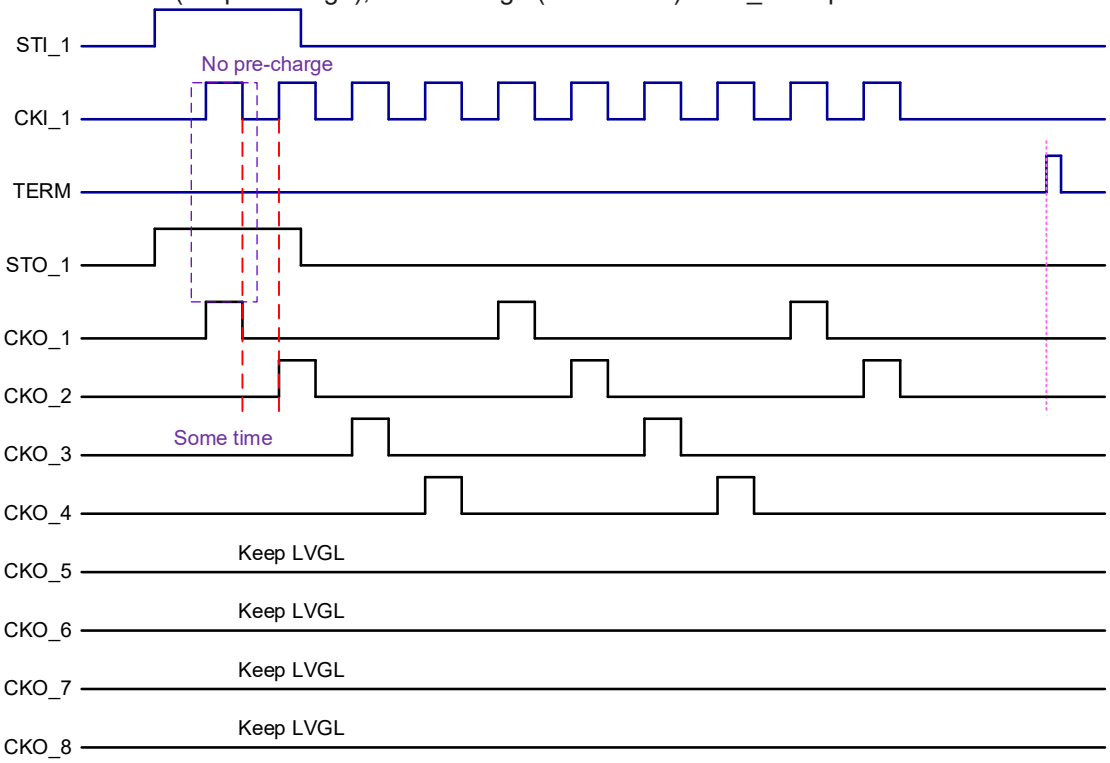
MODE1 = Low level (2 pre-charge); SET2 = Low/Floating (No time) CKO_s = 4 phase



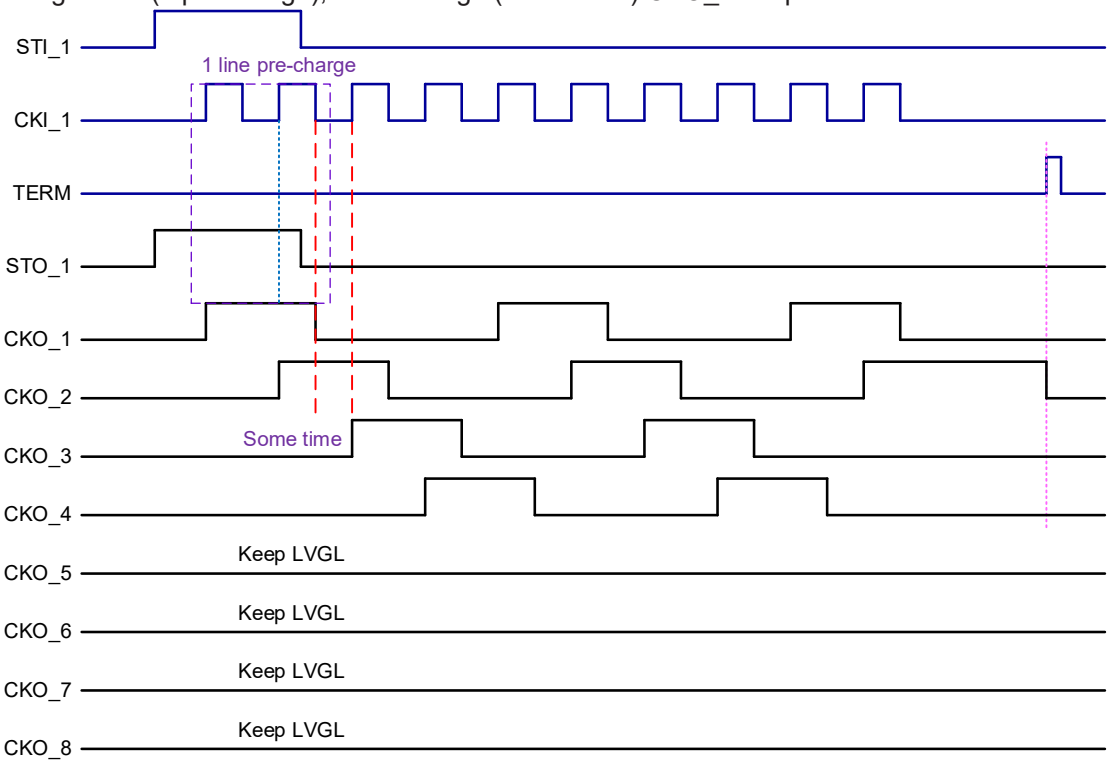
MODE1 = Extra High level (3 pre-charge); SET2 = Low/Floating (No time) CKO_s = 4 phase

Invalid setting (All CKO output always pull low LVGL)

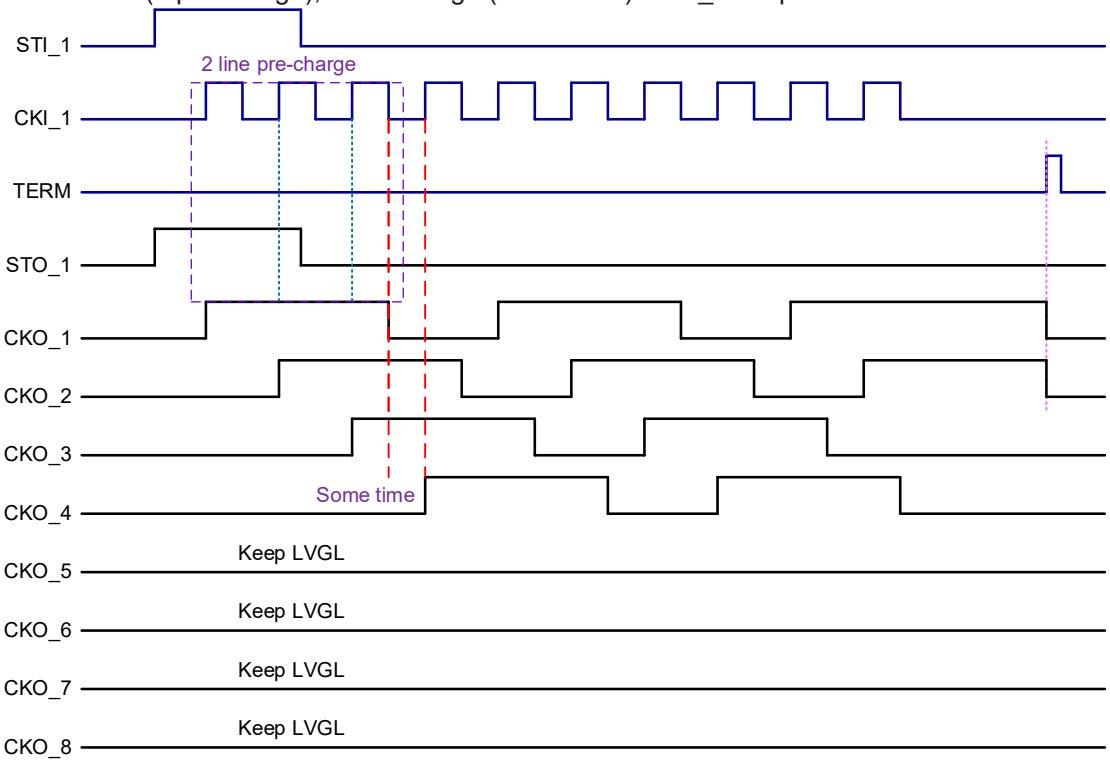
MODE1 = Middle level (No pre-charge); SET2 = High (Some time) CKO_s = 4 phase



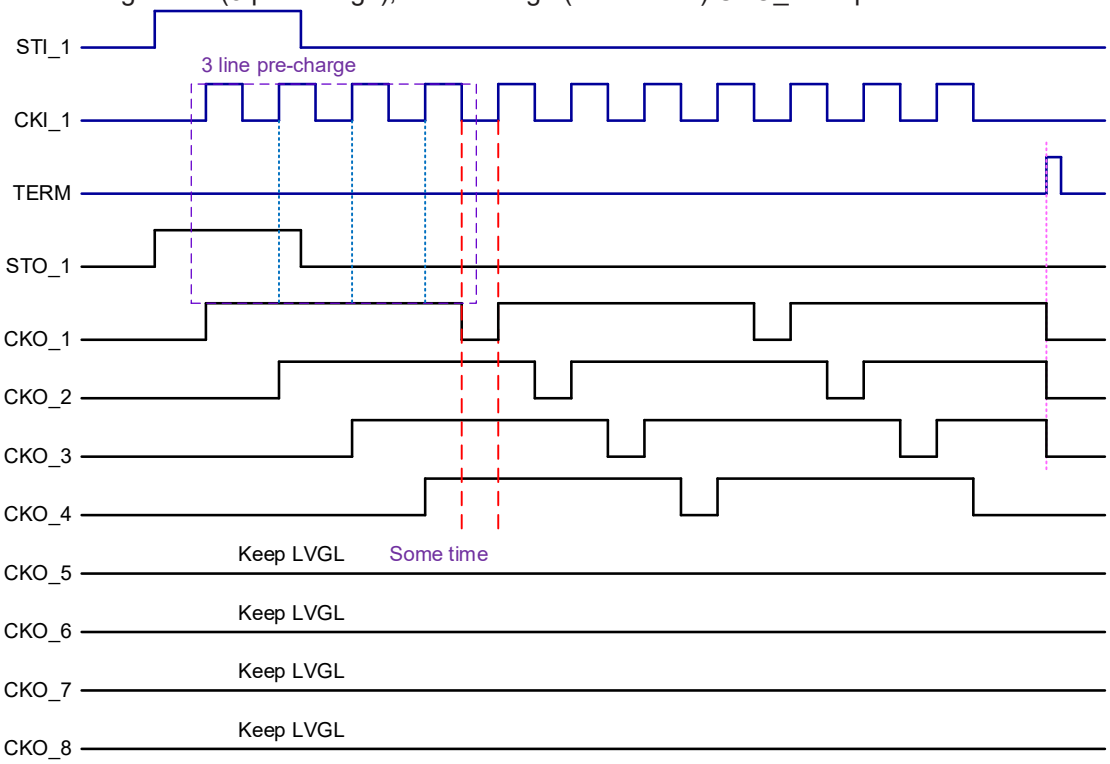
MODE1 = High level (1 pre-charge); SET2 = High (Some time) CKO_s = 4 phase



MODE1 = Low level (2 pre-charge); SET2 = High (Some time) CKO_s = 4 phase



MODE1 = Extra High level (3 pre-charge); SET2 = High (Some time) CKO_s = 4 phase



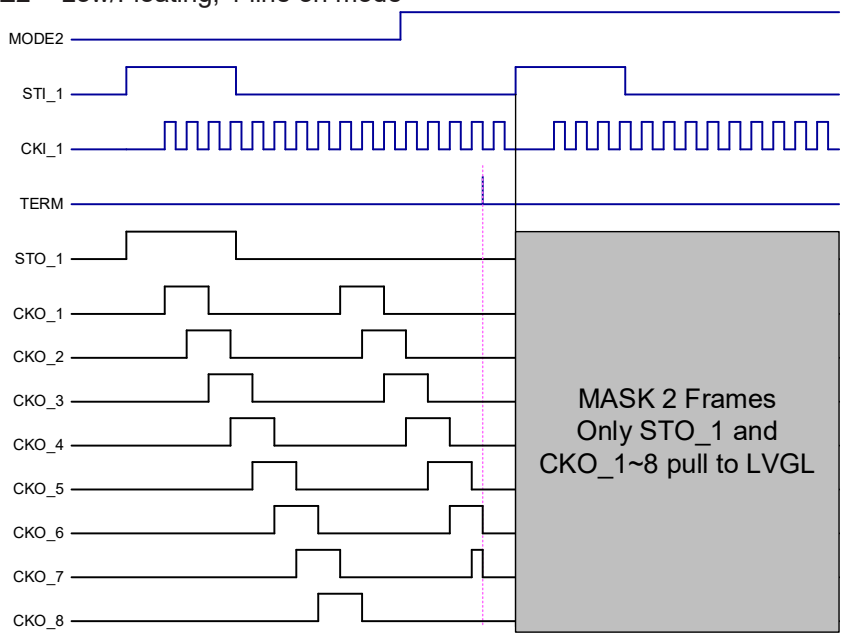
MODE2:

MODE2 is to set the CKO_s 1 line on mode output or 2 line on mode output

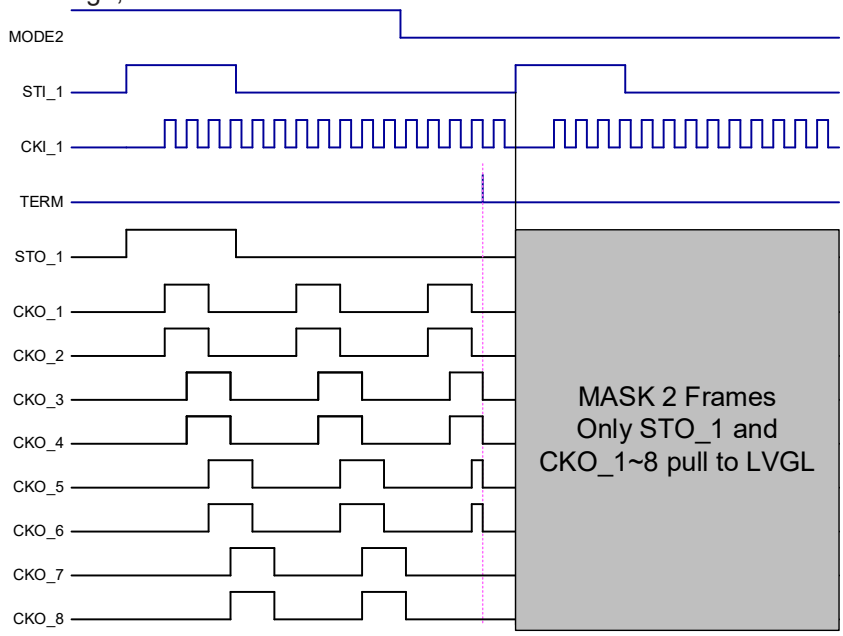
When Mode2 input signal level (L -> H or H -> L) change, the HCs will not change until next STI_1 rising edge. After that, LP6274AQVF will mask output 2 frames (only STO_1, HC1~8 pull to VGL).

PIN	Status	Level Shifter output
MODE2	High level	CKO_s is 2-line on mode. CKO_1=CKO_2, CKO_3=CKO_4 CKO_5=CKO_6, CKO_7=CKO_8
	Low/Floating	CKO_s is 1-line on mode. CKO_1~8 sequentially from CKO_1~8

MODE2 = Low/Floating; 1 line on mode



MODE2 = High; 2 line on mode

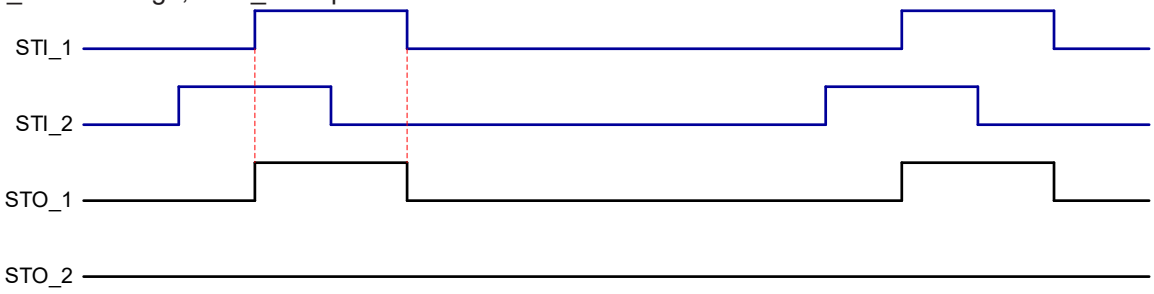


DISA_DSTO:

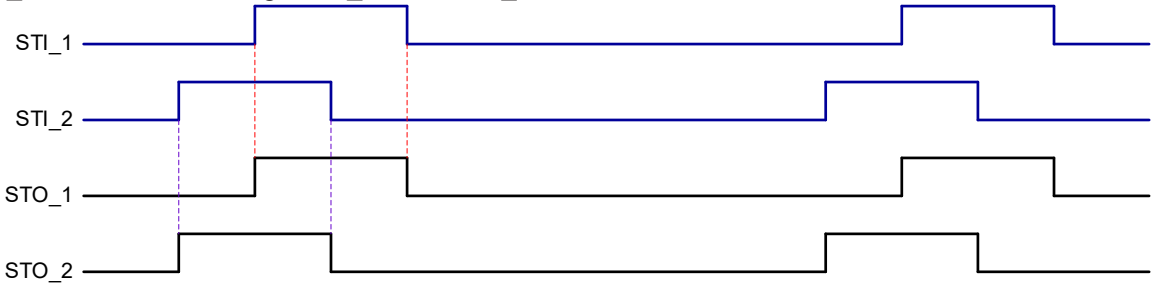
DISA_DSTO function is list below:

PIN	Status	Level Shifter output
DISA_DSTO	High level	STO_1 ON, (follow STI_1) STO_2 keep in LVGL
	Low/Floating	STO_1 ON, (follow STI_1) STO_2 ON, (follow STI_2)

DISA_DSTO = High, STO_2 keep in VGL

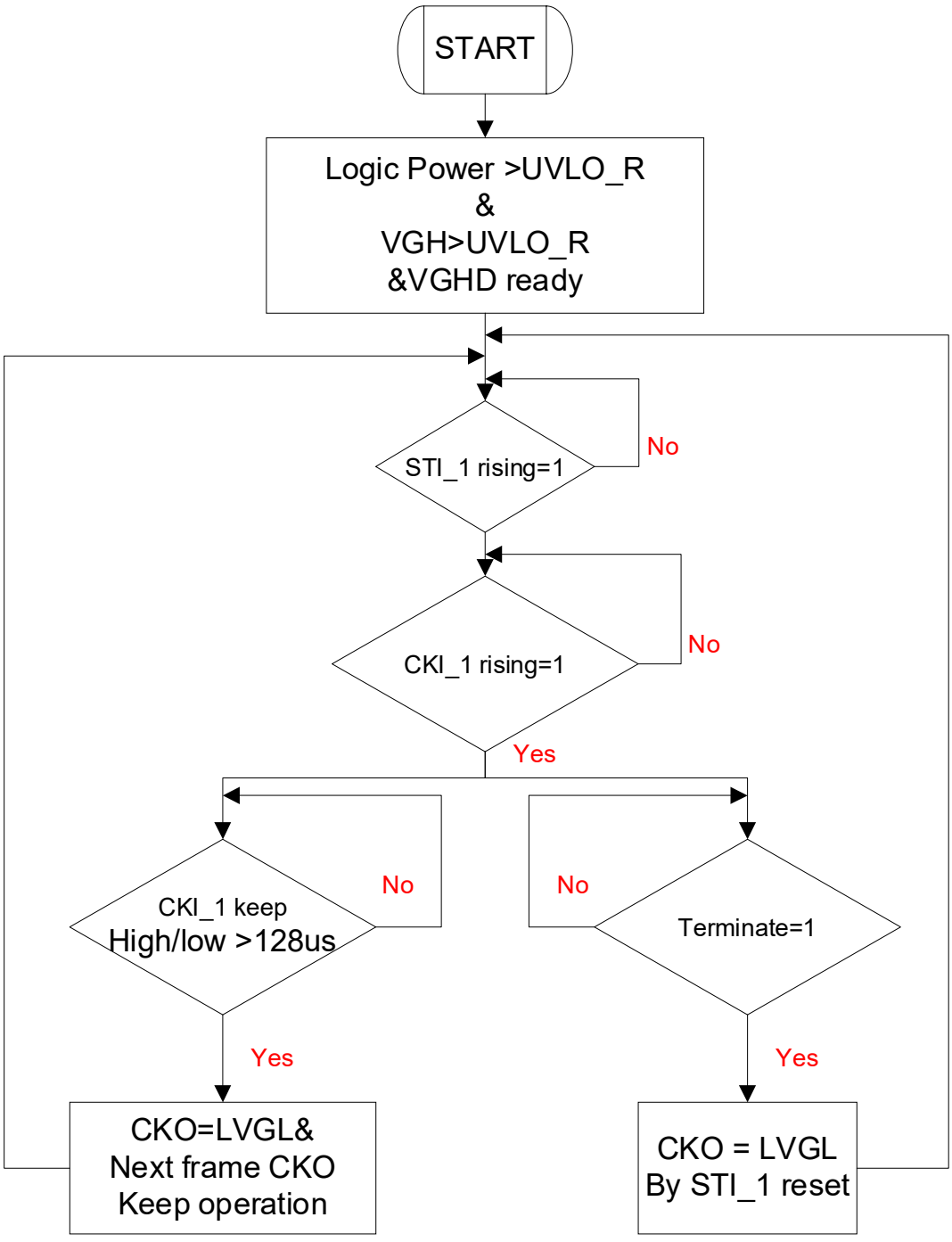


DISA_DSTO = Low/Floating, STO_2 follow STI_2



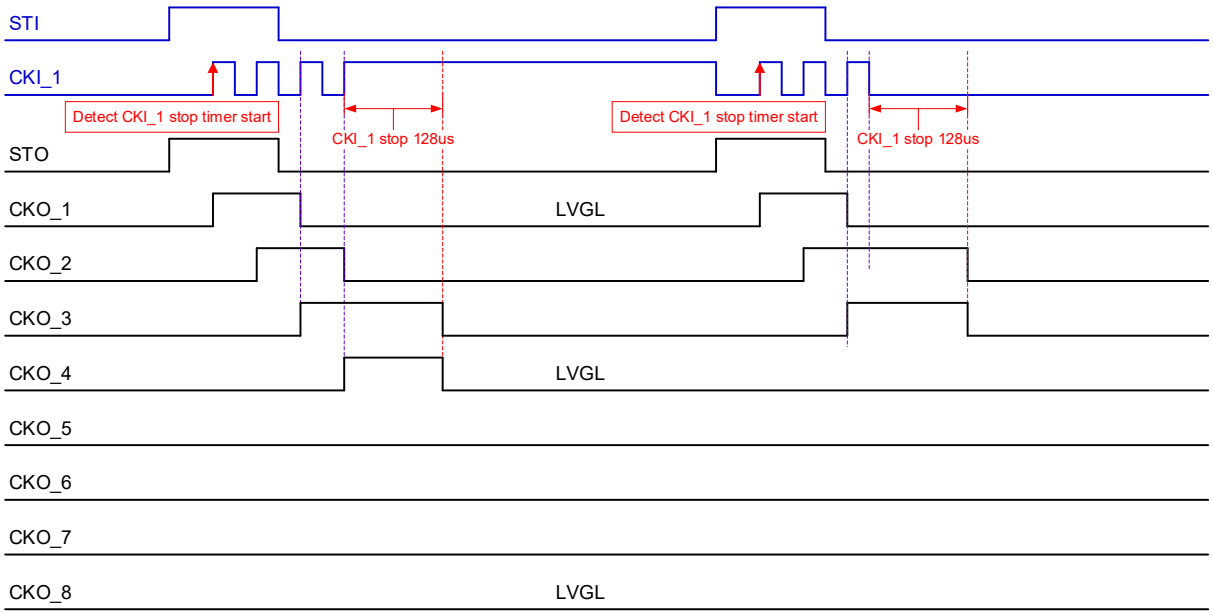
CKI_1 stop protection(CKISP)

The LP6274AQVF can generate an internal terminate signal to pull CKO_1~8 output to negative voltage. Please follow reference flow chart. The priority of CKI_1 stop protection is highest. If CKI_1 stop protection is working, then the Multi-CKI protection is stoped.

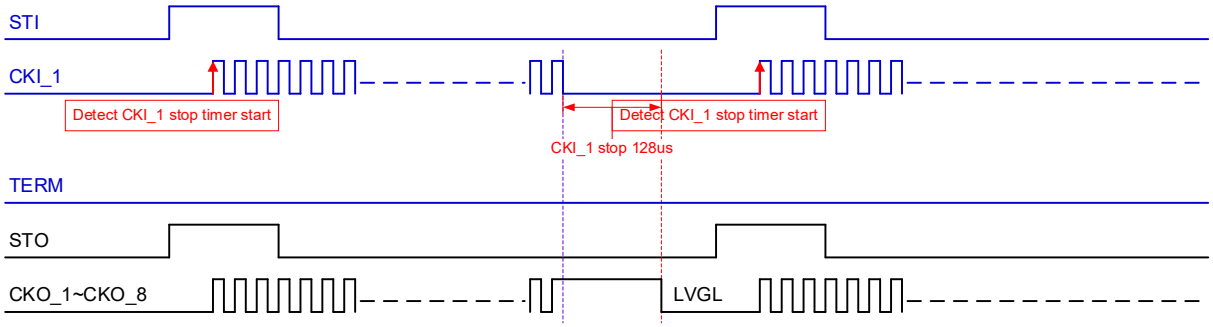


CKI_1 stop protection flow chart

Case 1: CKI_1 stop high/low (1 clock control CKO_x output)



Case 2: CKI_1 Blanking time (1 clock control CKO_x output)

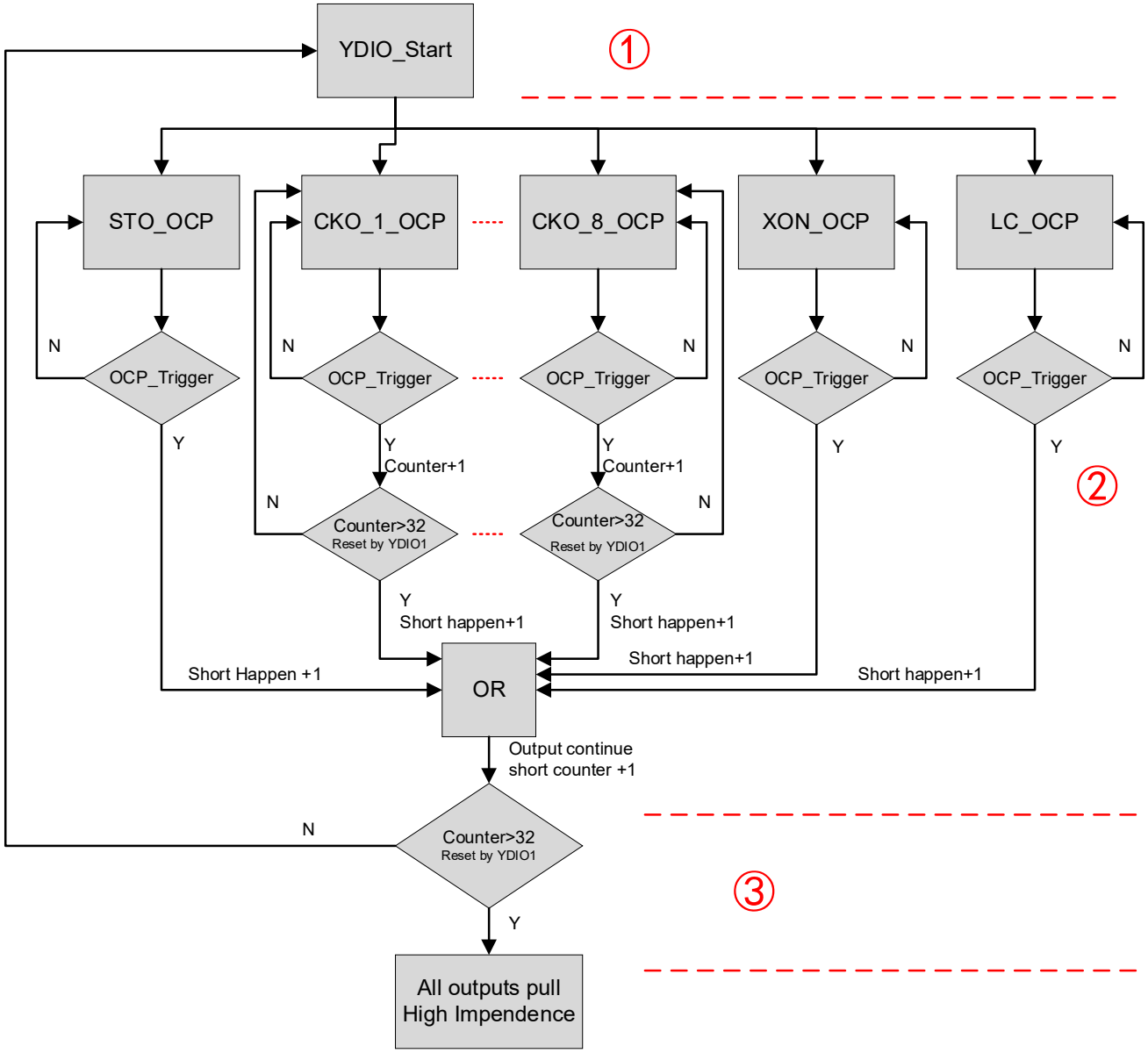


Over Current Protection (OCP)

The LP6274AQVF can detect output pins (STO_1~2, CKO_1~CKO_8, LC1~LC2, XON) short to each other short current. If the pin to pin short current over limit, the IC all outputs will pull high impendence state. After VIN_UVLO, IC recovers again. Please follow reference flow chart. If continue 32 times ST have short occur, IC will pull all outputs to high impendence state. After VIN_UVLO, IC recovers again.

OCP Fucntion is list below:

PIN	Status	Level Shifter output
OCP_EN	High	OCP Function Disable
	Floating	OCP Function Enable, Current limit = 60mA
	Low	OCP Function Enable, Current limit = 100mA

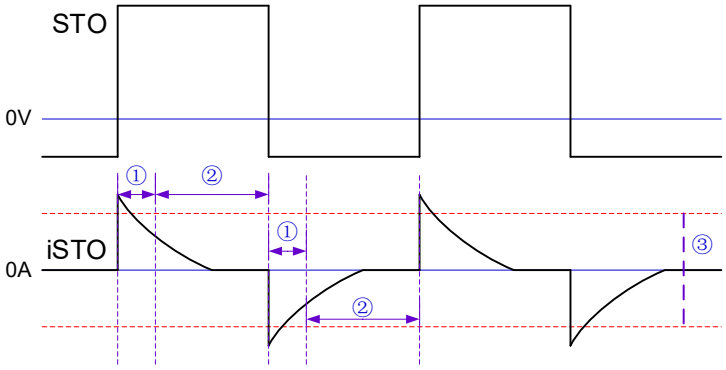


Over Current Protection flow chart

*Each CKO channel need to count OCP trigger times with itself, until counter>32 then alarm short happen+1.

STO:

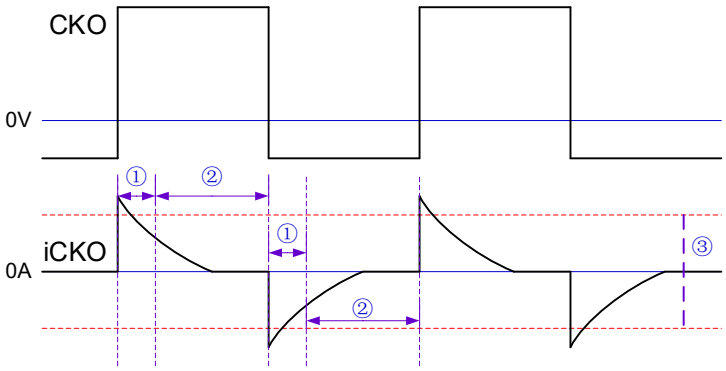
1. Blanking time: to avoid inrush current in this time period.
2. De_noise time: to detect continue over current in this time period. Only continue over current time bigger than de_noise time, and then trigger over current counter+1 per STO.
3. Detect over current level: follow OCP current level setting



STO OCP detect waveform

CKO:

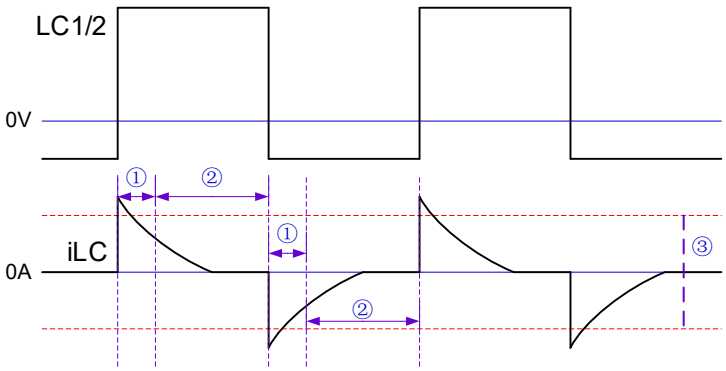
1. Blanking time: to avoid inrush current in this time period.
2. De_noise time: to detect continue over current in this time period. Only continue over current time bigger than de_noise time, and then trigger over current counter+1 per STO.
3. Detect over current level: follow OCP current level setting



CKO OCP detect waveform

LC:

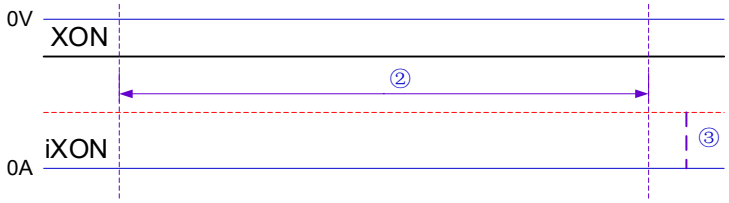
1. Blanking time: to avoid inrush current in this time period.
2. De_noise time: to detect continue over current in this time period. Only continue over current time bigger than de_noise time, and then trigger over current counter+1 per STO.
3. Detect over current level: follow OCP current level setting



LC OCP detect wavefor

XON:

2. De_noise time: to detect continue over current in this time period. Only continue over current time bigger than de_noise time, and then trigger over current counter+1 per STO.
3. Detect over current level: follow OCP current level setting



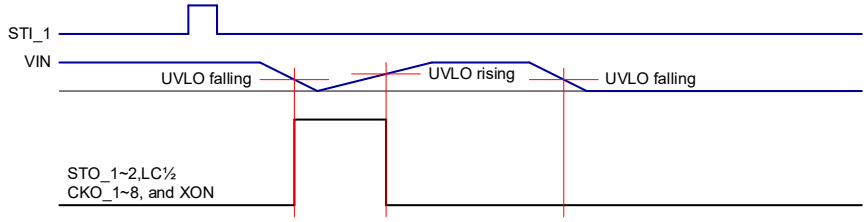
XON OCP detect waveform

Protection

Protection	Level Shifter
UVLO(Falling), VIN high to low VGH>UVLO_R	VGH
OTP, T>150℃	OFF(HI-Z)
CKI_1 Keep high/low 128us (CKI_1 protection)	All CKO pull LVGL until next CKI_1
Output over current	OFF(HI-Z)
Short current	OFF(HI-Z)

XON Function

The LP6274AQVF defines a special output timing of the level-shifter output:
Once VIN drops below UVLO falling threshold & CKI_1 exist, all the output (include XON, STO_1~2, LC1/LC2 and CKO_1~CKO_8) must be pulled high immediately and simultaneously.
When VIN is abnormal as following diagram, XON function will reset (XON is pulled to VGL, CKO_1~CKO_8 are pulled to LVGL, and STO_1~2 and LC1~2 are pulled to LVGL) no mater what voltage level VIN falls to. If VIN falls below UVLO falling in the constraint region (please refer) XON function can't be active. That is, XON, CKO_1~CKO_8, STO_1,STO_2, and LC1 or LC2 are pulled to LVGL.

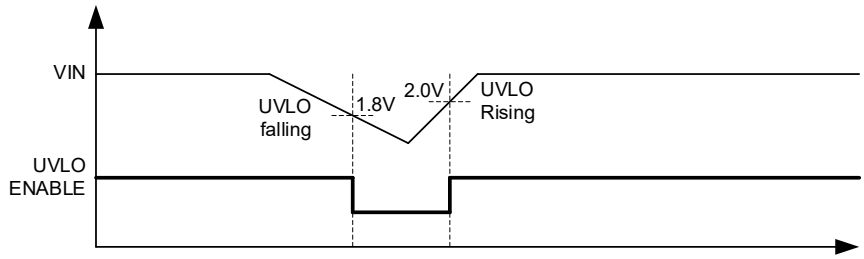


OTP Function

Overload Thermal protection (OTP) prevents excessive power dissipation from overheating the LP6274AQVF. When junction temperature exceeds 150°C, a thermal sensor triggers the OTP, all channel outputs are set to Hi-Z state. Only cycle the VIN can clear the OTP latch and reactivate the device.

Under-Voltage Lockout (UVLO)

The UVLO circuit compares the input voltage at VIN with the UVLO threshold (2V rising, 1.8V falling, typ.) to ensure the input voltages is high enough for reliable operation. The 200mV(typ.) hysteresis prevents supply transients from causing a shutdown. Once the VIN exceeds the UVLO rising threshold, start-up begins. When VIN falls below the UVLO falling threshold, the controller turns off all of IC internal function.



The Setting Table

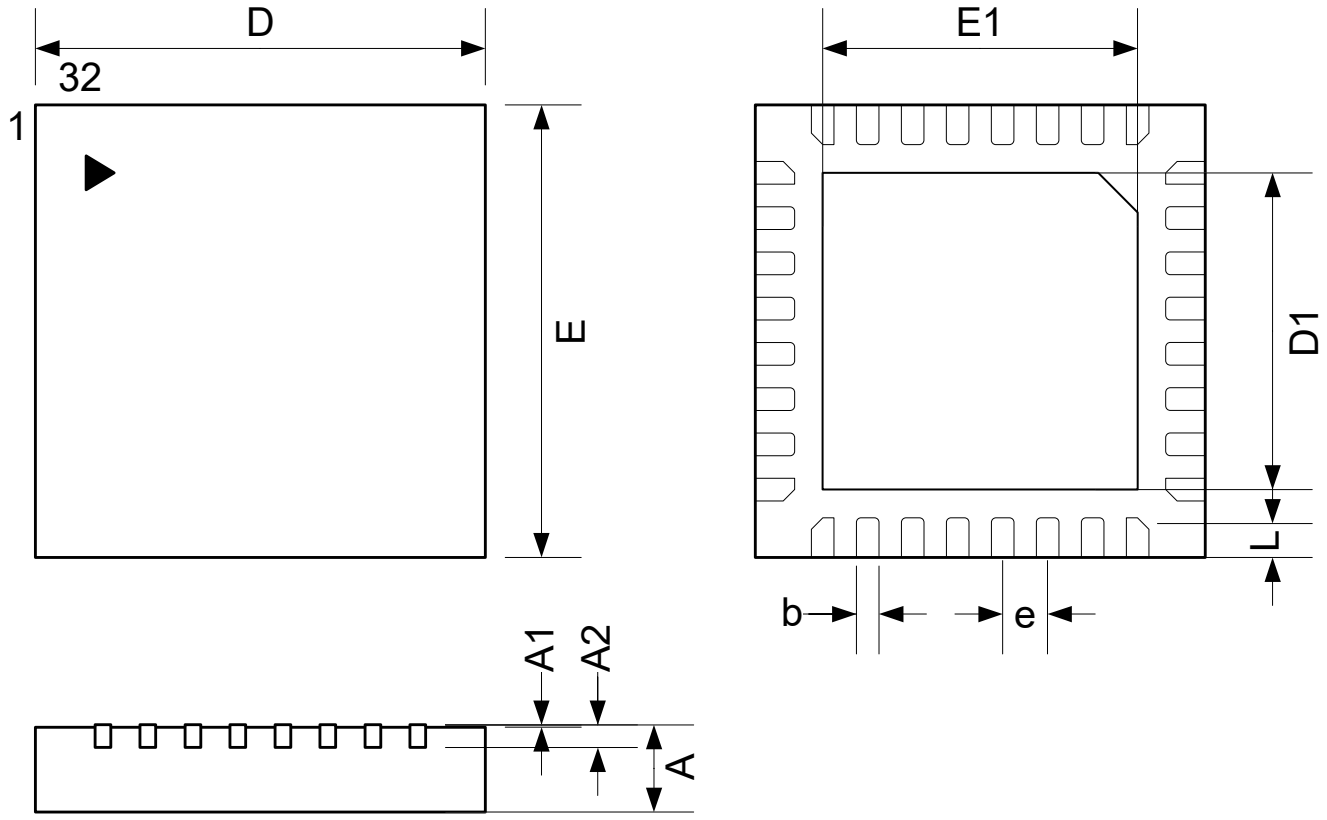
PIN	Status	Voltage Level	Level Shifter output
SET1 (*1)	High Level	2.5V~3.6V	8 phase CKO outputs
	Floating	1.2V~2.2V	4 phase CKO outputs, CKO_5~CKO_8 keep in LVGL
	Low Level	0V ~ 0.8V	6 phase CKO outputs, CKO_7, CKO_8 keep in LVGL
SET2 (*2)	High Level	1.5V~3.6V	There is some time interval between CKO_s
	Low Level/Floating	0V~0.8V	There is no time interval between CKO_s
MODE1 (*2)	Extra High Level	3.0V~4.0V	3-line pre-charge
	High Level	1.5V~2.5V	1-line pre-charge
	Middle Level	0.9V~1.4V	No pre-charge
	Low Level	0V~0.8V	2-pine pre-charge
MODE2 (*2)	High Level	1.5V~3.6V	2-line mode on
	Low Level/Floating	0V~0.8V	1-line mode on
DISA_DSTO (*2)	High Level	1.5V~3.6V	STO_1 On (follow STI_1), STO_2 keep in LVGL
	Low Level/Floating	0V~0.8V	STO_1 On (follow STI_1), STO_2 On (follow STI_2)
OCP_EN (*1)	High Level	2.5V~3.6V	OCP Function Disable
	Floating	1.2V~2.2V	OCP Function Enable, current limit level2
	Low Level	0V ~ 0.8V	OCP Function Enable, current limit level1

* 1 For a tri-state setting pin, it is connected 400KΩ resistor to VIN and 400KΩ to AGND inside.

* 2 It is connected 400KΩ resistor to AGND inside.

Packaging Information

QFN4X4-32



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.60	2.65	2.70	0.1023	0.1043	0.1063
E1	2.60	2.65	2.70	0.1023	0.1043	0.1063
b	0.15	0.20	0.25	0.0059	0.0079	0.098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.35	0.40	0.0118	0.0138	0.0157