LP4121

2-Cell Boost Switching Charger

Features

- Easy-to-use standalone 2-cell synchronous Boost switching charger
  - Proprietary charge current control
  - 4.5V to 6.2V input voltage operation
  - 20V absolute maximum input voltage rating
  - Charge voltages: 8.2V/8.3V/8.4V/8.6V/8.7V
  - 0.35A- 2.0A maximum fast charge current
  - 1.3MHz switching frequency
  - 1μH inductor for low DCR loss and small footprint
  - 93% charge efficiency at 1A charge
  - Support Precharge, Constant Current (CC) charge, Constant Voltage (CV) charge, charge termination and recharge
  - Battery short circuit protection
  - Resistor programmable charge voltage
  - Resistor programmable charge current
- High charge accuracy
  - +/- 0.75% charge voltage regulation
  - +/- 7.5% switching charge current regulation
- Protections
  - Cycle-by-cycle current limit protection
  - Input voltage regulation (VINDPM)
  - Battery short protection
  - Cold/hot battery temperature monitoring (For LP4121QVF only)
  - Junction temperature thermal regulation (TREG)
- Packaging
  - DFN3x3-10L or ESOP-8L
  - RoHS compliant and halogen free
  - 100% lead (Pb) free

Applications

- 2-cell battery charger
- BT speaker
- Portable printers
- Toys

General Description

The LP4121 is a standalone Boost switching battery charger to charge 2-cellbatteries at up to 2A charge current. The 2-cell switching battery charger operates at 1.3MHz switching frequency to allow a small size of 1μH inductor with low DCR loss.

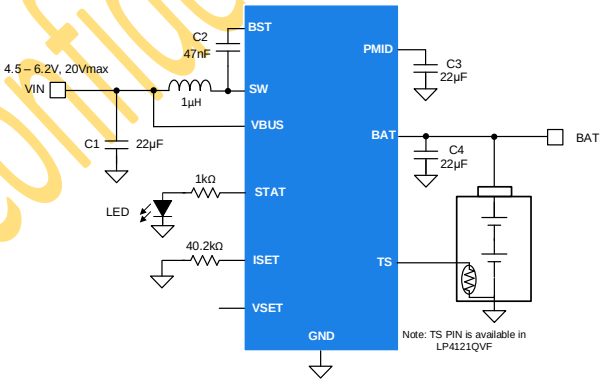
The LP4121 is available in DFN3x3-10L package and ESOP-8L package.

Order Information

LP4121 □□ □

F: Pb-Free
Package Type
QV: DFN -10
SP: ESOP-8

Application Circuit

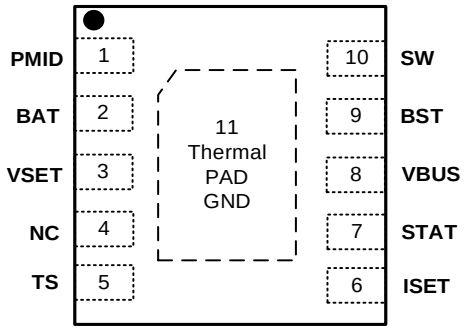


(BOM are shown in Figure 11)

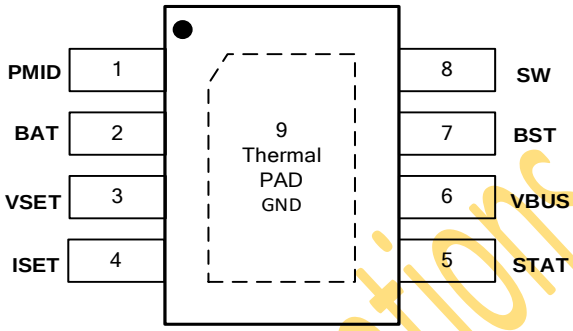
Device Information

Part Number	Temperature Sensing	Top Marking	Package	Moisture Sensitivity Level	Shipping
LP4121QVF	Yes	LPS LP4121 YWX	DFN3x3-10L	MSL3	5K/REEL
LP4121SPF	No	LPS LP4121 YWX	ESOP-8L	MSL3	4K/REEL

Pin Diagram



DFN 3x3 - 10L
(Top View)
LP4121QVF



ESOP-8L
(Top View)
LP4121SPF

Pin Description

Pin Name	LP4121 QVF	LP4121 SPF	Description
PMID	1	1	Boost output. Connect to a Boost output capacitor.
BAT	2	2	Charge output. Connected to a battery.
VSET	3	3	Charge voltage program input.
NC	4	N/A	No connection.
TS	5	N/A	Battery temperature sense thermistor input. Support 10kΩ thermistor with programmable charge temperature range. Charge is suspended if the battery thermistor temperature is out of range. If TS pin function is not used, short this pin to ground. If leave this pin floating, the charge termination is disabled and the Boost charger can be used as a Boost converter with BAT output regulated at V_{BATREG} with constant current limit and short circuit protection.
ISET	6	4	Fast charge current program input. Connect a 1% resistor RISET from this pin to ground to program the charge current. If ISET pin is floating, charge current is near zero, If ISET pin is pulled below 0.35V, charge is disabled. The fast charge current can be set as: ICHG=40/RISET(kΩ) (A)
STAT	7	5	Charge status indication output. Connect a LED from STAT pin to GND via a current limiting resistor. STAT pin is internally connected to a 5V voltage source. The STAT pin indicates charger status: • Charge in progress: STAT pin is internally pulled HIGH. • Charge complete or not in charge: STAT pin is internally OPEN.
VBUS	8	6	Input voltage.
BST	9	7	Bootstrap input. Connect a 47nF capacitor from SW to BST pin.
SW	10	8	Switching node. Connect to input inductor terminal.
GND &Thermal PAD	11	9	Ground and thermal pad. Connected to GND internally.

Absolute Maximum Ratings (Note)

VBUS, PMID, SW, BAT Voltage to GND ---------- -0.3V to 20V
BST to SW Voltage ---------- -0.3V to 6V
VSET, ISET, TS, STAT Voltages to GND ---------- -0.3V to 6V
STAT Source Current ---------- 6mA
Maximum Junction Temperature (Tj) ---------- 150℃
Storage Temperature Range ---------- -40℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance, DFN3x3-10L) ---------- 48℃/W
θ_{JA} (Junction-to-Ambient Thermal Resistance, SOP-8E) ---------- 45℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	4.5		6.2	V
I_{CHG}	Fast Charge Current (1)	0.35		2.0	A
V_{BATREG}	Battery Charge Voltage	8.2		8.7	V
T_J	Operating Junction Temperature Range (T_J)	-40		125	℃
T_A	Ambient Temperature Range	-40		85	℃

Notes:

(1) The maximum charge current may be limited by the capacity of input power supply and thermal dissipation environment.

Recommended Component Parameter Range(1)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
C_{VBUS}	Input Capacitance at VBUS	6	22	60	μF
C_{PMID}	PMID Capacitance	6	22	60	μF
C_{BAT}	BAT Capacitance	6	22	60	μF
L	Boost Inductance	0.7	1.0	2.65	μH

Notes:

(1) The values recommended in the table are effective inductance and capacitance.

Electrical Characteristics

(The specifications are at V_{BUS}=5V, V_{BAT}=7.6V, T_J = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
I_{Q_BAT}	Battery reverse current	No VBUS VBAT= 9V			2	μA
I_{Q_BAT}	Battery leak current at termination	Charge is terminated V_{BAT}= V_{BATREG}			20	μA
I_{Q_BAT}	Battery leak current	TS is pulled to GND			15	μA
I_{VBUS}	Input current	BAT pin open, Boost switching		2		mA
INPUT VOLTAGE AND CURRENT						
V_{UVLO_RISE}	Under voltage lock out (UVLO) voltage	V_{VBUS} rising	3.8	4.0	4.2	V
V_{UVLO_FALL}	UVLO voltage	V_{VBUS} falling		400		mV
V_{INDPM}	VINDPM at VBUS	Regulated at VBUS pin	4.2	4.35	4.5	V
V_{VBUS_OVP}	VBUS over voltage protection	V_{VBUS} rising	7.0	7.5	8.0	V
V_{VBUS_OVP}	VBUS over voltage protection hysteresis	Option 1 V_{VBUS} falling		380		mV
CHARGE CURRENT SETTING ISET						
V_{ISET}	ISET pin voltage			1		V
I_{CHG}	Charge current setting range		0.35		2.0	A
K_{ICHG}	Charge current ratio	I_{CHG}=1A		40		A x kΩ
V_{ISET_LOW}	ISET voltage low		0.33	0.35	0.37	V

Electrical Characteristics

(The specifications are at V_{VBUS}=5V, V_{BAT}=7.6V, T_J = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BOOST CONVERTER AND PMID REGULATION						
f_{SW1}	Switching frequency		1180	1300	1420	kHz
I_{LSFET_OCP}	LSFET over current protection (OCP)			6.5		A
T_{ON_MIN}	Minimum on-time			100		ns
Dmax	Maximum duty cycle			92.5		%
MOSFETs						
R_{DSON_Q2}	Boost high-side FET on-resistance	V_{VBUS}=5V		40		mΩ
R_{DSON_Q1}	Boost low-side FET on-resistance	V_{VBUS}=5V		40		mΩ
R_{DSON_Q3}	Battery FET on-resistance			35		mΩ
COLD/HOT THERMISTOR COMPARATOR						
I_{TS_SOURCE}	TS pin pull-up current		95	100	105	uA
V_{TS_FLT}	TS floating detect	V_{VBUS}=5V No termination		4.5		V
V_{TS_GND}	TS ground detect	V_{VBUS}=5V TS function not in use	0.13	0.15	0.17	V
$V_{T1\_HOT\_F}$	TS hot threshold	V_{TS} falling	485	500	515	mV
$V_{T1\_HOT\_R}$	TS hot threshold	V_{TS} rising	535	550	565	mV
$V_{T3\_COLD\_R}$	TS cold threshold	V_{TS} rising	2450	2500	2550	mV
$V_{T3\_COLD\_F}$	TS cold threshold	V_{TS} falling	2200	2250	2285	mV

Electrical Characteristics

(The specifications are at V_{VBUS}=5V, V_{BAT}=7.6V, T_J = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER						
V_{BATREG}	Charge voltages	RVSET = Open	8.358	8.4	8.442	V
		RVSET =240kΩ	8.557	8.6	8.643	V
		RVSET = 120kΩ	8.259	8.3	8.341	V
		RVSET = 68kΩ	8.159	8.2	8.241	V
		RVSET = 1kΩ	8.657	8.7	8.743	V
$V_{BAT\_LOWV\_RISE}$	V_{BAT} fast charge rising threshold	Precharge to fast charge	5.7	5.8	5.9	V
$V_{BAT\_LOWV\_FALL}$	V_{BAT} fast charge falling threshold	Fast charge to precharge		5.4		V
$V_{BATSHORT\_RISE}$	V_{BAT} precharge rising threshold	BAT short to precharge	3.8	4	4.2	V
$V_{BATSHORT\_FALL}$	V_{BAT} precharge falling threshold	BAT precharge to BAT short	3.4	3.6	3.8	V
V_{PMID_REF}	PMID voltage	PMID regulation voltage in linear mode, V_{VBUS}=5V	5.7	5.9	6.1	V
I_{CHG_CC}	Fast charge current	I_{CHG}=1.5A, V_{BAT}=7.6V	1425	1500	1575	mA
		I_{CHG}=1A, V_{BAT}=7.6V	950	1000	1050	mA
		I_{CHG}=0.5A, V_{BAT}=7.6V	450	500	550	mA
I_{PRECHG}	Precharge current	V_{PMID}=5.95V, VBAT=5V		125		mA
$I_{BATSHORT}$	Battery short current	V_{PMID}=5.95V, VBAT=2V		90		mA
I_{TERM}	Termination current		150	180	210	mA
V_{RECHG_HYS}	Recharge hysteresis	V_{BAT} falling from V_{BATREG}	200	250	300	mV
STAT						
V_{STAT}	STAT pull-up voltage	STAT internally pulled up to V_{STAT} V_{BUS}=5V, I_{STAT}=0	4.9		5	V
V_{STAT}	STAT pull-up voltage	STAT internally pulled up to V_{STAT} V_{BUS}=5V, I_{STAT}= 6mA	4.6	4.7	4.8	V
I_{SAT_SOURCE}	STAT source current capability		6			mA
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Thermal regulation temperature		112	120	128	°C
T_{SHUT_RISE}	Thermal shut down in all conditions	Temperature rising	140	150	160	°C
T_{SHUT_HYST}	Thermal shut down in all conditions	Temperature falling		30		°C

Typical Characteristics

(L=1μH, C1, C3, C4 =22μF, C2= 47nF and T_J = 25°C unless otherwise noted; The schematic is as shown in Figure 11)

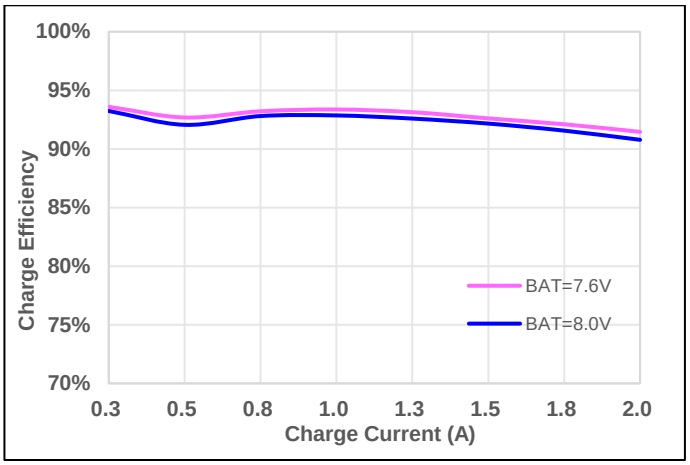


Figure 1. Charge Efficiency vs. Charge Current (VBUS=5V)

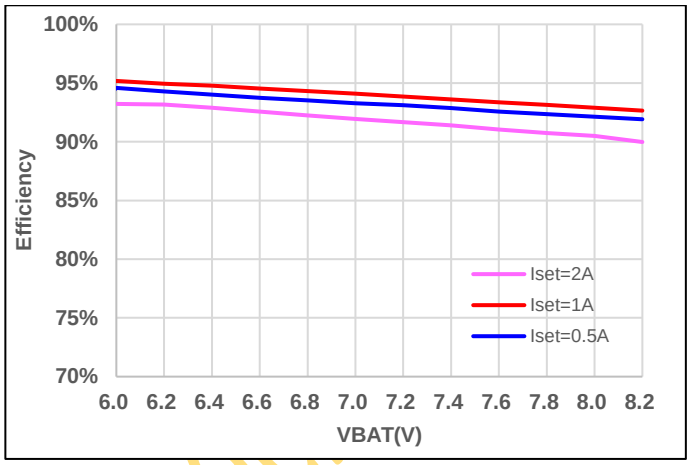


Figure 2. Charge Efficiency vs. Battery Voltage (VBUS=5V, ISET=2A/1A/0.5A)

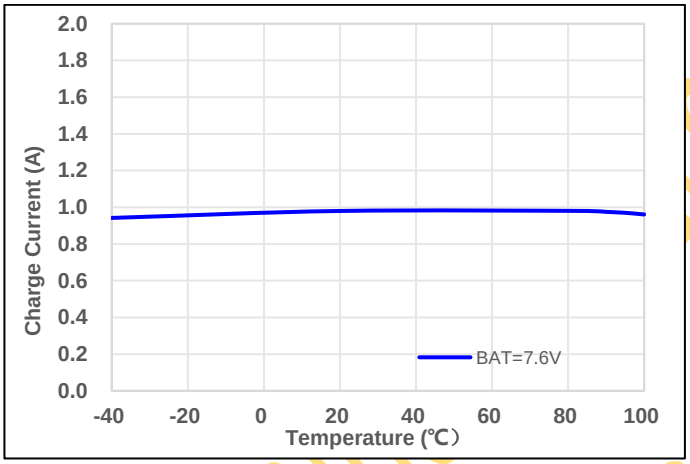


Figure 3. Battery Charge Current vs. Junction Temperature (VBUS=5V, VBAT=7.6V, ISET=1A)

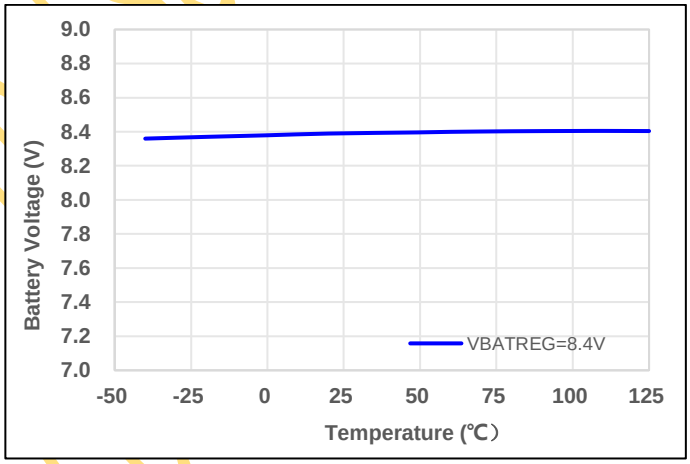


Figure 4. Battery Regulation Voltage vs. Junction Temperature (VBATREG=8.4V, VBUS=5V, ISET=1A, Temperature = -40 to 100°C)

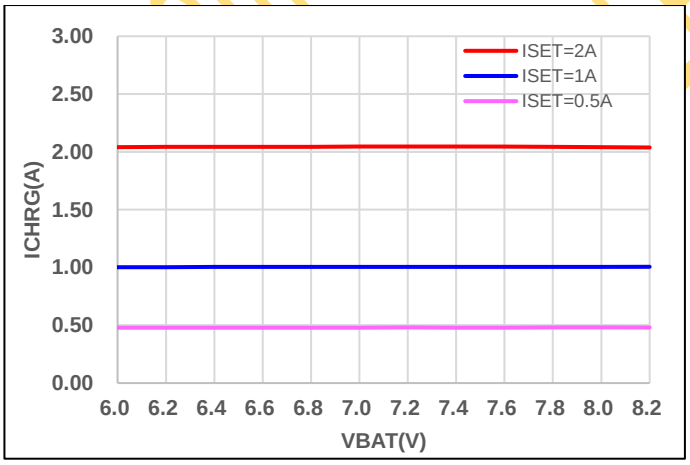


Figure 5. Charge current vs. Battery Voltage (VBUS=5V, ISET=0.5A/1A/2A)

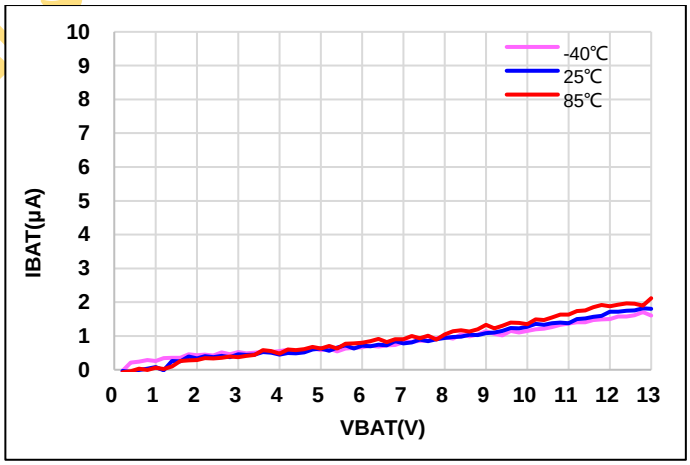


Figure 6. Battery leakage current vs. Battery Voltage (No VBUS, Temperature = -40/25/85°C)

Typical Characteristics

(L=1μH, C1, C3, C4 =22μF, C2= 47nF and T_J = 25°C unless otherwise noted; The schematic is as shown in Figure 11)

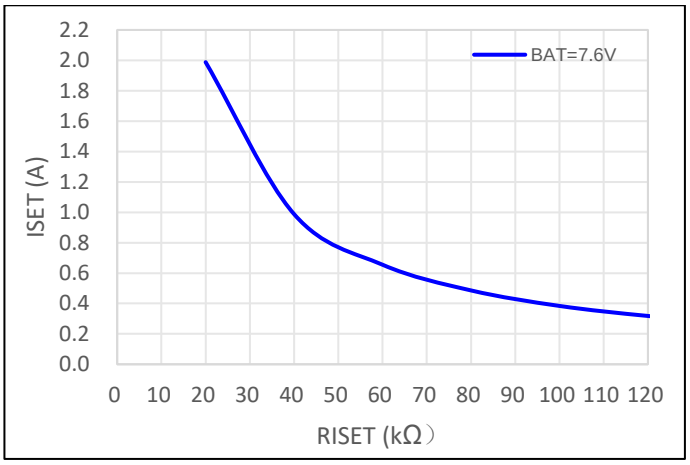


Figure 7. Charge Current vs. Charge Current Setting Resistance (VBUS=5V, VBAT=7.6V)

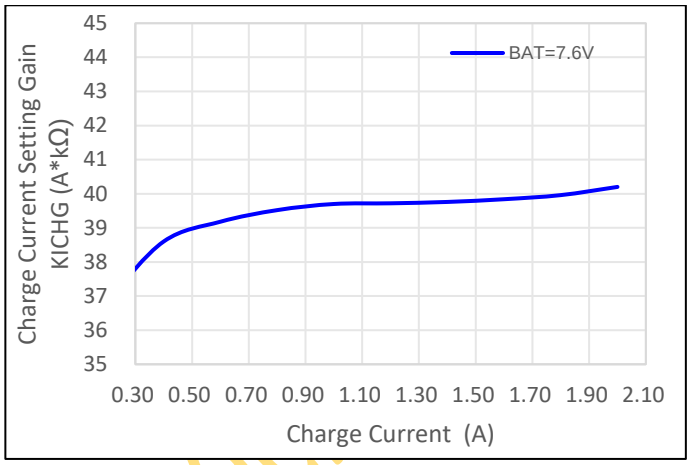
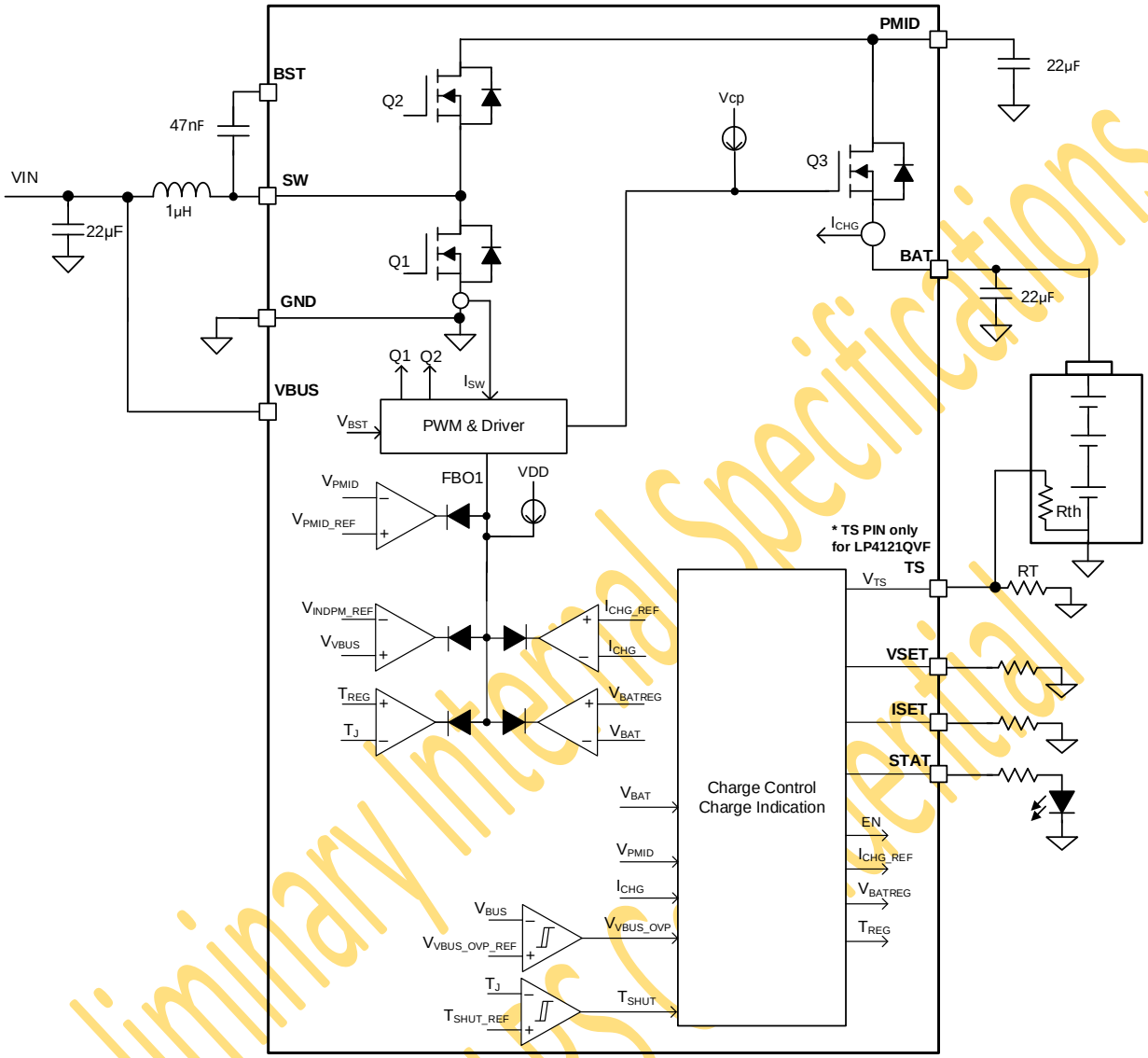


Figure 8. Charge Current Setting Gain KICHG vs. Charge Current (VBUS=5V, VBAT=7.6V)

Functional Block Diagram



Detailed Description

Overview

The LP4121 is a standalone Boost charger for 2-cell batteries. The charge current is resistor programmable up to 2A. The charge voltage is programmable with a resistor connected to VSET pin and GND.

Device Power-up

With VBUS voltage V_{VBUS} rising above V_{UVLO_RISE}, Boost starts up with PMID voltage regulated V_{VBUS} + 0.9V. After the Boost soft startup is complete, BATFET is enabled with soft-start to avoid inrush current through Q3.

Device Functional Mode

The device operates in different modes depending on V_{VBUS} and V_{BAT}. The functional modes are listed in the following table.

Table 1: Device Functional Mode

MODE	CONDITIONS	CHARGE	STAT
HiZ Mode	V_{VBUS} <V_{UVLO}	NO	OPEN
VINDPM Mode	V_{VBUS} =V_{INDPM}	YES	HIGH
BATFET Q3 Linear Mode	(V_{PMID}– V_{BAT}) > I_{CHG} *R_{dson_Q3} (R_{dson_Q3} is the on-resistance of Q3)	YES	HIGH
BATFET Q3 Switch Mode	(V_{PMID}– V_{BAT}) = I_{CHG} *R_{dson_Q3} (R_{dson_Q3} is the on-resistance of Q3)	YES	HIGH
CC/CV Charge Mode	V_{BAT}> V_{BAT_LOWV}	YES	HIGH
Precharge Mode	V_{BAT_SHORT}<V_{BAT}< V_{BAT_LOWV}	YES	HIGH
Battery Short Mode	V_{BAT}< V_{BAT_SHORT}	YES	HIGH
Fault Mode	Input OVP or TS cold/hot or T_{SHUT} is triggered	NO	OPEN
Charge Termination	Charge is terminated if V_{VBUS} >V_{UVLO} and I_{CHG}<I_{TERM} and V_{BAT} >V_{BATREG} - V_{RECHG_HYS}	NO	OPEN

Battery Charge Profile

Typical charge cycles are shown in Figure 9. The battery charge current is determined by input voltage, battery voltage and charge current setting. The battery charge voltage can be set by a resistor value at VSET pin and charge current is set by a resistor value at ISET pin in fast charge mode.

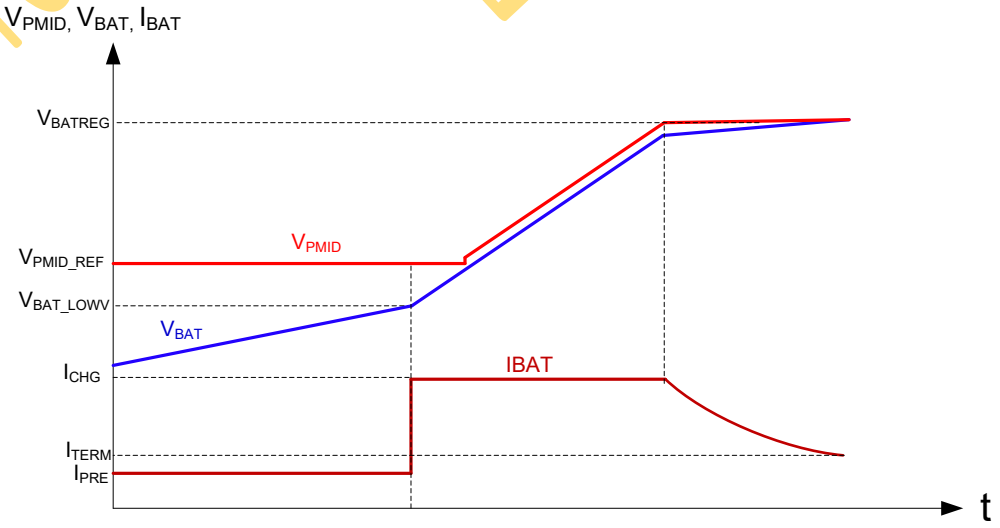


Figure 9.Typical battery charge cycle for battery charging

Battery Short

The device charges the battery at $I_{BATSHORT}$ if a battery voltage is below V_{BAT_SHORT} in battery short mode.

Precharge

The device charges the battery at I_{PRECHG} in precharge mode if a battery voltage is below V_{BAT_LOWV}.

Constant Current (CC) Charge

CC charge is also called fast charge. The device charges the battery from Boost converter at current level of K_{ICHG} / R_{ISET}, where K_{ICHG} is the gain of charge current setting. The device charges the battery at 100% of programmed fast charge current I_{CHG_CC} in fast charge mode if a battery voltage is above V_{BAT_LOWV}.

Constant Voltage (CV) Charge

With the battery voltage being charged up, the BAT pin voltage reaches the battery regulation voltage V_{BATREG} and the charge current starts to decrease from fast charge current I_{CHG_CC}. The actual battery voltage keeps increasing until charge is terminated.

Charge Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold (V_{BATREG} – V_{RECHG_HYS}) and the charge current decrease below termination current I_{TERM} for deglitch time t_{TERM}. The termination current threshold I_{TERM} is fixed at I_{TERM}. After charge is terminated, Boost converter turns off with V_{BAT} and TS pin being continuously monitored.

Battery Recharge

Once a charge cycle is terminated, if battery voltage V_{BAT} decreases below the recharge threshold (V_{BATREG} – V_{RECHG_HYS}) and the charge conditions are met, the charger is enabled again. In addition to recharge, charge cycle starts if V_{VBUS} voltage is recycled or fault conditions are cleared even with the battery voltage above the recharge threshold.

Battery Temperature Monitoring (Only for LP4121QVF)

The charger device provides a single NTC thermistor input TS pin for battery temperature monitor. TS pin has internal pull-up current 100uA and TS voltage is internally clamped. If TS pin is open or pulled higher than 4.5V, charge termination is disabled. If TS pin is pulled to ground, TS pin is ignored and battery is charged without TS detection

The device continuously monitors battery temperature by sensing the voltage at TS pin. The cold temperature is corresponding to the voltage threshold of V_{T3_COLD} and the hot temperature is corresponding to the voltage threshold of V_{T1_HOT}.If the TS voltage V_{TS} falls betweenV_{T1_HOT} and V_{T3_COLD}, the device charges battery normally. If the TS voltage V_{TS} falls out of the range and the TS pin is not shorted to GND or left open, the device stops charge.

As shown in Figure 10, to monitor the battery temperature, a negative temperature coefficient (NTC) thermistor is connected to TS pin through R_{T1} and R_{T2} resistors. The R_{T1} and R_{T2} resistors are used to adjust cold and hot temperatures.

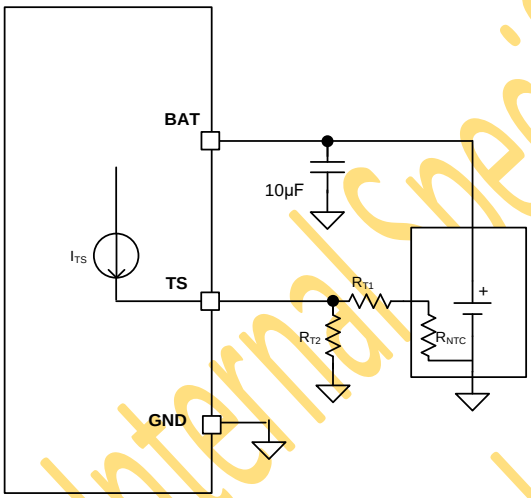


Figure 10. Battery Temperature Monitoring

The RT1 and RT2 resistance can be calculated based on NTC specifications and charge temperature range. The design steps are as shown below:

1. Convert the cold voltage threshold $V_{T3\_COLD\_R}$ to a corresponded resistor value using the equation below:
   $$R_{COLD} = \frac{V_{T3\_COLD\_R}}{I_{TS\_SOURCE}} = \frac{2500mV}{100\mu A} = 25k\Omega$$
   Convert the hot voltage threshold $V_{T1\_HOT\_F}$ to a corresponded resistor value using the equation below:
   $$R_{HOT} = \frac{V_{T1\_HOT\_F}}{I_{TS\_SOURCE}} = \frac{500mV}{100\mu A} = 5k\Omega$$
2. According to the required battery operation temperature range, for example 0℃ to 45℃, look up the NTC thermistor resistor values. For a 10kΩ (B=3435K) NTC thermistor, the resistance values at 0℃ is $R_{NTC_{COLD}} = 27.28k\Omega$and the resistance value at45℃ is$R_{NTC_{HOT}} = 4.911k\Omega$
3. The R_{T1}, R_{T2} can be calculated by the equations:
   $$R_{T1}(k\Omega) = \frac{-(R_{NTC_{COLD}}+R_{NTC_{HOT}})+\sqrt{(R_{NTC_{COLD}}+R_{NTC_{HOT}})^2-4\times(R_{NTC_{COLD}}\times R_{NTC_{HOT}}+\frac{(R_{NTC_{COLD}}-R_{NTC_{HOT}})\times R_{COLD}\times R_{HOT}}{R_{HOT}-R_{COLD}})}}{2} \quad (1)$$
   $$R_{T2}(k\Omega) = \frac{R_{NTC_{HOT}}\times R_{HOT}+R_{T1}\times R_{HOT}}{R_{NTC_{HOT}}+R_{T1}-R_{HOT}} \quad (2)$$

The resistor network values can be calculated:

R_{T1}= 0.180kΩ, R_{T2} = 279.04kΩ

Select 1% accuracy resistors R_{T1}= 0.182kΩ, R_{T2} = 280kΩ

Input Voltage Dynamic Power Management (VINDPM)

When the input current of the device exceeds the current capability of the power supply, the charger device regulates VBUS voltage by reducing charge current to avoid crashing the input power supply.

ISET Pin

A resistor connected at ISET pin programs fast charge current as $I_{CHG\_CC}(A) = 40 / R_{ISET}$ (kΩ). If ISET pin is open, the device is operating but the charge current is minimized. If ISET pin is shorted to GND (V_{ISET}<0.35V), the device is disabled.

VSET Pin

A resistor connected at VSET pin programs charge voltages.

- R_{VSET} = 1kΩ or short, V_{BATREG}=8.7V
- R_{VSET} = 68kΩ, V_{BATREG}=8.2V
- R_{VSET} = 120kΩ, V_{BATREG}=8.3V
- R_{VSET} = 240kΩ, V_{BATREG}=8.6V
- R_{VSET} = open, V_{BATREG}=8.4V

Thermal Regulation (TREG)

The device monitors the junction temperature T_J to avoid overheating the chip and limit the device surface temperature. When the internal junction temperature exceeds thermal regulation limit T_{REG}, the charger current is reduced.

During thermal regulation, the average charging current is below the programmed battery charging current. In thermal regulation, termination is temporarily disabled.

Thermal Shutdown (TSHUT)

The devices have thermal shutdown built in to turn off the charger when device junction temperature exceeds T_{SHUT}. The charger is re-enabled with soft-start when the junction temperature is 30°C below T_{SHUT}.

Application and Implementation

Application Information

The device can be used for general purpose high-efficiency fast charge for 2-cell Li-on batteries. The charge current is programmable by a resistor from ISET pin to GND. The charge voltage is programmable by a resistor from VSET pin to GND. The charger can be enabled or disabled by a MCU GPIO with open-drain structure connected to ISET pin or TS pin.

Application Schematic

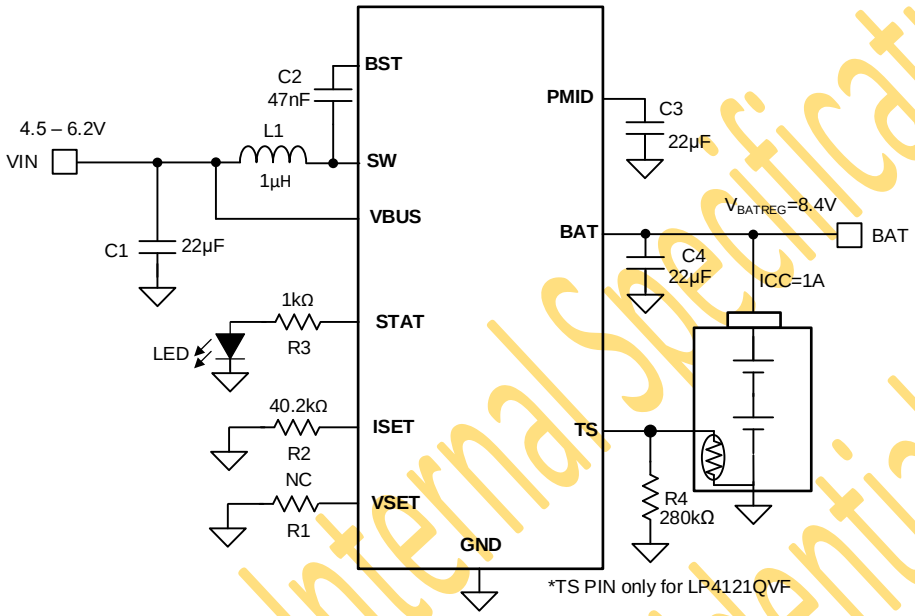


Figure 11: Typical Applications Schematic

Designator	Values	Part Number(s)	Manufacturer	Package Size	Specifications
C1, C3, C4	22μF ±20%	GRM21BR61C226ME44L	Murata	0805	16V Ceramic, X5R
C2	47nF ±10%	CL10B473KB8NNNC	SAMSUNG	0603	50V Ceramic, X7R
L1	1μH ±20%	FTC252012S1R0MBCA	CJIANG	2.5*2.0*1.2mm	Isat=5.0A, DCR=42mΩ
R1	NC	N/A	N/A	N/A	N/A
R2	40.2kΩ ±1%	0603WAF4022T5E	UNI-ROYAL	0603	±1%, 100mW
R3	1kΩ ±1%	0603WAF1001T5E	UNI-ROYAL	0603	±1%, 100mW
R4	280kΩ ±1%	0603WAF2803T5E	UNI-ROYAL	0603	±1%, 100mW
LED	20mA	KT-0603R	KENTO	0603	40mW, Vf=2.4V

Charge Current Setting

The charger current is set by the resistor value at the ISET pin according to the equation below:

$$I_{CHG}\,(A) = K_{ICHG}\,(A{\cdot}k\Omega) / R_{ISET}(k\Omega) \qquad (3)$$

K_{ICHG} is current setting gain that is listed in Electrical Characteristics table and RISET is the resistor value from ISET pin to GND. K_{ICHG} is typically 40 (A·kΩ).

Application and Implementation

Application Curves

(L=1μH, C1, C3, C4 =22μF, C2= 47nF and T_J = 25°C unless otherwise noted; The schematic is as shown in Figure 11)

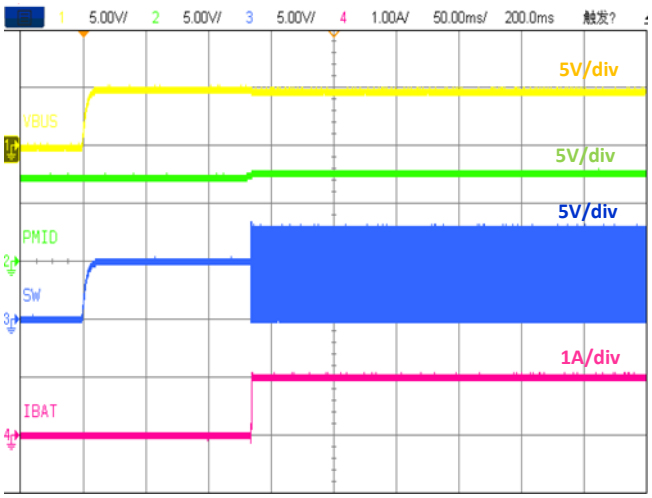


Figure 12. Startup from VBUS
(VBUS=5V, VBAT=7.6V, ICHG=1A)

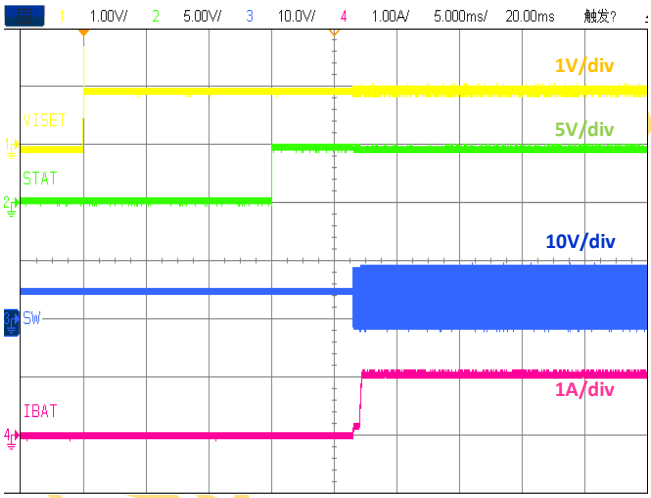


Figure 13. RISET released from short
(VBUS=5V, VBAT=7.6V, ICHG=1A)

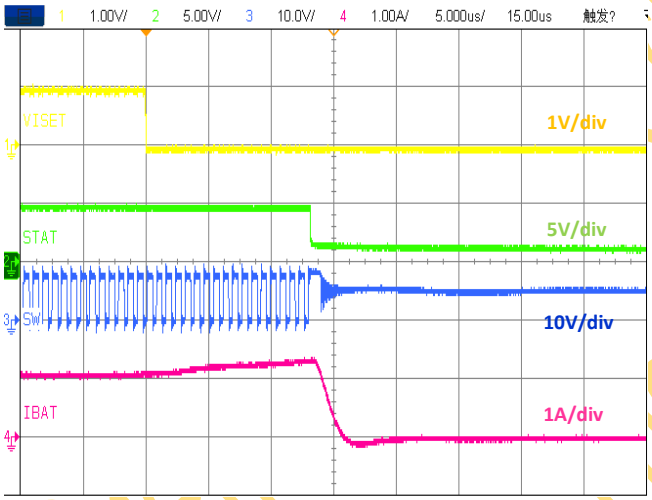


Figure 14. RISET Short
(VBUS=5V, VBAT=7.6V, ICHG=1A)

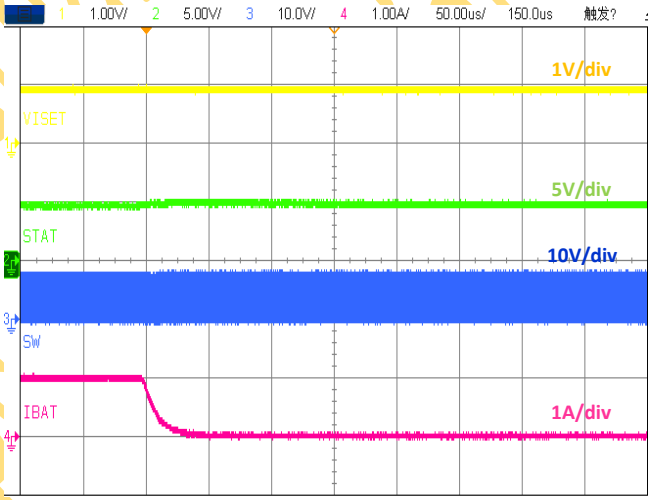


Figure 15. RISET open
(VBUS=5V, VBAT=7.6V, ICHG=1A)

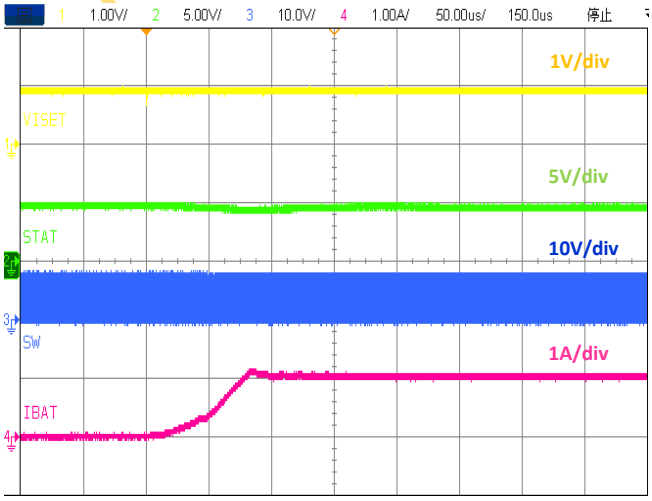


Figure 16. RISET re-connected
(VBUS=5V, VBAT=7.6V, ICHG=1A)

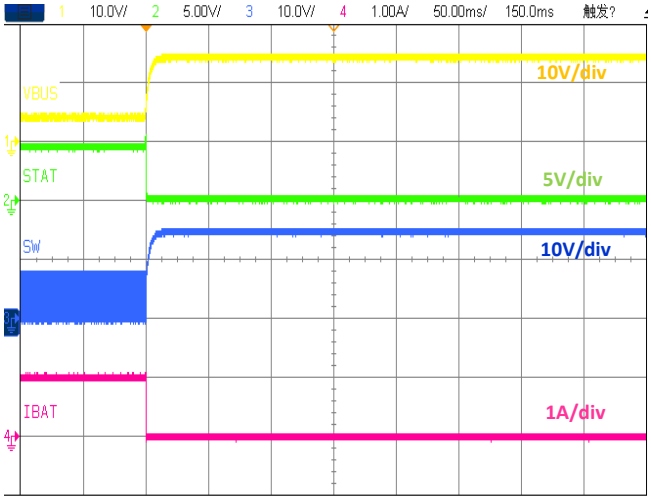


Figure 17. Input Over Voltage
(VBUS=5V to 15V, VBAT=7.6V, ICHG=1A),

Application and Implementation

Application Curves

(L=1μH, C1, C3, C4 =22μF, C2= 47nF and TJ = 25°C unless otherwise noted; The schematic is as shown in Figure 11)

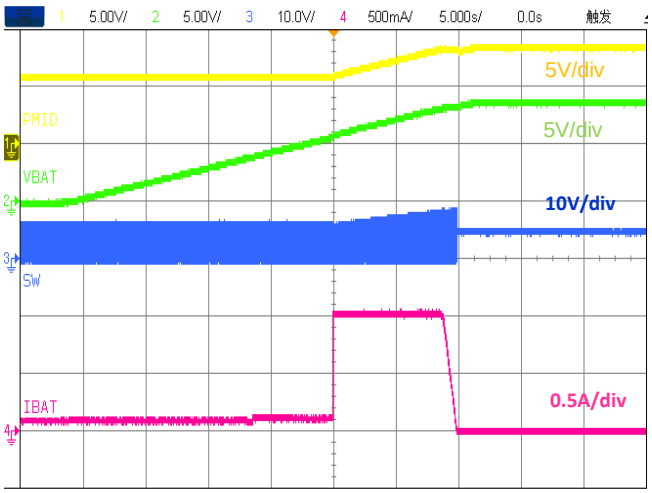


Figure 18. Battery Charge Cycle (VBUS=5V, ICHG=1A)

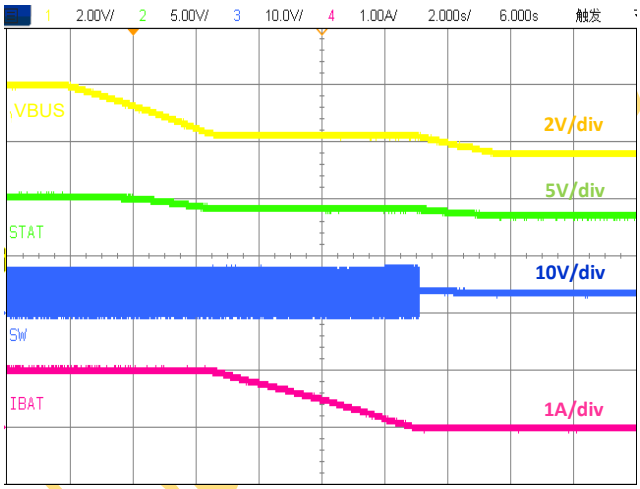


Figure 19. Input Voltage Dynamic Power Management (VIN=7.5V to 3.5V, ICHG=1A, a 0.7Ω resistor is connected in series between VIN and VBUS)

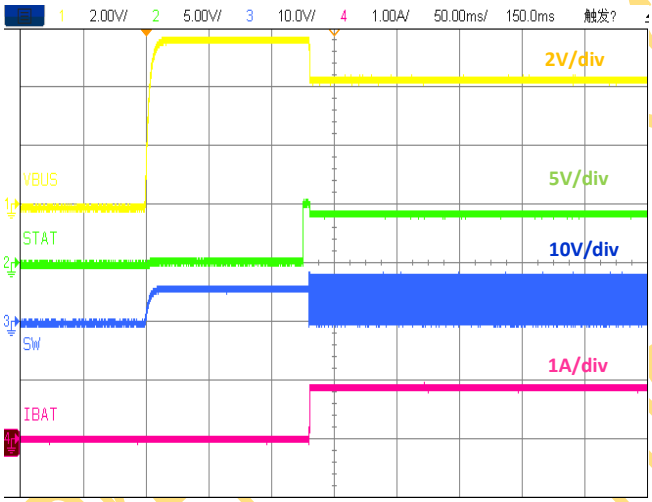


Figure 20. Input Voltage Dynamic Power Management (VIN Hot-Plug, VIN=5.7V, ICHG=1.5A a 0.7Ω resistor is connected in series between VIN and VBUS)

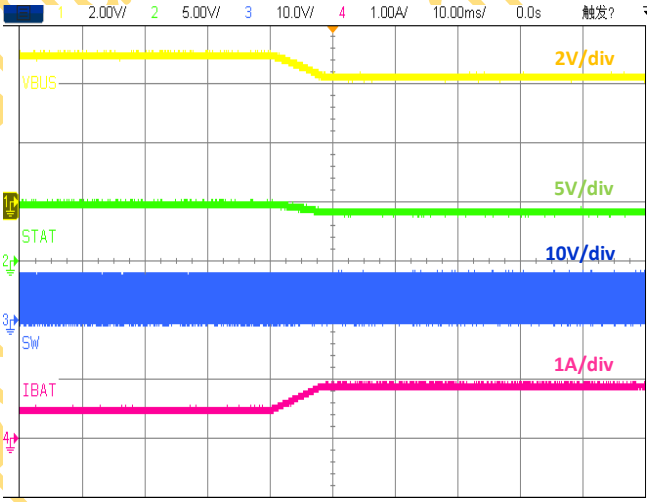


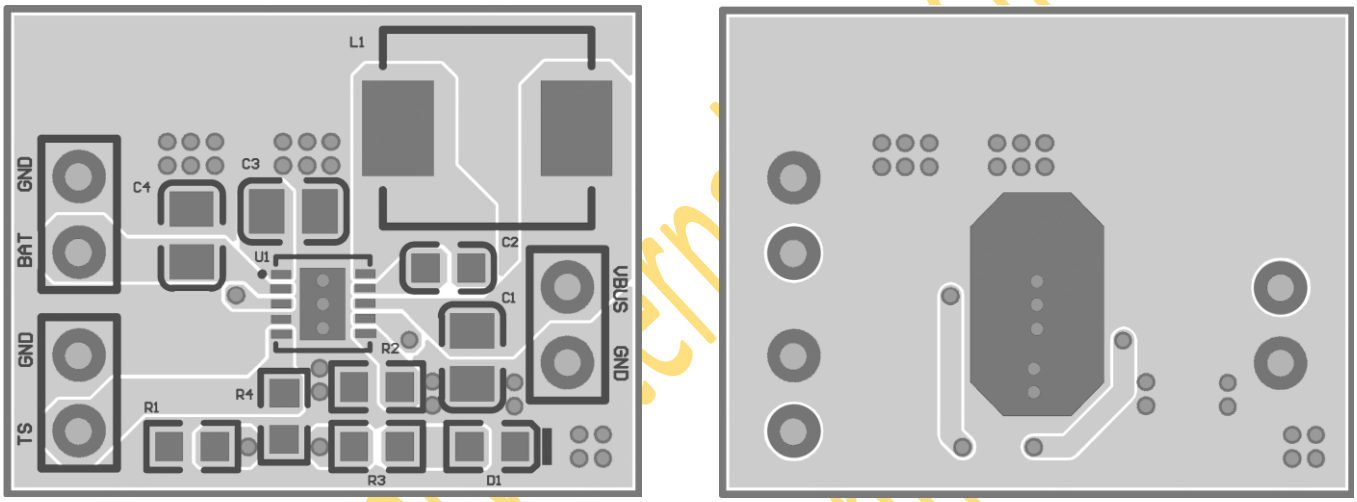
Figure 21. Input Voltage Dynamic Power Management (ICHG=0.5A→1.5A, VIN=5.7V, a 0.7Ω resistor is connected in series between VIN and VBUS)

PCB Layout Guideline

Appropriate PCB layout is important in the switching power supply design, especially at high peak currents and high switching frequencies. Good PCB layout minimizes EMI and noise, allows good output voltage regulation and achieves higher efficiency. Therefore, use wide and short traces for the main current path and for the power ground paths. The following design considerations are recommended:

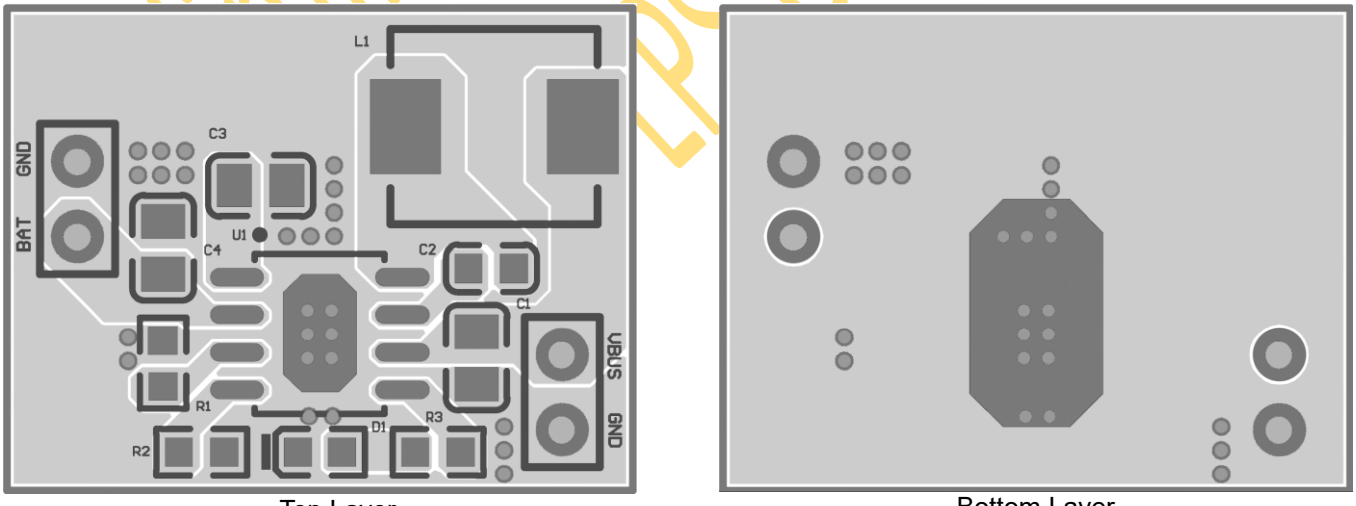
- Using a ceramic capacitor to decouple PMID pins to GND on top layer or through GND copper plane with short and wide copper path.
- Decouple VBUS to GND on top layer and place decoupling capacitors as close to these Pins as possible. Always avoid vias if possible because they have parasitic inductance and resistance. If vias are inevitable, always use more than one vias in parallel to decrease parasitic for power traces.
- Connect GND pad to the ground plane on the bottom side with multiple vias that is for both heat dissipation and electrical connection.
- Place inductor closed to SW node, minimize switching SW node size and trace lengths, keep SW and BST nodes away from ISET.

The examples of 20mmx15mm 2-layer PCB layouts a shown in Figure 22, 23, refer to Figure 11 for schematic.



Top Layer Bottom Layer

Figure 22. DFN3x3-10L, 2-layer PCB Layout Example (20mm x 15mm)

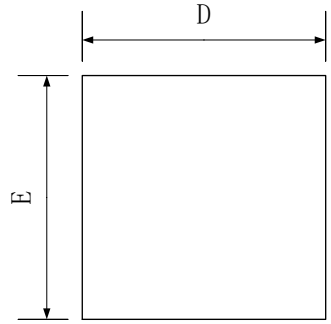


Top Layer Bottom Layer

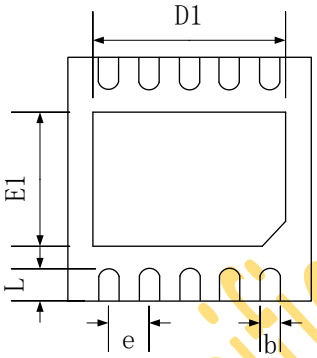
Figure 23. ESOP-8, 2-layer PCB Layout Example (20mm x 15mm)

Packaging Information

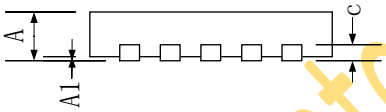
DFN-10



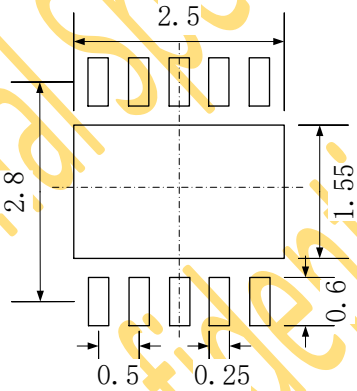
TOP VIEW



BOTTOM VIEW



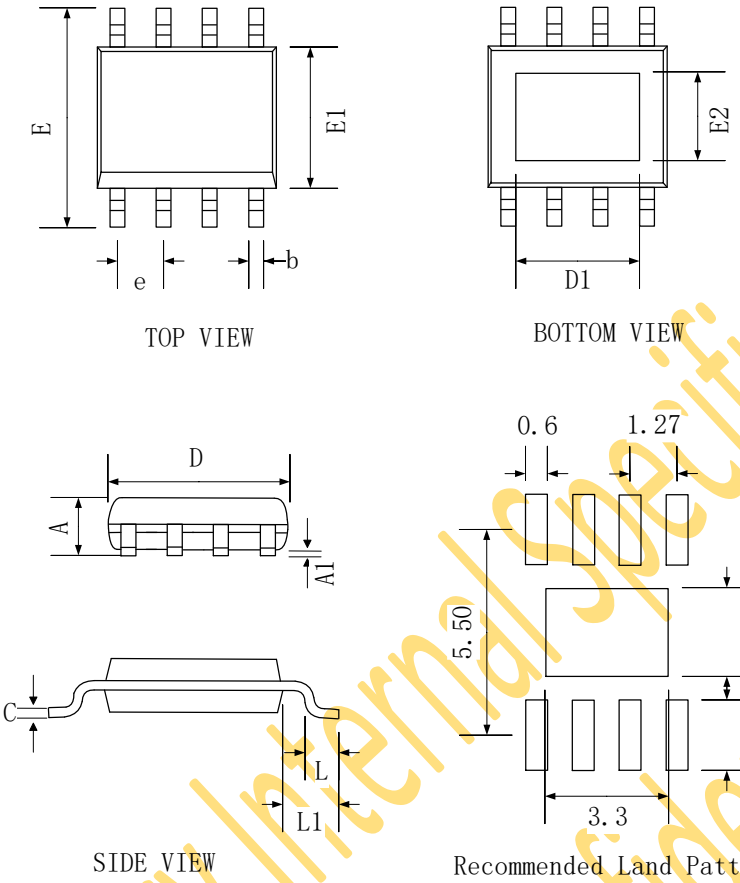
SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.2	0.25	0.30
C		0.203 REF	
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
e		0.50 BSC	
L	0.30	0.40	0.50

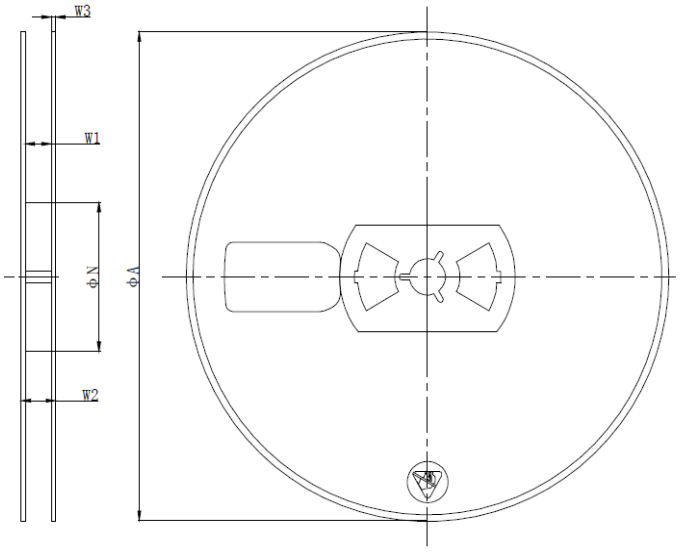
ESOP-8



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.00	-	0.15
b	0.30	0.40	0.50
c		0.20 REF	
D	4.70	4.90	5.10
D1		3.2 REF	
E	5.70	6.00	6.30
E1	3.70	3.90	4.10
E2		2.30 REF	
e		1.27 BSC	
L	0.40	0.60	0.80
L1		1.05 REF	

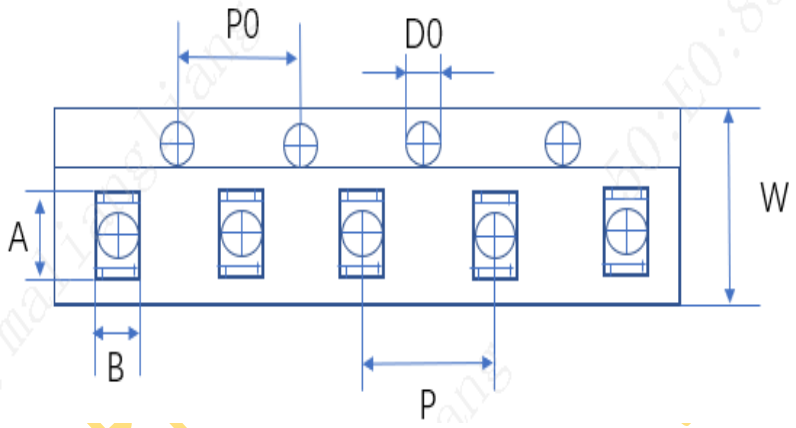
Tape and Reel information-DFN-10L

REEL DIMENSIONS (Unit: mm)



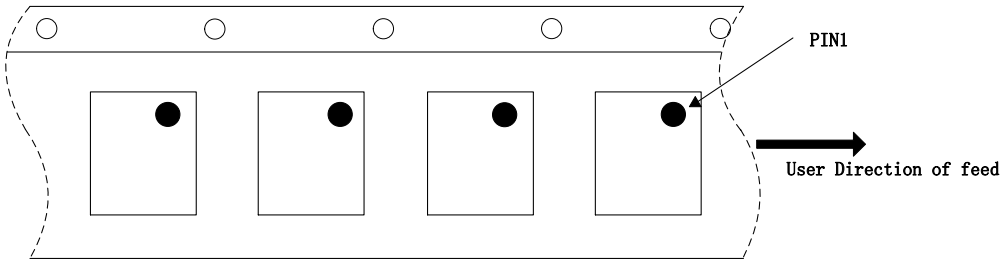
ΦA	W2
329±2	16.4±2

TAPE DIMENSIONS (Unit: mm)



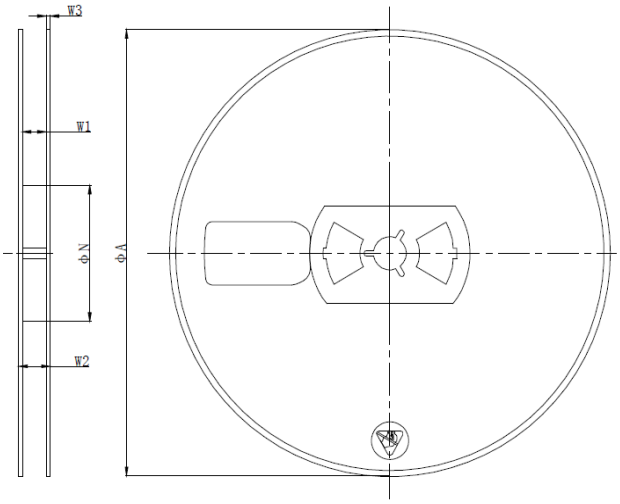
Device	A	B	P0	P	D0	W	C
LP4121QVF	3.4±0.30	3.4±0.30	4.0±0.10	8.0±0.10	1.55±0.10	12.00±0.30	1.10±0.15

PIN1 AND TAPE FEEDING DIRECTION



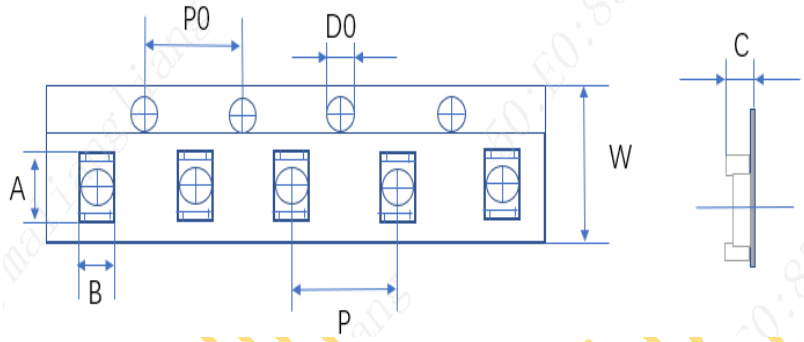
Tape and Reel information-ESOP-8

REEL DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	325.00	329.00	333.00
W2	15.00	17.00	19.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	6.20	6.60	7.00
B	5.10	5.50	5.90
P0	3.80	4.00	4.20
P	7.80	8.00	8.20
D0	1.30	1.50	1.70
W	11.90	12.00	12.30
C	1.90	2.10	2.30

PIN1 AND TAPE FEEDING DIRECTION