Features

- Input Supply Voltage Range
  VDD: 2.7V to 5.5V
  VGH1/2: 16V to 40V
  VGL/LVGL: -18V to -3.0V
- 16 Channel Level Shifter Support
  10-ch CLK,2-ch STV,LC1/LC2,LS_VGL,LS_LVGL
- High Output Slew Rate to Drive Up to 4.7nF Load
  CLK Programmable Slew Rate control
- 55V Maximum Input for VGH1/2 - VGL
- Support 2 in Multi-Out
- Support 2 line mode
- Power Off Discharge Option
- IIC Interface
- Output Over Current Protection
  Programmable Output Current
  Programmable Current Detect time
- Over Temperature Protection
- RoHS Compliant and 100% Lead(Pb)-Free
- Compact Package: TQFN4×4-32

Applications

- LCD Panels Using GIP / GOA / ASG Technology

Order Information

LP6296B □ □ □

- F:Green
- Package Type
  QV:TQFN4X4-32

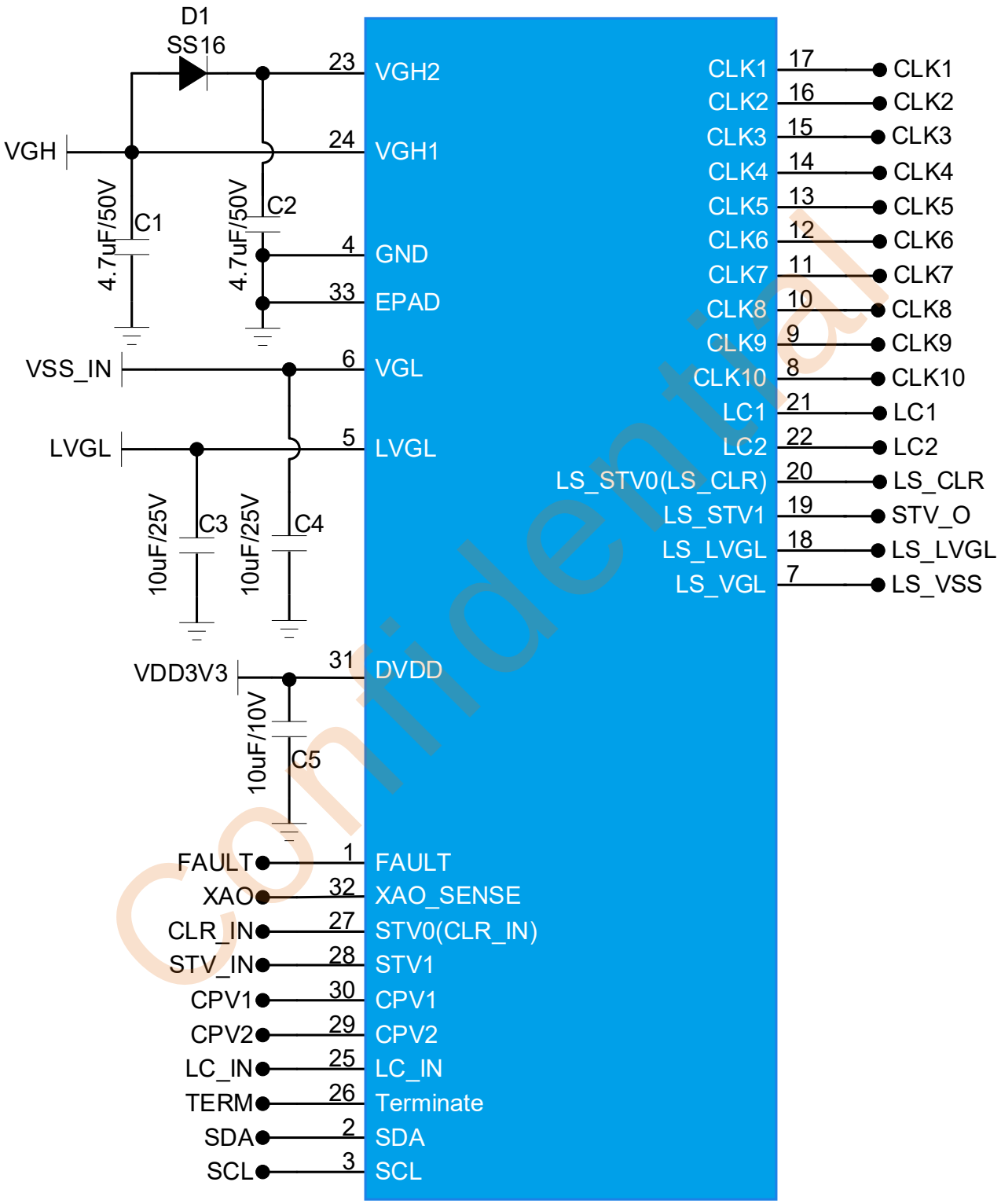
General Description

The LP6296B is a 16-CH high voltage level shifter with application such as TV and monitor. It converts logic level signals from Timing Controller (T-CON) to high level signals used by the LCD panel. The outputs are switching from VGL/LVGL to VGH1/VGH2, with capacitive loads up to 4.7nF.

Level shifter is designed for generating a high voltage signal to drive the TFT LCD panel. It provides outputs (LS_STV0/1, LC1/2, CLK1~10, LS_VGL, LS_LVGL) which are switching from VGL/LVGL to VGH1/2, it also integrates Terminate function.

The LP6296B features extensive protection functions that include OCP, OTP. It is available in a 4mmx4mm, 32-lead TQFN package.

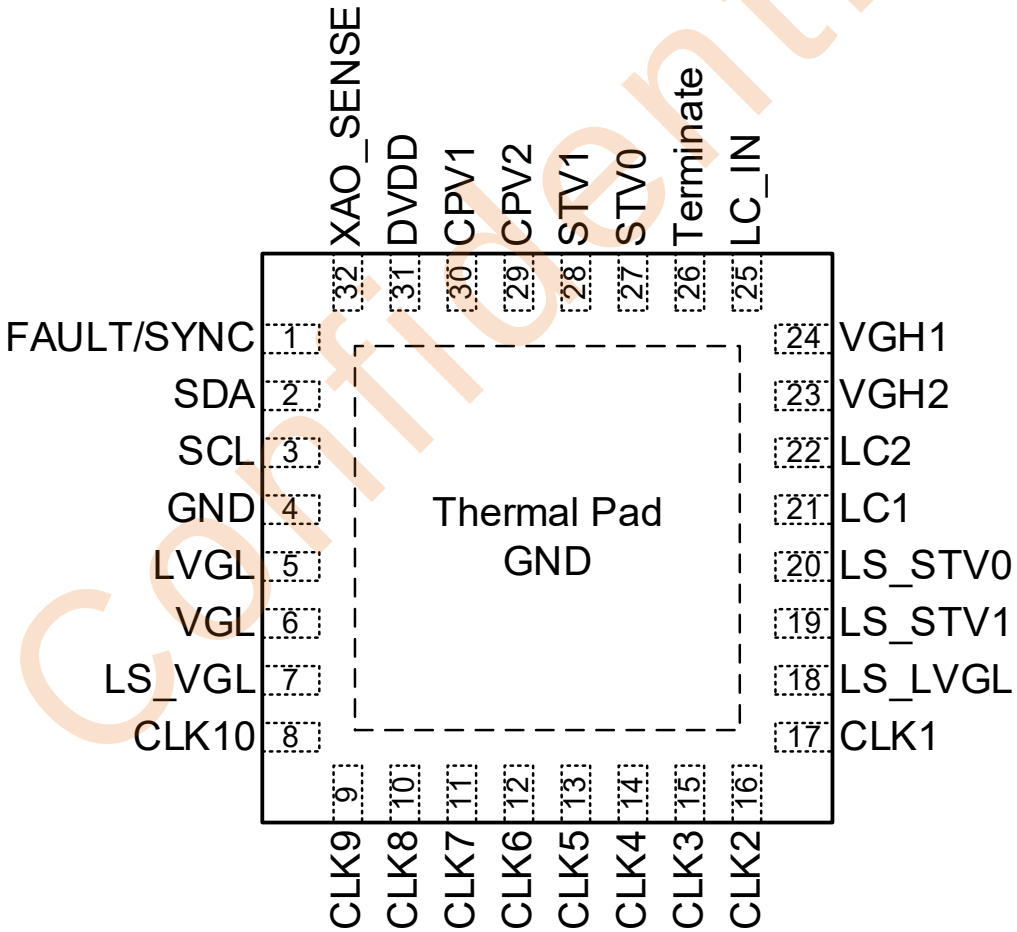
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6296BQVF	LPS LP6296B YWX	MSL3	TQFN4X4-32	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



LP6296BQVF

Pin Description

Pin#	Name	Description
1	FAULT/SYNC	FAULT terminal SYNC_XON Function Detect
2	SDA	I2C - Compatible serial bidirectional data line.
3	SCL	I2C - Compatible clock input.
4	GND	Ground.
5	LVGL	LC1/2、CLK1 to 10and LS_STV0/1 negative power supply. (The voltage of LVGL must be lower (or equal) than VGL)
6	VGL	Low level of LS_VGL circuit.
7	LS_VGL	Discharge function for liquid crystal capacitor.
8	CLK10	Level Shift Output.
9	CLK9	Level Shift Output.
10	CLK8	Level Shift Output.
11	CLK7	Level Shift Output.
12	CLK6	Level Shift Output.
13	CLK5	Level Shift Output.
14	CLK4	Level Shift Output.
15	CLK3	Level Shift Output.
16	CLK2	Level Shift Output.
17	CLK1	Level Shift Output.
18	LS_LVGL	Discharge function for liquid crystal capacitor.
19	LS_STV1	Level Shift Output.
20	LS_STV0	Level Shift Output.
21	LC1	Level shifter output signal (Low frequency clock 1)
22	LC2	Level shifter output signal (Low frequency clock 2)
23	VGH2	LS_STV0(LS_CLR) and LS_LC1,LS_LC2 positive power supply.
24	VGH1	LS_STV1,LS_CLK1 to 10,LS_VGL,LS_LVGL positive power supply.
25	LC_IN	Level shifter input signal (low frequency clock). The LC is the high/low level trigger.
26	Terminate	Level shifter input signal. Pull CLK1 to CLK10 low on TERMINATE rising edge.
27	STV0	Level shifter input signal (condensed clock) The STV0 is rising/falling edge trigger.
28	STV1	Level shifter input signal (condensed clock) The STV1 is rising/falling edge trigger.
29	CPV2	Level shifter input signal (condensed clock) The CPV2 is rising/falling edge trigger.
30	CPV1	Level shifter input signal (condensed clock) The CPV1 is rising/falling edge trigger.
31	DVDD	Supply voltage input.
32	XAO-SENSE	XAO Function Input
33	EPAD	GND The exposed pad must be soldered to a large PCB and connected to GND for maximum dissipation.

Absolute Maximum Ratings (Note1)

DVDD to GND ---------- -0.3V to +7V
VGH1/2 to GND ----------0.3V to +45V
VGL,LVGL to GND ----------25V to +0.3V
VGH1/2 to VGL/LVGL ----------0.3V to +60V
FAULT to GND ---------- -0.3V to +7V
STV0/1,CPV1/2,LC_IN,Terminate to GND ---------- -0.3V to +7V
LS_STV0,LS_STV1,LC1,LC2,CLKn,LS_VGL,LS_LVGL to GND---------- VGL+0.3V to VGH-0.3V

Note1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 3KV
HBM (Human Body Model) LVSH_I/O to GND ---------- 8KV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 800V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ----------150℃
Operating Junction Temperature Range (TJ)---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec)----------260℃
θ_{JA} (Junction-to-Ambient Thermal Resistance) ----------54.5℃/W
θ_{JC} (Junction-to-CaseThermal Resistance) ----------19℃/W

Electrical Characteristics

(DVDD = 3.3V, VGH1/2=30V, VGL=-6.0V, LVGL = -10V, GND= 0V, TA= 25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
V_{DD}	Supply Voltage		2.7		5.5	V
$V_{GH1/2}$	VGH Input Voltage Range	VGH_UVLO_R=15V	16		40	V
$V_{GH1/2}$	VGH Input Voltage Range	VGH_UVLO_R=7V	8		40	V
V_{GL}	VGL Input Voltage Range		-18		-3.0	V
V_{LVGL}	LVGL Input Voltage Range		-18		-3.0	V
V_{GH} -V_{LVGL}	Voltage difference between VGH & LVGL				55	V
$I_{VGH1/2}$	VGH1+VGH2 Quiescent current	CPVx=STVx=0V		1.8	3.0	mA
I_{VGL}	VGL Quiescent current	CPVx=STVx=0V		0.1		mA
I_{LVGL}	LVGL Quiescent current	CPVx=STVx=0V		0.5		mA
$V_{DD\_UVLO\_R}$	DVDD Under Voltage Lockout Threshold	VDD Rising,Hys.=600mV	2.5	2.6	2.7	V
$V_{DD\_UVLO\_F}$		VDD Falling	1.8	2.0	2.2	V
$V_{GH\_UVLO\_R1}$	VGH2 Under Voltage Lockout Threshold	VGH2 Rising 1	14	15	16	V
$V_{GH\_UVLO\_R2}$		VGH2 Rising 2	6	7	8	V
$V_{GH\_UVLO\_F}$		VGH2 Falling	5	5.5	6	V
V_{GH_POR}	VGH2 Power on Reset voltage	VGH2 POR	2.5	3	3.5	V
	DVDD Discharge Under Voltage Lockout Threshold	DVDD Falling Hys.=200mV	2.37	2.5	2.63	V
T_{SD}	Thermal Shutdown Temperature	Rising, Hys=20℃	130	150	170	℃
T_{HYS}	Thermal Shutdown Hysteresis			20		℃
INPUT SIGNALS (CPV1,CPV2,STV0,STV1,LC_IN,TERMINATE,FAULT)						
	Maximum Operating Frequency CPV1/CPV2		550			KHz
V_{IW}	Input Signal Minimum Pulse Width		150			nS
V_{IL}	CPV1,CPV2,STV0,STV1,LC_IN,TERMINATE Input Voltage	VDD = 2.6V to 5.5V			0.6	V
V_{IH}		VDD = 2.6V to 5.5V	1.5			V
$R_{PULL.DOWN}$	CPV1,CPV2,STV0,STV1,LC_IN,TERMINATE Internal Pull Down Resistor			400		KΩ
$R_{PULL.UP}$	FAULT Internal Pull Up Resistor			200		KΩ
Level Shifter Output (CLK1 to CLK10)						
$R_{DS(ON).HS}$	CLK1 to CLK10 High-Side Resistance	ILOAD=10mA		9		Ω
$R_{DS(ON).LS}$	CLK1 to CLK10 Low-Side Resistance	ILOAD=10mA		7		Ω
Slew+	CLKx Rising Slew Rate	RL=51Ω,CL=4.7nF VOUT=20% to 80%		1000		V/uS
Slew-	CLKx Falling Slew Rate	RL=51Ω,CL=4.7nF VOUT=20% to 80%		1000		V/uS
T_{PR}	CLKx Rising Edge Propagation Delay	COUT=150pF		60	100	nS
T_{PF}	CLKx Falling Edge Propagation Delay	COUT=150pF		60	100	nS

Note：The sequence of LVGL must be earlier (or equal) than VGL in the application. And the voltage of LVGL must be lower(or equal) than VGL　Rising/Falling time measure point is before RC

Electrical Characteristics

(DVDD = 3.3V, VGH1/2=30V, VGL=-6.0V, LVGL = -10V, GND= 0V, TA= 25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Level Shifter Output (LS_STV0,LS_STV1,LC1,LC2,LS_VGL,LS_LVGL)						
$R_{DS(ON).HS}$	LS_STV0,LS_STV1,LC1,LC2,LS_VGL,LS_LVGL High-Side Output Resistance	ILOAD=10mA		9		Ω
$R_{DS(ON).LS}$	LS_STV0,LS_STV1,LC1,LC2,LS_VGL,LS_LVGL Low-Side Output Resistance	ILOAD=10mA		7		Ω
Slew+	LS_STV0,LS_STV1,LC1,LC2 Rising Slew Rate	RL=51Ω,CL=4.7nF VOUT=20% to 80%		700		V/uS
Slew-	LS_STV0,LS_STV1,LC1,LC2 Falling Slew Rate	RL=51Ω,CL=4.7nF VOUT=20% to 80%		700		V/uS
	LS_VGL,LS_LVGL Rising Time	RL=51Ω,CL=4.7nF VOUT=10% to 90%			1	uS
T_{PR}	LS_STV0,LS_STV1,LC1,LC2 Rising Propagation Delay	COUT=150pF		60	100	nS
T_{PF}	LS_STV0,LS_STV1,LC1,LC2 Falling Propagation Delay	COUT=150pF		60	100	nS
Over Current Protection (CLK1 to CLK10,LS_STV0,LS_STV1,LC1/LC2,LS_VGL,LS_LVGL)						
	CLK1 to CLK10 Current detect level	02h [2:0] = 001	20	30	40	mA
		02h [2:0] = 010	40	50	60	mA
		02h [2:0] = 011	60	70	80	mA
		02h [2:0] = 100	77	90	103	mA
		02h [2:0] = 101	102	120	138	mA
		02h [2:0] = 110	136	160	184	mA
		02h [2:0] = 111	170	200	230	mA
	LS_STV0,LS_STV1,LC1/LC2 LS_VGL,LS_LVGL Current detect level	02h [5:3] = 001	20	30	40	mA
		02h [5:3] = 010	40	50	60	mA
		02h [5:3] = 011	60	70	80	mA
		02h [5:3] = 100	77	90	103	mA
		02h [5:3] = 101	102	120	138	mA
		02h [5:3] = 110	136	160	184	mA
		02h [5:3] = 111	136	160	184	mA
	CLK High-Side Detect time	Error = +/-20% Except for 2us	2	---	16	uS
	CLK Low-Side Detect time	Error = +/-20% Except for 2us	2	---	16	uS
	LS_STV0/LS_STV1 High-Side Detect time	Error = +/-20% Except for 2us	2	---	16	uS
	LS_STV0/LS_STV1 Low-Side Detect time	STV1 rising edge	32	40	48	uS
	LC1/2 High-Side Detect time		32	40	48	uS
	LC1/2, LS_VGL, LS_LVGL Low-Side Detect time		32	40	48	uS

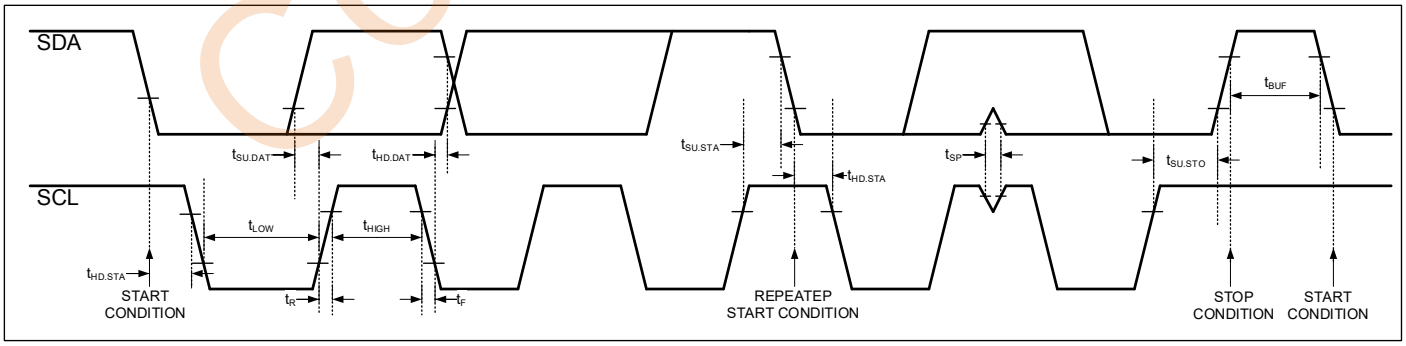
Electrical Characteristics

(DVDD = 3.3V, VGH1/2=30V, VGL=-6.0V, LVGL = -10V, GND= 0V, TA= 25℃)
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IIC INTERFACE(SDA,SCL)						
V_{IH}	High Level Input Voltage		1.2	---	---	V
V_{IL}	Low Level Input Voltage		---	---	0.6	V
IIC TIMING CHARCTERISTICS						
F_{SCL}	Serial-Clock Frequency		1	---	600	KHz
T_{BUF}	Bus Free Time Between STOP and START Conditions		1300	---	---	nS
$T_{HD.STA}$	Hold Time(Repeated) START Condition		600	---	---	nS
T_{LOW}	SCL Pulse-Width Low		1300	---	---	nS
T_{HIGH}	SCL Pulse-Width High		600	---	---	nS
$T_{SU.STA}$	Setup Time for a Repeated START Condition		600	---	---	nS
$T_{HD.DAT}$	Data Hold Time		50	---	800	nS
$T_{SU.DAT}$	Data Setup Time		100	---	---	nS
T_R	SDA and SCL Receiving Rise Time	CB is IN pF	20+ 0.1CB	---	300	nS
T_F	SDA and SCL Receiving Fall Time	CB is IN pF	20+ 0.1CB	---	300	nS
T_F	SDA Transmitting Fall Time	CB is IN pF	20+ 0.1CB	---	300	nS
$T_{SU.STO}$	Setup Time for STOP Condition		600	---	---	nS
CB	Bus Capacitance		---	---	400	pF
T_{SP}	Pulse Width of Suppressed Spike		---	85	---	nS

I2C Serial-Interface

The LP6296B communicates through an industry standard 2-wire I2C serial-interface to receive data in slave mode. The bus consists of a data line (SDA) and a clock line (SCL) with pull-up structures. A master device, usually a microcontroller or a digital signal processor, controls the bus.



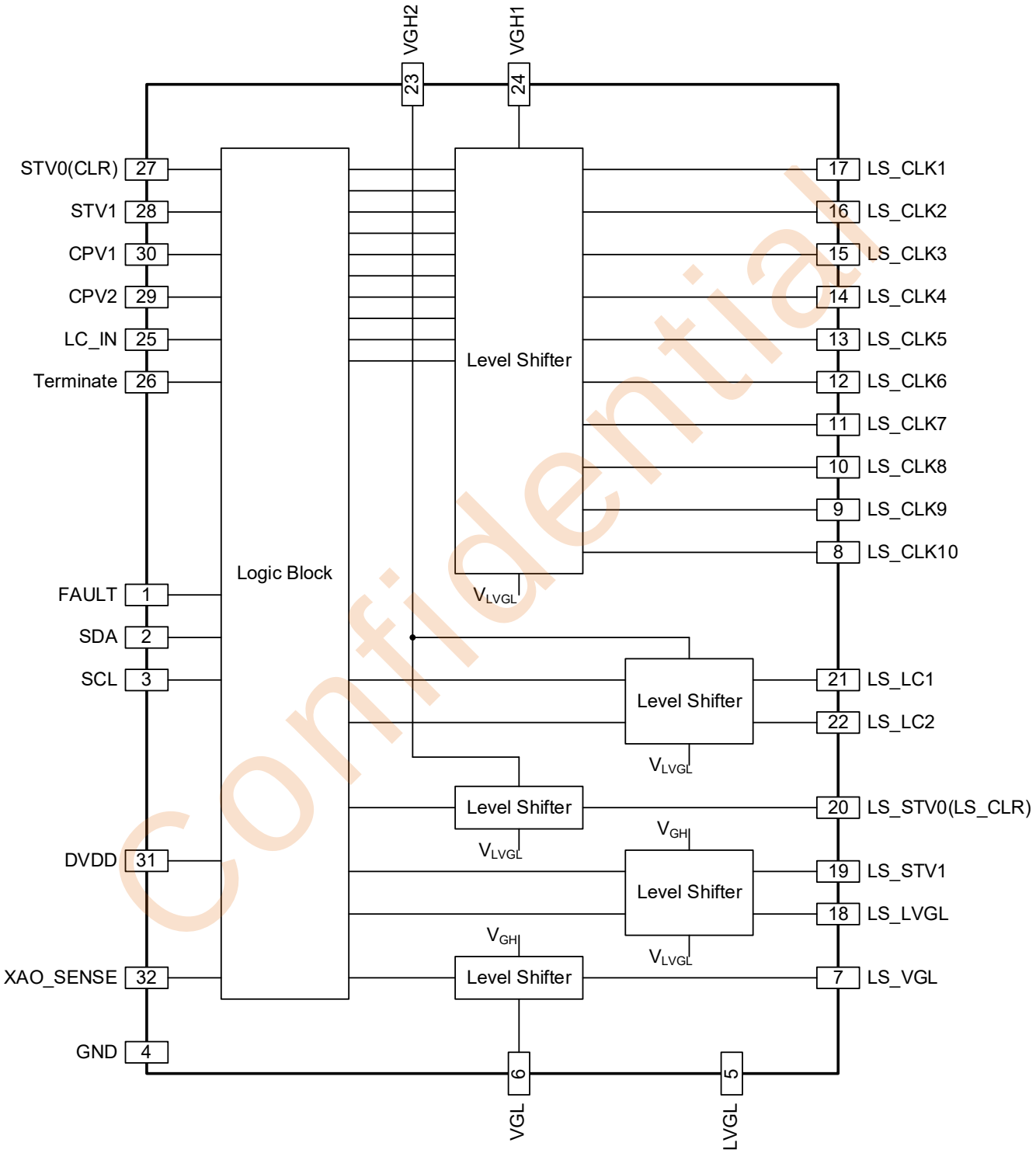
Note：

The input signal pulse width must be over 150ns

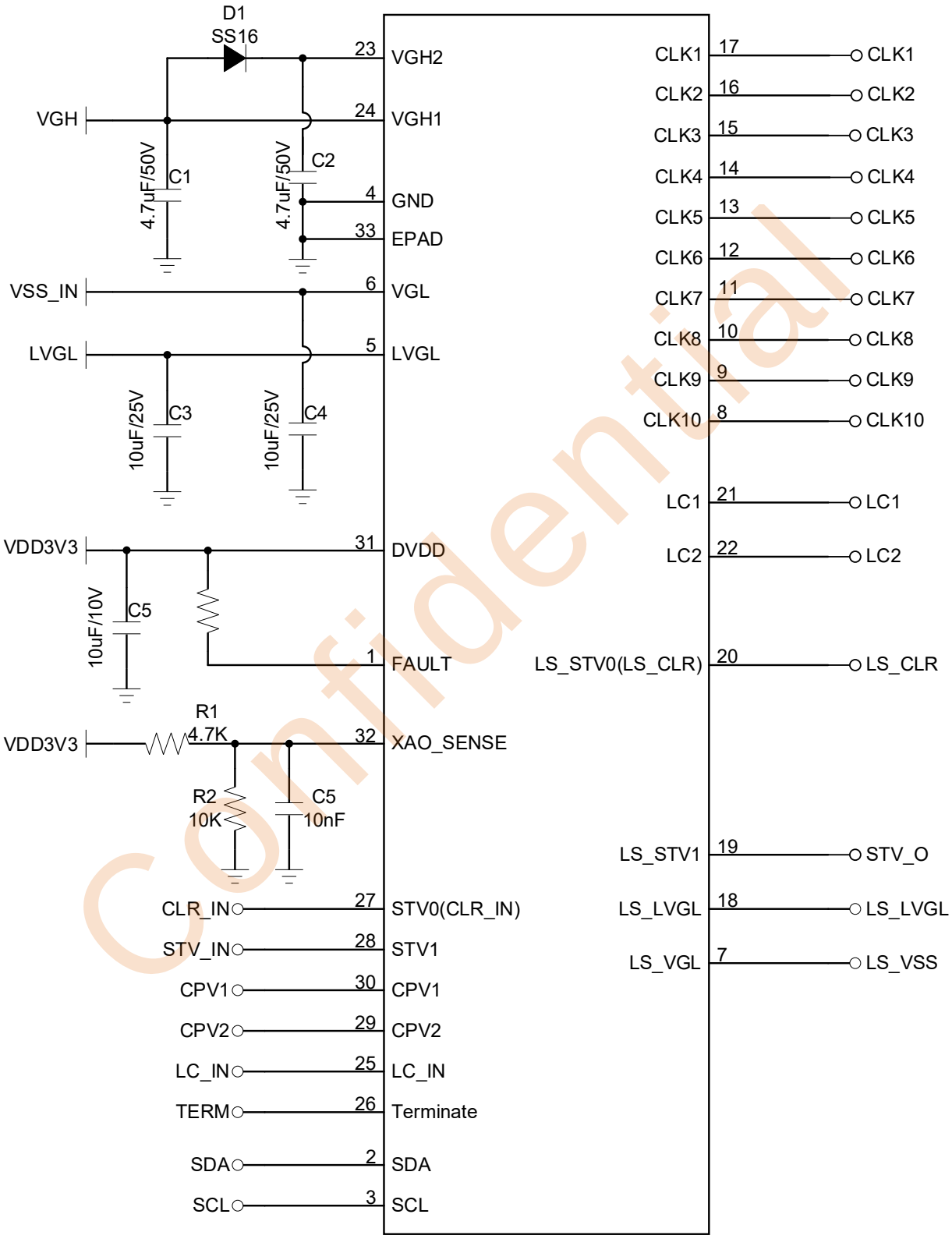
CLK1 to CLK10 Slew Rate can select by 03h [7:6]

LS_STV0,LS_STV1 High-Side Detect time can select by 03h [2:0]

Functional Block Diagram

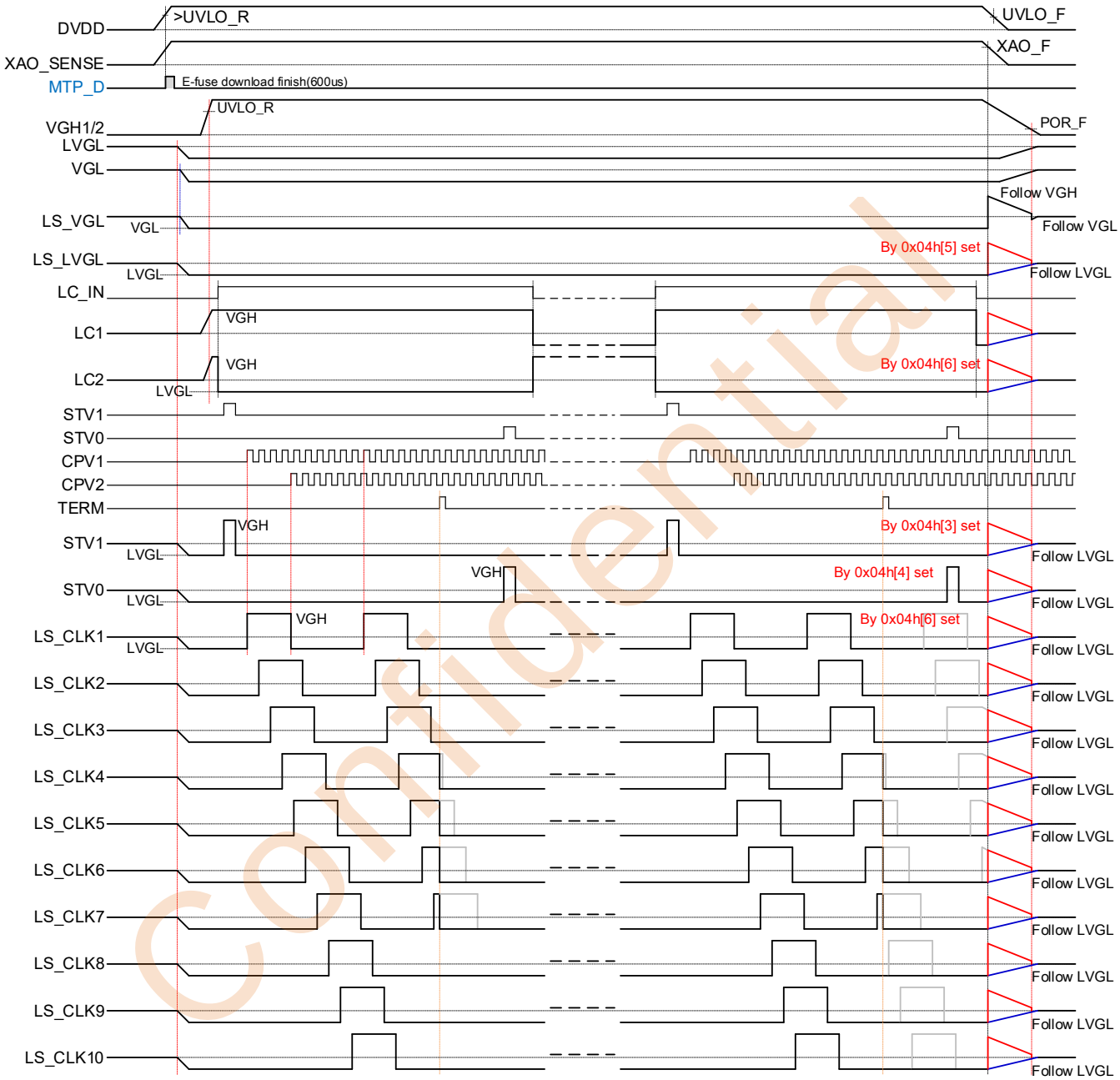


Typical Application Circuit



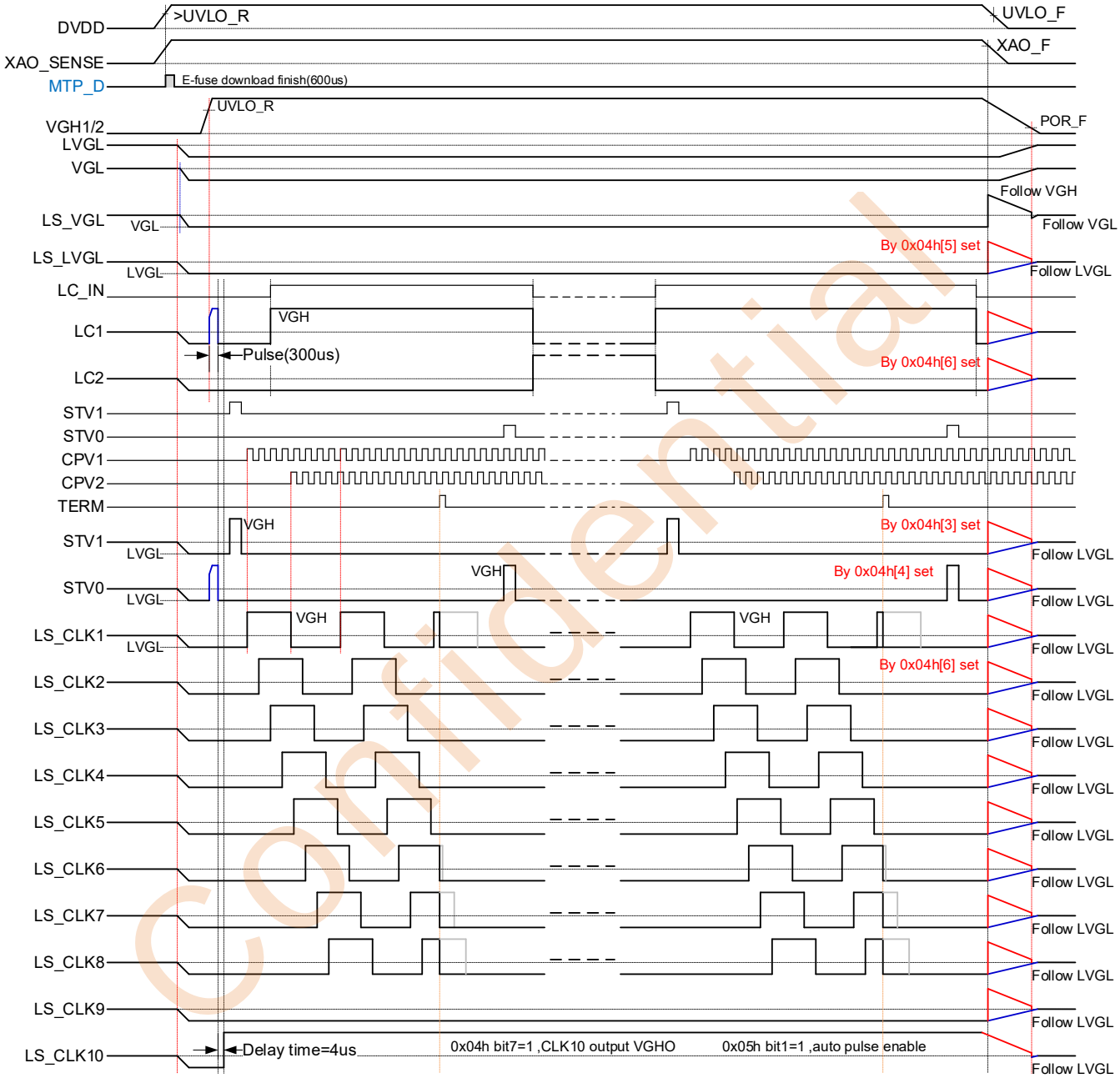
Timing Diagram MODE1

Power On/Off Sequence



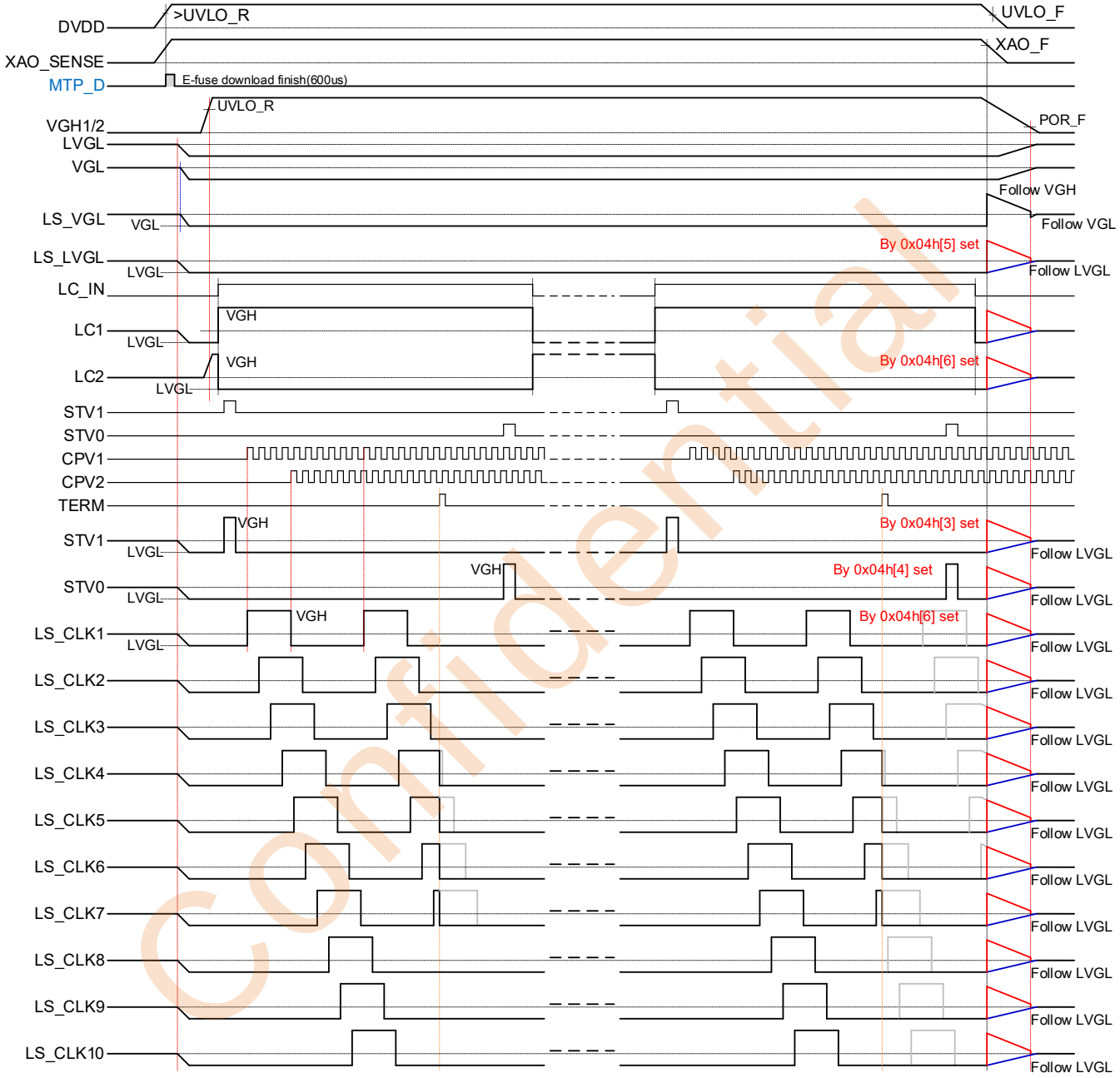
Timing Diagram MODE2

Power On/Off Sequence



Timing Diagram MODE3

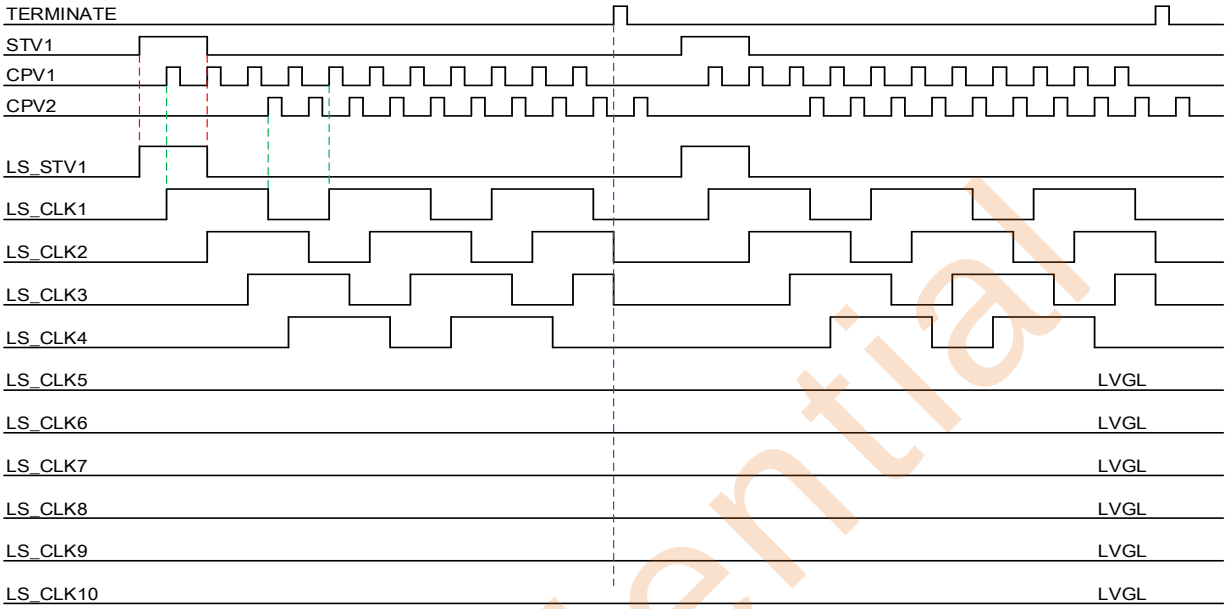
Power On/Off Sequence



Application for 2-In 4-Out waveform

LS_CLKO_PH(0x04 [1:0] = 00 : 4 phase; CLK5 to 10 still do discharge at power-off)

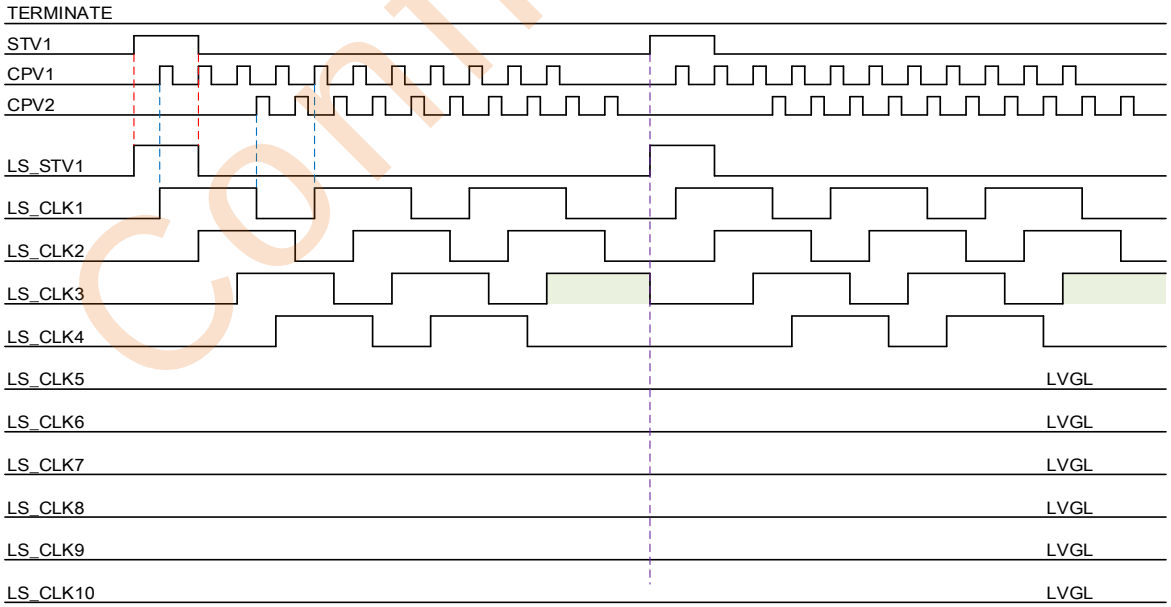
STV1_RST(0x04 [2] = 0 Don't reset all L/S CLKx output)



Application for 2-In 4-Out waveform

LS_CLKO_PH(0x04 [1:0] = 00 : 4 phase CLK5 to 10 still do discharge at power-off)

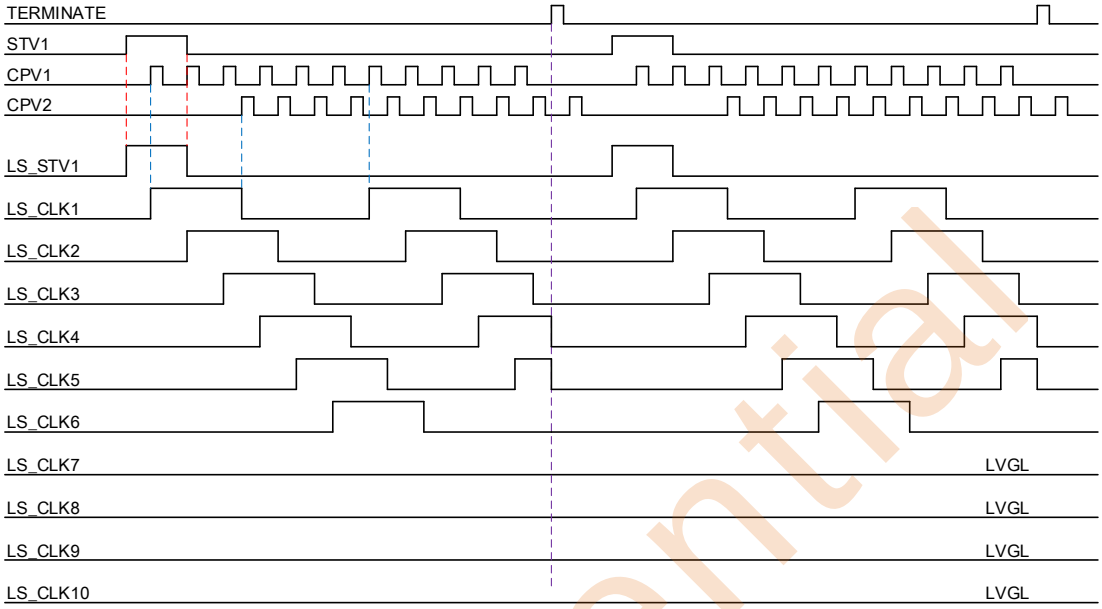
STV1_RST(0x04 [2] = 1 Reset all L/S CLKx output to LVGL)



Application for 2-In 6-Out waveforms

LS_CLKO_PH(0x04 [1:0] = 01 : 6 phase; CLK7 to 10 still do discharge at power-off)

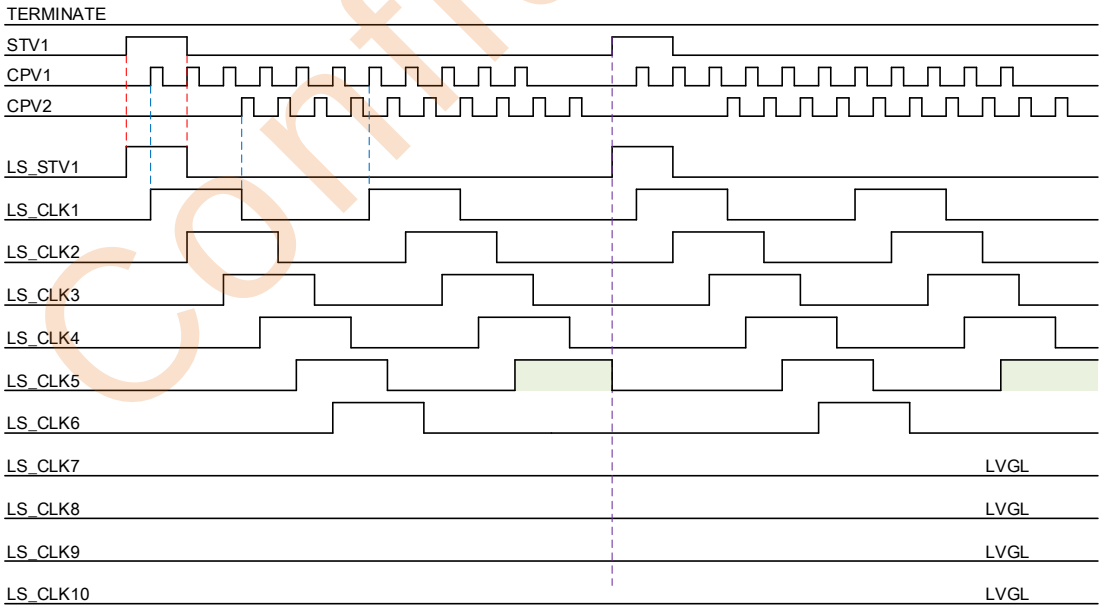
STV1_RST(0x04 [2] = 0 Don't reset all L/S CLKx output)



Application for 2-In 6-Out waveforms

LS_CLKO_PH(0x04 [1:0] = 01 : 6 phase CLK7 to 10 still do discharge at power-off)

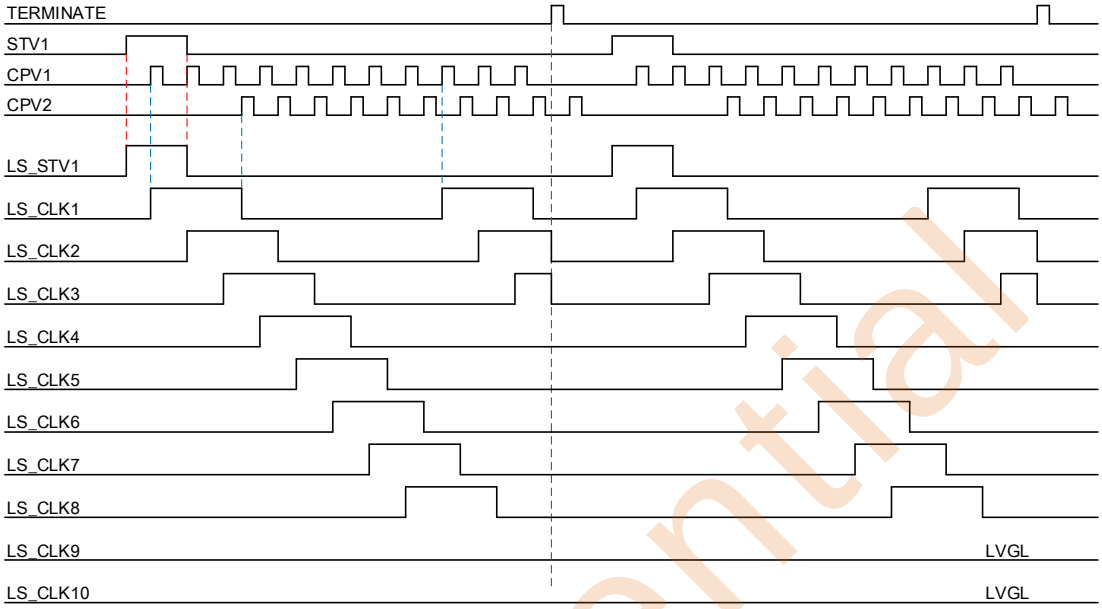
STV1_RST(0x04 [2] = 1 Reset all L/S CLKx output to LVGL)



Application for 2-In 8-Out waveforms

LS_CLKO_PH(0x04 [1:0] = 10 : 8 phase; CLK9 to 10 still do discharge at power-off)

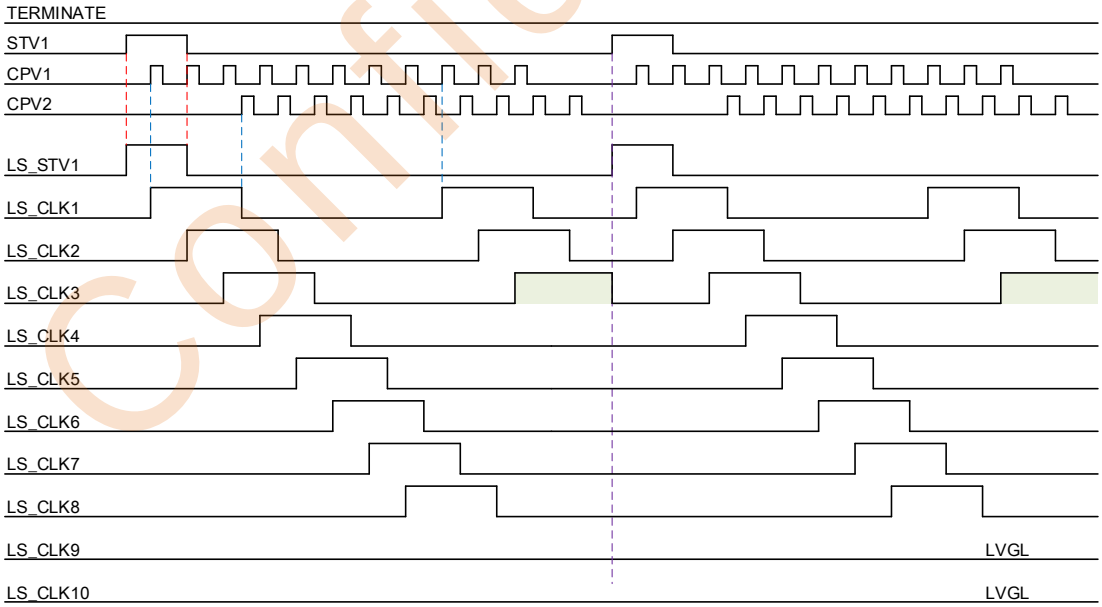
STV1_RST(0x04 [2] = 0 Don't reset all L/S CLKx output)



Application for 2-In 8-Out waveforms

LS_CLKO_PH(0x04 [1:0] = 10 : 8 phase; CLK9 to 10 still do discharge at power-off)

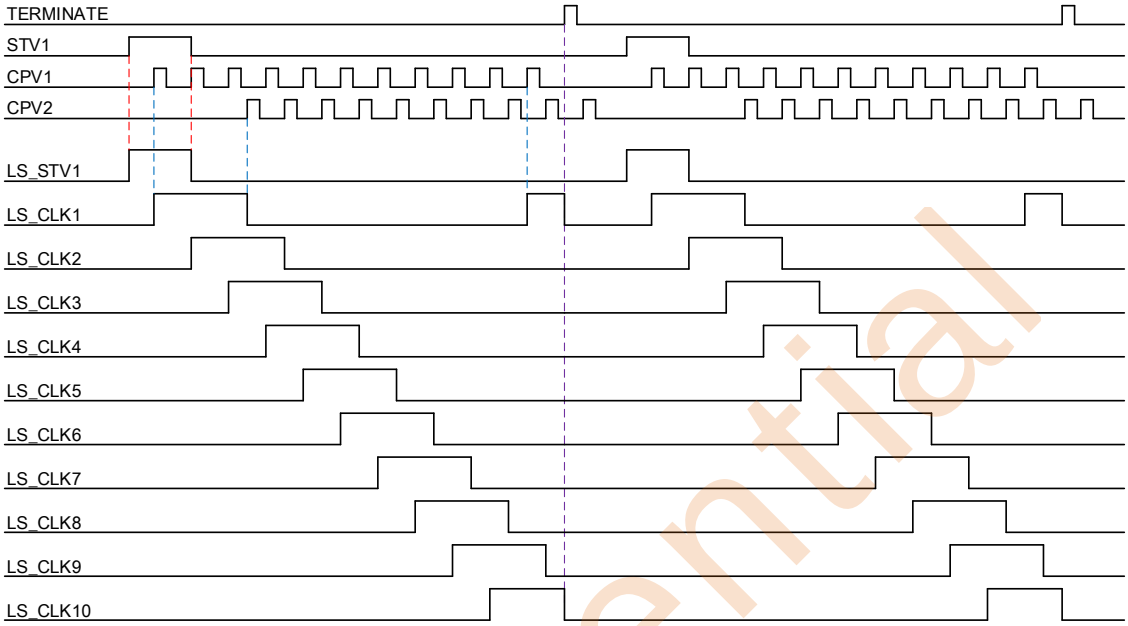
STV1_RST(0x04 [2] = 1 Reset all L/S CLKx output to LVGL)



Application for 2-In 10-Out waveforms

LS_CLKO_PH(0x04 [1:0] = 11 : 10 phase)

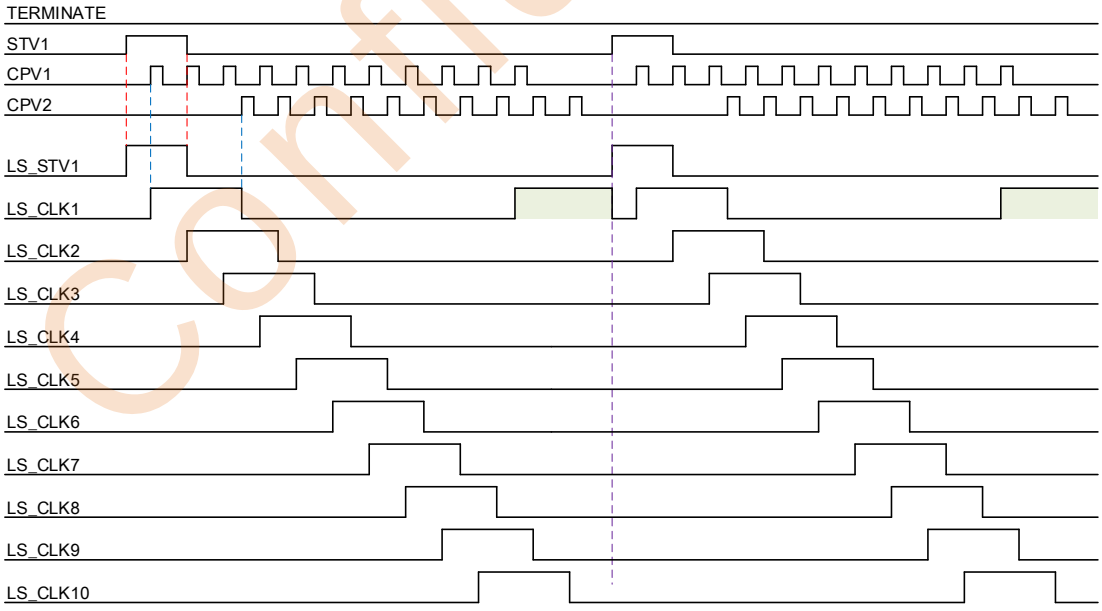
STV1_RST(0x04 [2] = 0 Don't reset all L/S CLKx output, terminate control CLKx output pull LVGL)



Application for 2-In 10-Out waveforms

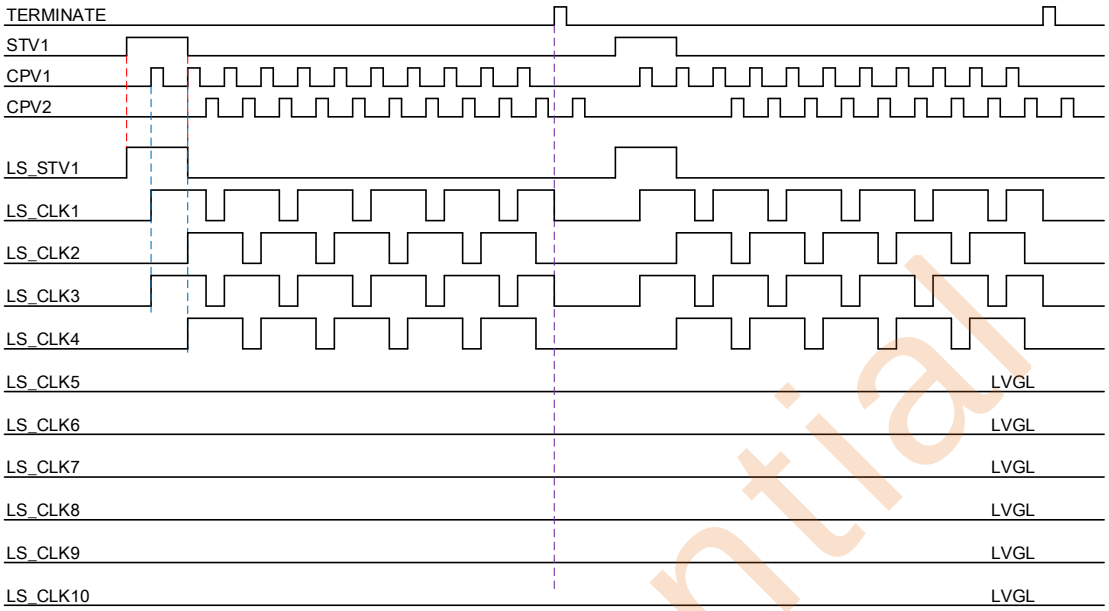
LS_CLKO_PH(0x04 [1:0] = 11 : 10 phase)

STV1_RST(0x04 [2] = 1 Reset all L/S CLKx output to LVGL)



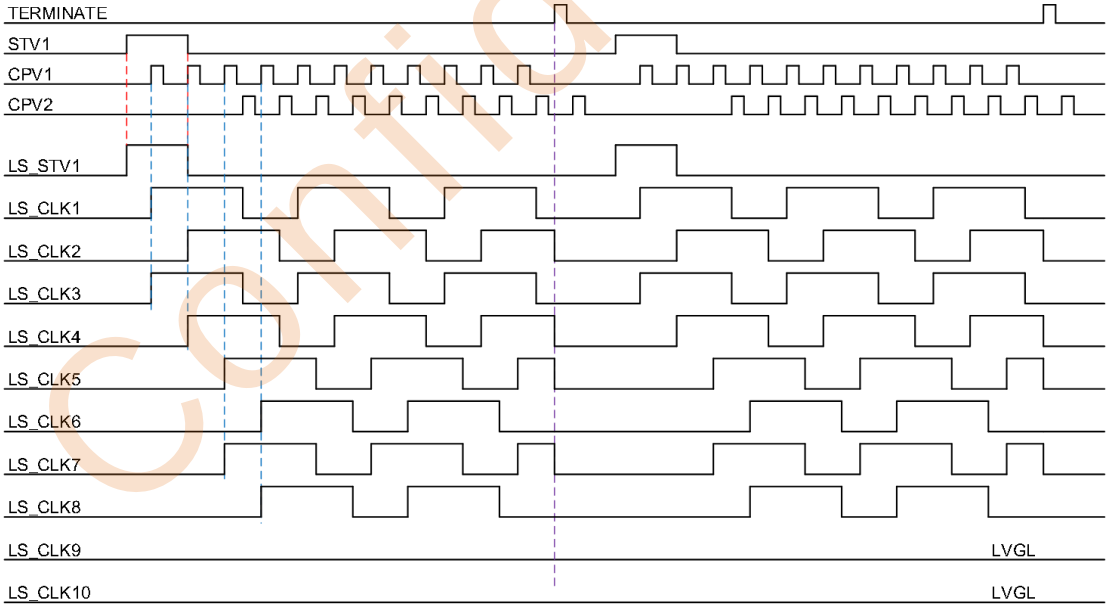
Application for 2line mode 2-in 4-out waveforms

LS_CLKO_PH(0x04 [1:0] = 00: 4 phase 2Line Mode)



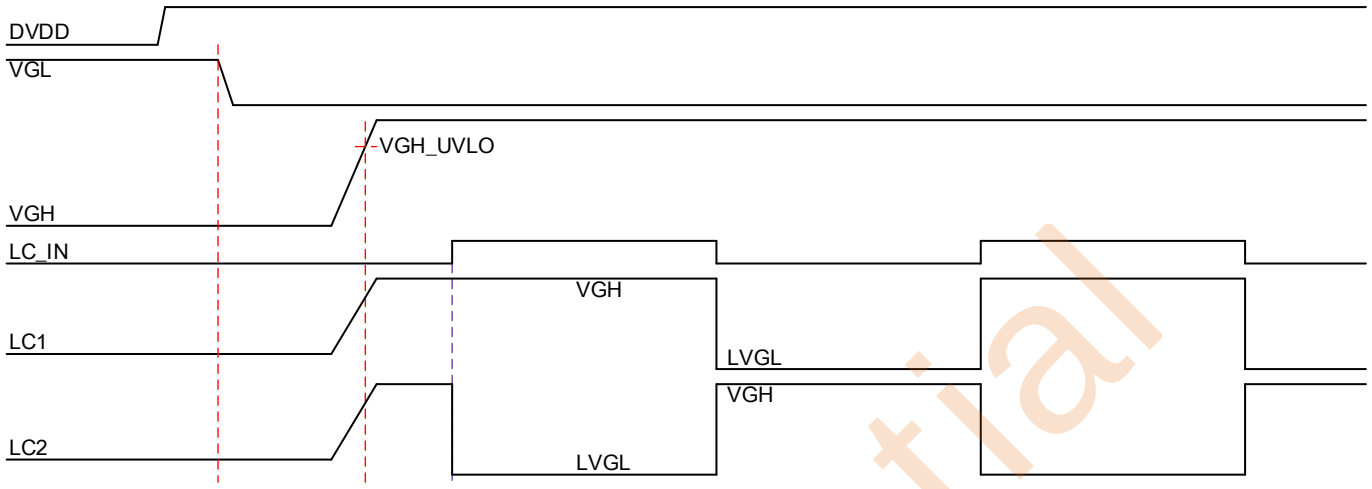
Application for 2line mode 2-in 8-out waveforms

LS_CLKO_PH(0x04 [1:0] = 10: 8 phase 2Line Mode)

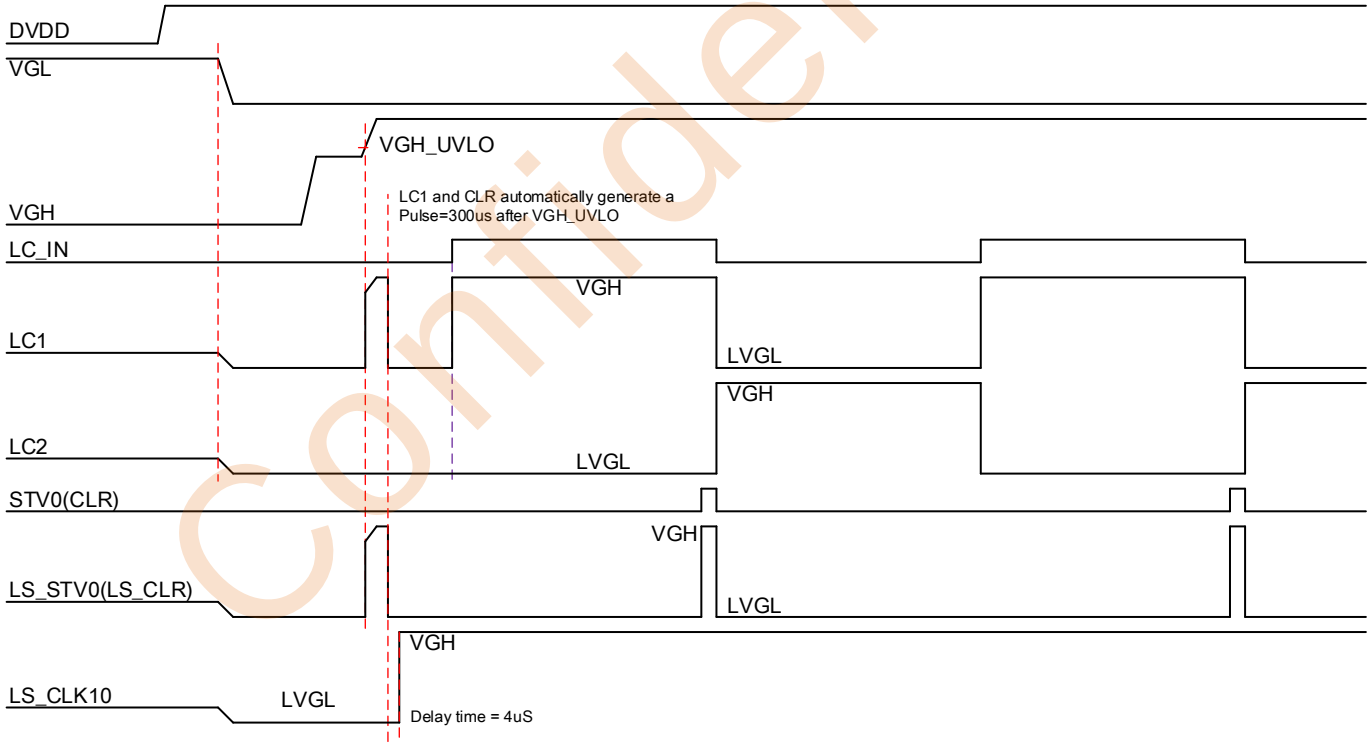


Application for LC Power ON Condition

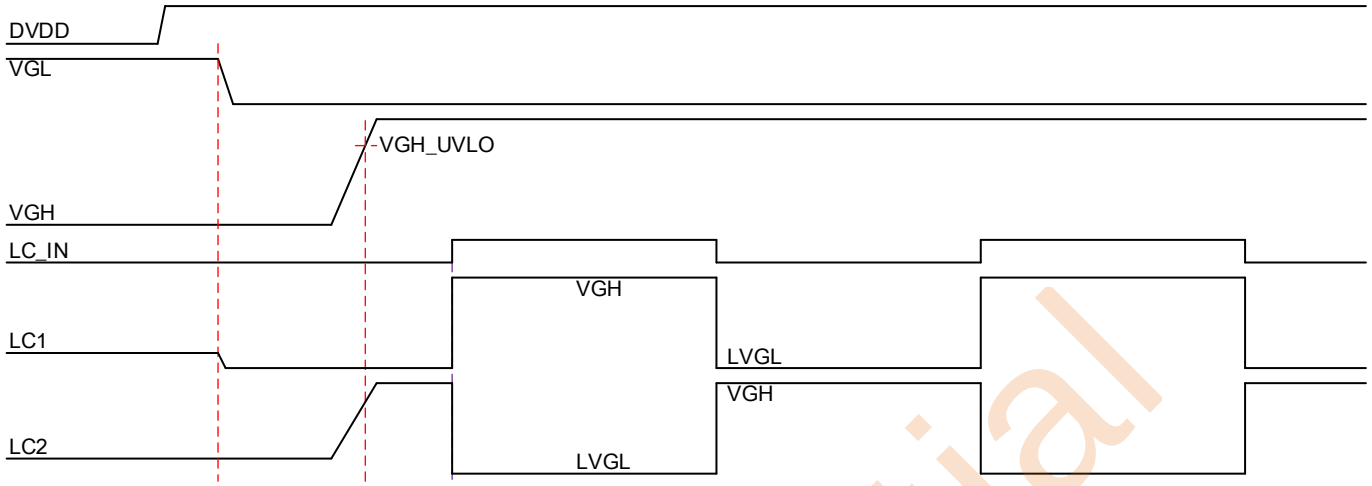
LC PON (0x05 [4:3] = 00 MODE1)



LC PON (0x05 [4:3] = 01 , MODE2)

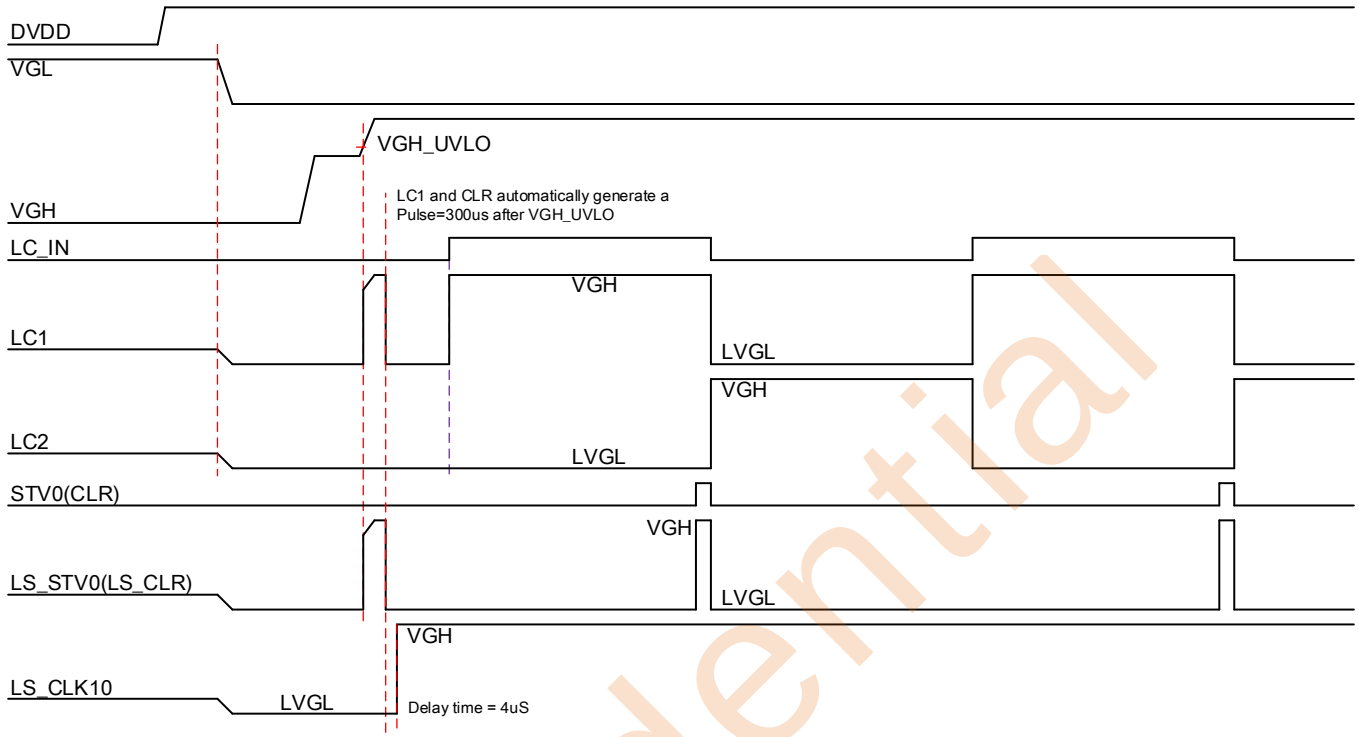


LC PON (0x05 [4:3] = 10/11 MODE3)

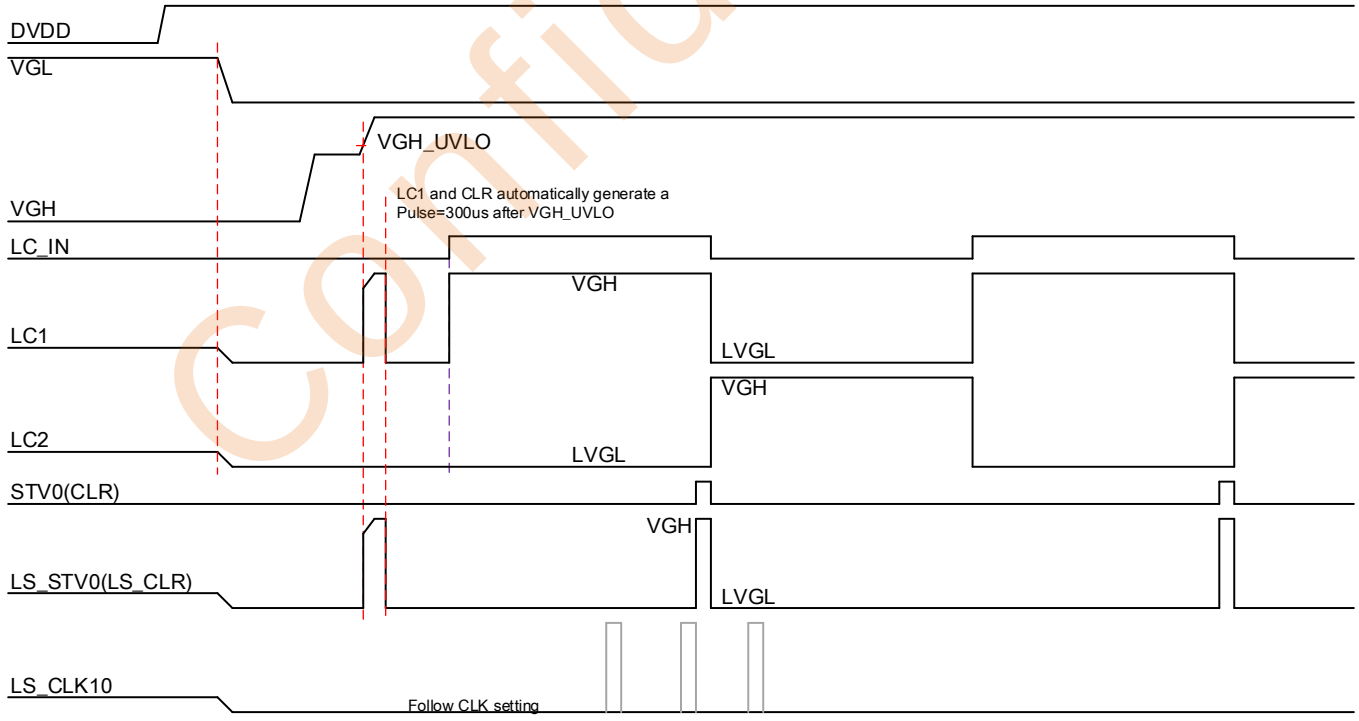


Application for Auto Pulse Function

AUTO PULSE ON (0x05 [1] = 1 Auto Pulse Function Enable, 0x04 [7] = 1 Enable VGH_O)



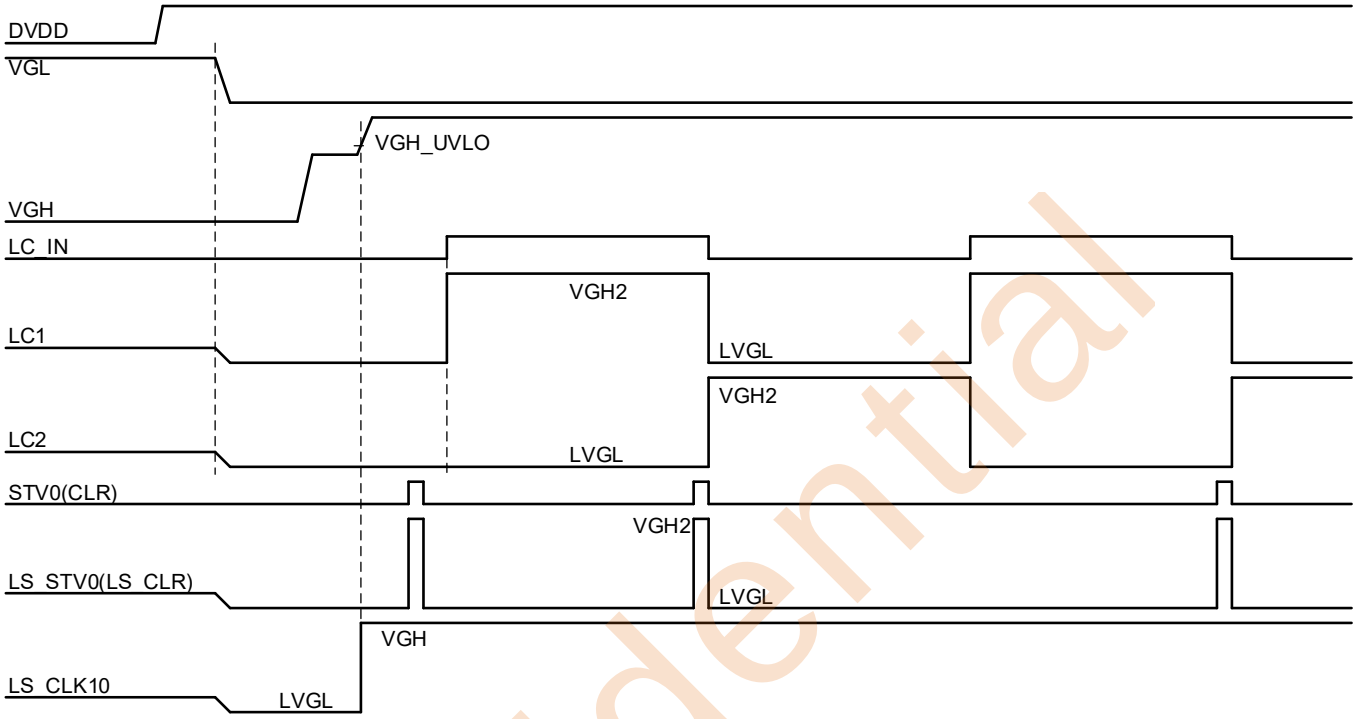
AUTO PULSE ON (0x05 [1] = 1 Auto Pulse Function Enable, 0x04 [7] = 0 Disable VGH_O)



CLKO_10 Follow VGH OUT (VGH>UVLO_R)

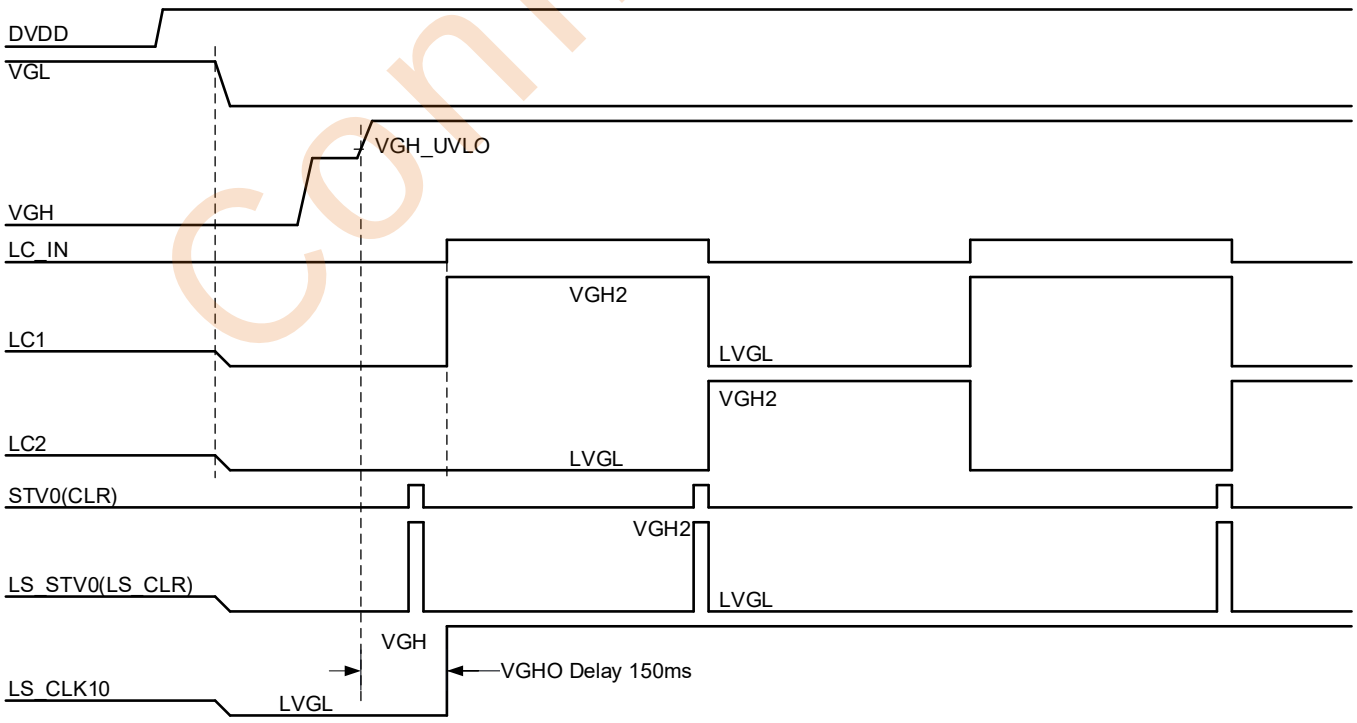
AUTO PULSE OFF (0x05 [1]= 0 Auto Pulse Function Disable)

CLKO_10 Follow VGH OUT (VGH>UVLO(R)) (0x04 [7] = 1 Enable 0x05 [6] = VGHO_DLY = 0ms)



AUTO PULSE OFF (0x05 [1] = 0 Auto Pulse Function Disable)

CLKO_10 Follow VGH OUT (VGH>UVLO(R)) (0x04 [7] = 1 Enable 0x05 [6] =1 VGHO_DLY=150mS)



IIC Command

Device Slave Address (0x52h)

MSB							LSB
0	1	0	1	0	0	1	R/W

Read Address	Write Address
01010011(53h)	01010010(52h)

1. Write single byte of data to DAC register

Start	01010010(Slave ID)	Slave ACK	00000011(Register)	Slave ACK	D7-D0(Data 03h)	Slave ACK	Stop

2. Write multiple byte of data to DAC register

Start	01010010(Slave ID)	Slave ACK	00000010(Register)	Slave ACK	Data 02h	Slave ACK

Data 03h	Slave ACK	Data 04h	Slave ACK	Data 05h	Slave ACK	Stop

3. Read single byte of data to DAC register

Start	01010010 (Slave ID)	Slave ACK	00000010 (Data Address)	Slave ACK	Start	01010011 (Slave ID)	Slave ACK	Data 02h	Master ACK	Stop

4. Read multiple byte of data to DAC register

Start	01010010(Slave ID)	Slave ACK	00000010(Data Address)	Slave ACK

Start	01010011(Slave ID)	Slave ACK	Data 02h	Master ACK	Data 03h	Master ACK

Data 04h	Master ACK	Data 05h	Master NACK	Stop

5. Write DAC data to OTP

Start	01010010(Slave ID)	Slave ACK	00000000(Control REG)	Slave ACK	10100101(Control Data)	Slave ACK	Stop

Register Map:

Device address (0x52h)

Address	Name	Description	Default value	Note
00h	Control Byte	0x00=A5 -->Write Register to E-fuse (0x02h to 0x05h) 0x00=A4-->Download E-fuse to Register (0x02h to 0x05h)		
01h	Read Only	000 : E-fuse don't write 001 : E-fuse write 1 time 010 : E-fuse write 2 times 011 : E-fuse write 3 times 100 : E-fuse write 4 times 101 : E-fuse write 5 times 110 : E-fuse write 6 times	00000 /000	E-fuse have been written 6 times. If Register Data=110, E-fuse can't be written and keep 6th data.

Register Map:

Device address (0x52h)

Address	Name	Description	Default value	Range
02h (**64h**)	CLKO_OCPTH	[2:0] CLKx_O OCP Threshold	100	000: disable 001: 30mA 010: 50mA 011: 70mA 100: 90mA 101: 120mA 110: 160mA 111: 200mA
	STV_LC_DIS_OCPTH	[5:3] STV0/1,LC1/2 LS_VGL,LS_LVGL OCP Threshold	100	000: disable 001: 30mA 010: 50mA 011: 70mA 100: 90mA 101: 120mA 110: 160mA 111: 160mA
	CLKO_OCPDC	[7:6] CLKx_O OCP Detect Count	01	00: 4 times 01: 8 times 10: 16 times 11: 32 times
03h (**10h**)	CLKO_OCPDT	[2:0] CLKx_O/LS_STV0/LS_STV1 OCP Detect Time	000	000: 2uS 001: 4uS 010: 6uS 011: 8uS 100: 10uS 101: 12uS 110: 14uS 111: 16uS
	STV_DIS_OCP DC	[3] STV0/1,LS_VGL,LS_LVGL OCP Detect Count	0	0: 4 time 1: 16 time
	XAO_SENSE	[5:4] XAO_SENSE	01	SEL_XAO_SENSE = 0 (Detect from DVDD pin) 00: 2.3V 01: 2.5V 10: 2.7V 11: 2.9V SECL_XAO_SENSE = 1 (Detect from XAO_SENSE pin) 00: 1.0V 01: 1.5V 10: 2.0V 11: 2.5V
	CLKO_SR	[7:6] CLKx_O Slew Rate	00	00: 100% (1000V/us) 01: 70% (700V/us) 10: 40% (400V/us) 11: 10% (100V/us)

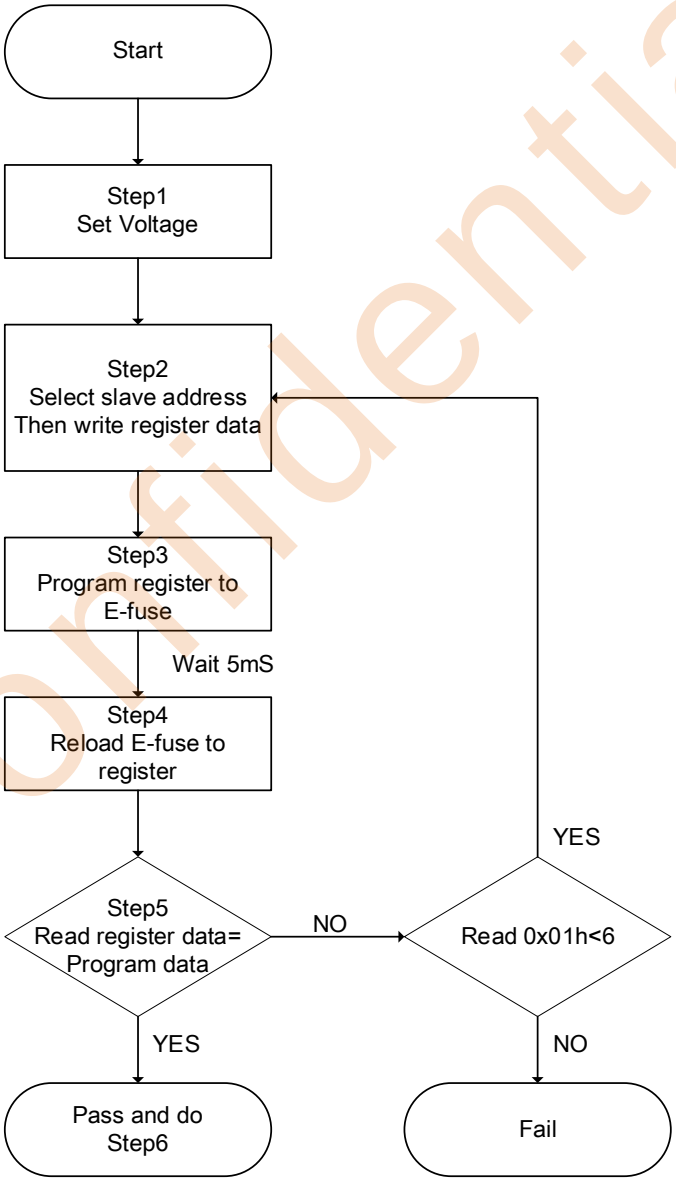
Register Map:

Device address (50h/52h)

Address	Name	Description	Default value	Range
04h (**47h**)	CLKO_PH	[1:0] CLKx_O Output Phase No.	11	00: 4 phase 01: 6 phase 10: 8 phase 11: 10 phase Note:(10 phase just only @04h,bit7=0)
	STV1_RST	[2] STV1 reset select	1	0: Don't reset all L/S output 1: Reset CLKx_O to LVGL
	STV1_POFF	[3] LS_STV1 Power Off condition	0	0: Output keeps LVGL 1: Output keeps VGH until VGH<POR. Output pulls LVGL
	STV0_POFF	[4] LS_STV0 Power Off condition	0	0: Output keeps LVGL 1: Output keeps VGH until VGH<POR. Output pulls LVGL
	LS_LVGL_POFF	[5] LS_LVGL Power Off condition	0	0: Output keeps LVGL 1: Output keeps VGH until VGH<POR. Output pulls LVGL
	CLK_LC_POFF	[6] CLKx and LC1/LC2 Power Off condition	1	0: Output keeps LVGL 1: Output keeps VGH until VGH<POR. Output pulls LVGL
	CLKO_10 VGHO OUT	[7] CLKO_10 Output VGHO	0	0: Normal 1: CLKO_PH only setting 4、6、8。CLKO_10 Output VGH VGH>UVLO(R)
05h (**00h**)	SEL_XAO_SENSE	[0] SEL_XAO_SENSE	0	0: Detect from DVDD Voltage 1: Detect from XAO_SENSE Voltage
	LS_STV0/LS_LC1 AUTO PULSE	[1] LS_STV0 and LS_LC1 Auto Pulse Function	0	0: Disable 1: Enable(with 300us) & VGHO delay time=4us(@ 04h,bit7=1,05h bit6=0)
	VGH2_UVLO_R	[2] VGH2_UVLO_R setting	0	0: 15V 1: 7V
	LC PON	[4:3] LS LC1/2 Power On Condition	00	00: MODE1 01: MODE2 10: MODE3
	CLK MODE setting	[5] CLK 1 Line or 2 Line Mode setting	0	0: 1 Line Mode 1: 2 Line Mode
	VGHO Delay Time	[6] VGHO output delay time setting	0	0: 0ms 1: 150ms
	FAULT/SYNC_XON	[7] FAULT/SYNC_XON pin select	0	0: FAULT function 1: SYNC_XON function

E-fuse Program Flow:

- Step1: DVDD = 3.3V → LVGL = VGL = -6V → VGH = 20V.
- Step2: Select Slave Address: 0x52, then write register (0x02h~0x05h) data.
- Step3: Program register to E-fuse: 0x00h = 0xA5.
- Step4: Reload E-fuse: 0x00h = 0xA4.
- Step5: Check register(0x02h~0x05h) data with writing code :
  If register (0x02h~0x05h) data is the same with writing code --> successfully written
  If register (0x02h~0x05h) data isn't the same with writing code --> Repeat Step2~5
  (Note: IC can't program over 6 times)
- Step6: VGH = 0V → LVGL = VGL = 0V → DVDD = 0V.



General Description

The LP6296B provides 16-channel Level Shifter designed to drive the GOA panel. This device converts the logic-level signals generated by the Timing Controller (TCON) to high-level signals required by GOA panel.

Protection

The LP6296B implies Over-Temperature Protection (OTP), Over-Current Protection (OCP). The following table shows the main behavior of each protection.

Function / Protection	Output	FAULT	Recovery
OTP	Hi-Z	Pull low	Tj decrease 20°C (Typ.) and STV rising
OCP	Hi-Z	Pull low	DVDD<UVLO_F

IC FAULT Function

During normal operating, FAULT pin becomes high-state. OTP or OCP happen, the FAULT pin becomes low-state.

Over Temperature Protection (OTP)

An Over-Temperature Protection (OTP) is equipped to prevent LP6296B from overheating due to the excessive power dissipation. The OTP will stop operating while junction temperature exceeds 150°C (Typ.). All of output channel start operating while the decrease of junction temperature approximately 20°C (Typ.).

Over Current Protection (OCP)

The LP6296B can detect output pins (STV1 to 2, CLK1 to 10, LC1 to 2, DIS_VGL, DIS_LVGL) short to each other short current. If the pin to pin short current over limit, the IC all outputs (STV0 to 1, CLK1 to 10, LC1 to 2, LS_VGL, LS_LVGL) will pull high impendence state. After DVDD<UVLO_F, IC recovers again.

CLK OCP Protection

When the CLK current exceeds the set OCP current Level, start timing. During Detect time duration, the CLK current value is higher than the set OCP current Level value, IC determines OCP and counts once; after the continuous count reaches OCP Count, IC performs OCP protection.

STV0/STV1 OCP Protection

When the STV0/STV1 current exceeds the set OCP current Level, start timing. During Detect time duration, the STV0/STV1 current value is higher than the set OCP current Level value, IC determines OCP and counts once; after the continuous count reaches OCP Count, IC performs OCP protection.

LC1/LC2 OCP Protection

The LC signal period is 4-6s, in a period of LC_IN, the current value exceeds the set OCP current at any time, and lasts for 40us, namely, the OCP is determined, the IC for OCP protection.

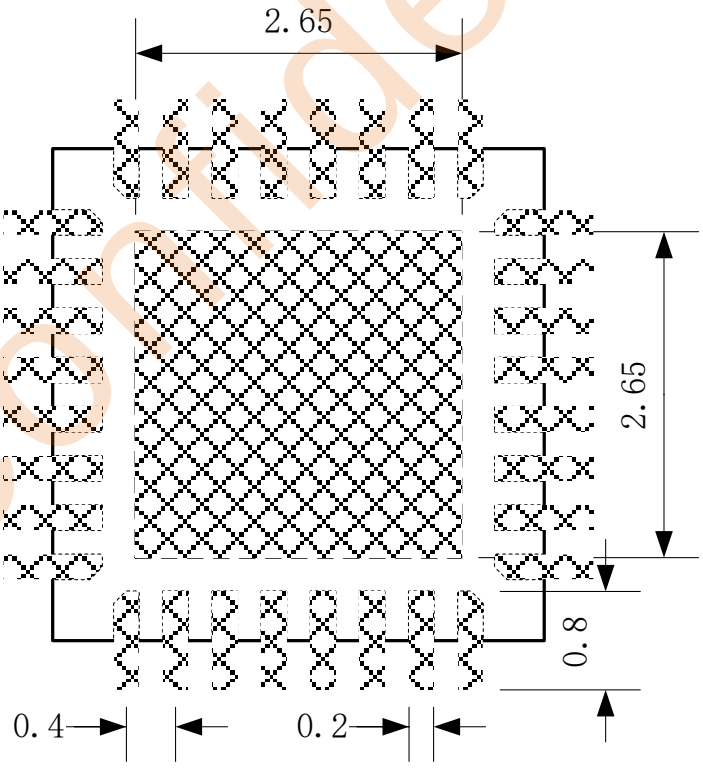
Power ON Sequence

When the DVDD exceeds UVLO, the internal signal ENA for condensed GOA logic will be high. The outputs of Level Shifter LS_CLK1~LC_CLK10, LS_VGL and LS_LVGL should follow LVGL level since DVDD exceeds UVLO. The outputs of Level Shifter STV1 and STV0 should follow LVGL level since DVDD exceeds UVLO. The outputs of Level Shifter LC1 and LC2 should follow LC_IN transient one VGH the other LVGL since DVDD exceeds UVLO. After ENA high, CLK1 to CLK10 do not output until receiving the first STV1 rising edge.
According to GOA circuit experience, it is recommended that
1. LC1 and LC2 start to work earlier than the 1st STV1 by 28us.
2. Logic signal (STV_IN1 to 2, LC_IN, CLK_IN1 to 2) must be sent after VGH power ready.
3.The recommended power-on sequence is DVDD → LVGL → VGL → VGH or DVDD → VGL = LVGL → VGH.
The concern of IC design is focus on VGL and LVGL ESD diode. The most negative voltage must be ready before the other negative voltage.

Layout Consideration

- The DVDD input capacitor should be closed the chip.
- The XAO_SENSE input capacitor should be closed the chip.
- The VGH1/2 input capacitor should be closed the chip.
- The VGL input capacitor should be closed the chip.
- The LVGL input capacitor should be closed the chip.
- The exposed pad of the chip should be connected to ground plane for thermal consideration.

Minimum Footprint PCB Layout Section



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Power on logic Table:

0x05h[0]=0,XAO sense detect DVDD pin:

CASE	Analog Power Input			Logic Input				Analog Output					
	DVDD	VGH2	XAO_ Detect	STV1	STV0	CPV1 CPV2	LC_IN	LS_STV 1	LS_STV 0	LS_CLK 1~10	LS_LC1, 2	LS_VGL	LS_LVG L
1	>UVLO	>UVLO	>2.5+HYS	w/i	w/i	w/i	w/i	Normal	Normal	Normal	Normal	VGL	LVGL
2	>UVLO	>UVLO	>2.5+HYS	w/i	w/o	w/o	w/i	Normal	LVGL	LVG	Normal	VGL	LVGL
3	>UVLO	>UVLO	>2.5+HYS	w/o	w/i	w/i	w/i	LVGL	Normal	LVGL	Normal	VGL	LVGL
4	>UVLO	>UVLO	>2.5+HYS	w/i	w/o	w/i	w/o	Normal	LVGL	Normal	VGH/LVGL (Reg.)	VGL	LVGL
5	>UVLO	>UVLO	>2.5+HYS	w/o	w/i	w/i	w/o	LVGL	Normal	LVGL	VGH/LVGL (Reg.)	VGL	LVGL
6	>UVLO	>UVLO	<2.5+HYS	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	VGH/LVGL (Reg.)	VGL	LVGL
7	>UVLO	<UVLO	>2.5+HYS	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	VGH/LVGL (Reg.)	VGL	LVGL
8	<UVLO	>UVLO	>2.5+HYS	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
9	<UVLO	>UVLO	<2.5+HYS	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL

Table 1. Power on (from 0 to DVDD)

Power off logic Table:

CASE	Analog Power Input			Logic Input				Analog Output					
	DVDD	VGH2	XAO_ Detect	STV1	STV0	CPV1 CPV2	LC_IN	LS_STV 1	LS_STV 0	LS_CLK 1~10	LS_LC1 ,2	LS_VGL	LS_LVG L
1	>UVLO	>UVLO_F	<2.5V(SET)	Don't care	Don't care	Don't care	Don't care	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH1	VGH/LVGL (Reg.)
2	<UVLO	>UVLO_F	Don't care	Don't care	Don't care	Don't care	Don't care	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH	VGH/LVGL (Reg.)
3	<UVLO	<UVLO_F >POR	Don't care	Don't care	Don't care	Don't care	Don't care	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH/LVGL (Reg.)	VGH	VGH/LVGL (Reg.)
4	<UVLO	<POR	Don't care	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL
5	>UVLO	<UVLO_F	>2.5V(SET)	Don't care	Don't care	Don't care	Don't care	LVGL	LVGL	LVGL	LVGL	VGL	LVGL

Packaging Information

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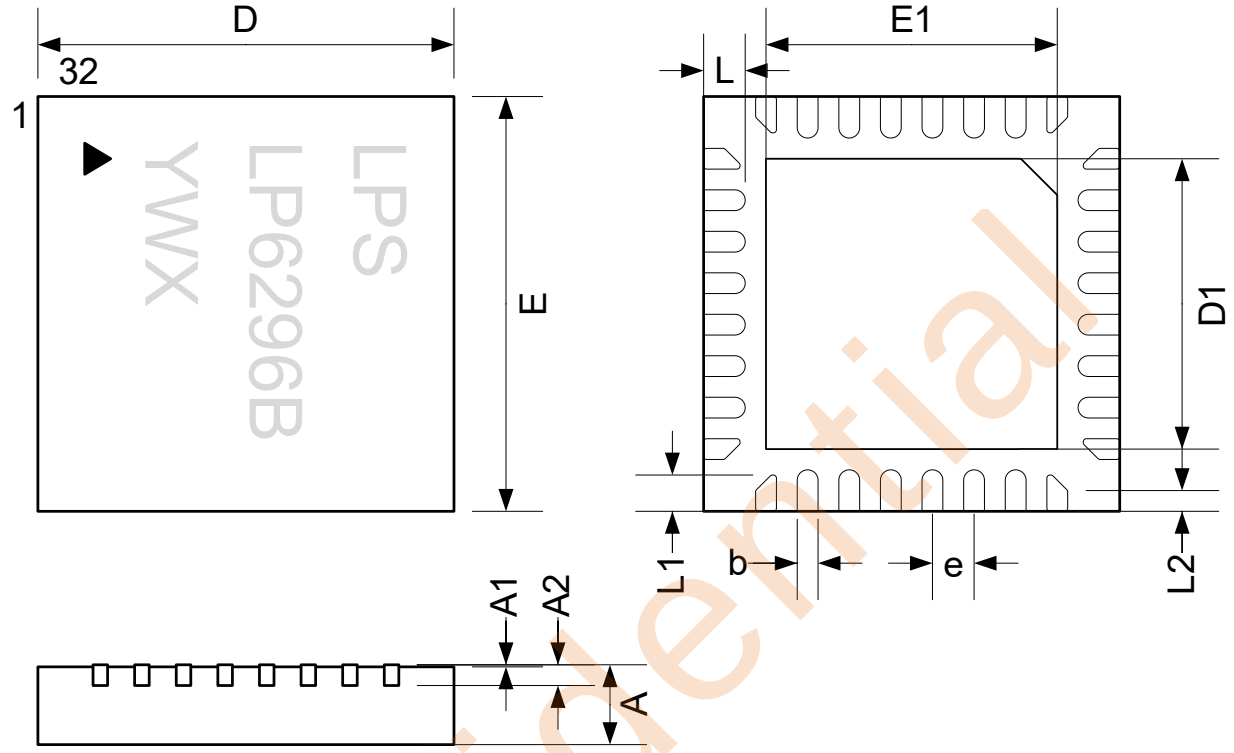

Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	3.95	4.00	4.05	0.1555	0.1575	0.1594
E	3.95	4.00	4.05	0.1555	0.1575	0.1594
D1	2.65	2.70	2.75	0.1043	0.1063	0.1083
E1	2.65	2.70	2.75	0.1043	0.1063	0.1083
b	0.15	0.20	0.25	0.0059	0.0079	0.098
e	0.40 BSC			0.0157 BSC		
L	0.35	0.40	0.45	0.0138	0.0157	0.0177
L1	0.30	0.35	0.40	0.0118	0.0138	0.0157
L2	0.15	0.20	0.25	0.0059	0.0079	0.098

Revision History

Revision	Date	Change Description
Rev 0.1p0	03/25/2024	Product Brief
Rev 0.2p18	04/09/2024	2 line mode output waveform
Rev 0.3p5	06/03/2024	Add θ_{JA}
Rev 0.4p5	06/17/2024	Add θ_{JC}
Rev 0.5p22	06/18/2024	CLK10 follow waveform
Rev 0.6p30	12/12/2024	Chip height A MAX described error