

## Features

- DiSEqC 1.x compatible
- Non-synchronous boost converter
  - 8.5~16V input voltage range
  - 1-MHz switching frequency
  - Improve efficiency in light-load
- Low noise linear regulator output (LNB)
  - Up to 600mA current capability
  - Fixed 1.2V low drop-out
  - 14V/19V output voltage
  - 700mV Vp-p ( $\pm 350$ mV) 22-KHz tone with fast rise/fall time (8 $\mu$ s)
    - Push-pull LNB output
- Integrated UVLO, OCP, SCP, and OTP protections
- Packaging
  - ESOP-8 package
  - RoHS Compliant and Halogen Free
  - 100% Lead (Pb) Free

## Applications

- STB (Set Top Box) Satellite Receiver
- TV Satellite Receiver
- PC Card Satellite Receiver

## General Description

Designed for analog and digital satellite receivers, the LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF is a monolithic voltage regulator to provide the 14V/19V power supply and the 22-kHz tone signaling to the LNB downconverter in the antenna dish or to the multi-switch box. It offers a complete solution with very low component count, low power dissipation together with simple design. The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF features high power efficiency. The boost converter runs at 1-MHz switching frequency. Drop out voltage at the linear regulator is 1.2-V to minimize power loss. LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF provides multiple ways to generate the 22-kHz signal. Integrated linear regulator with push-pull output stage generates clean 22-kHz tone signal superimposed at the output even at zero loading.

The boost converter supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF also integrates multiple protection functions, i.e., over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), and short circuit protection (SCP).

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF is available in an ESOP-8 package.

## Order Information

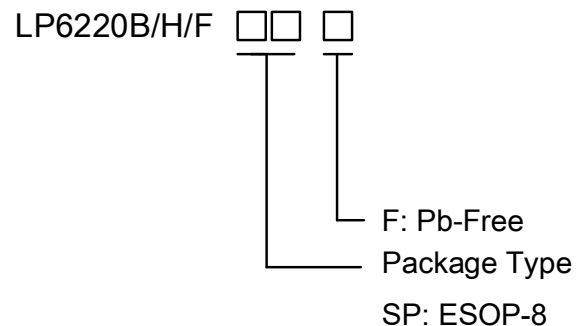


Figure 1 Order Information



## Device Information

Part Number	Top Marking	Package	LNB output voltage	MSL	Shipping
LP6220BSPF	LPS LP6220B YWX	ESOP-8	14V/19V	MSL3	4K/REEL
LP6220HSPF	LPS LP6220H YWX	ESOP-8	14.6V/19.4V	MSL3	4K/REEL
LP6220FSPF	LPS LP6220F YWX	ESOP-8	14V/19V	MSL3	4K/REEL
LP6220LSPF	LPS LP6220L YWX	ESOP-8	13.3V/18.3V	MSL3	4K/REEL

Marking indication: Y: Year code. W: Week code. X: Batch numbers.

Table 1. Device Information

## Typical Application

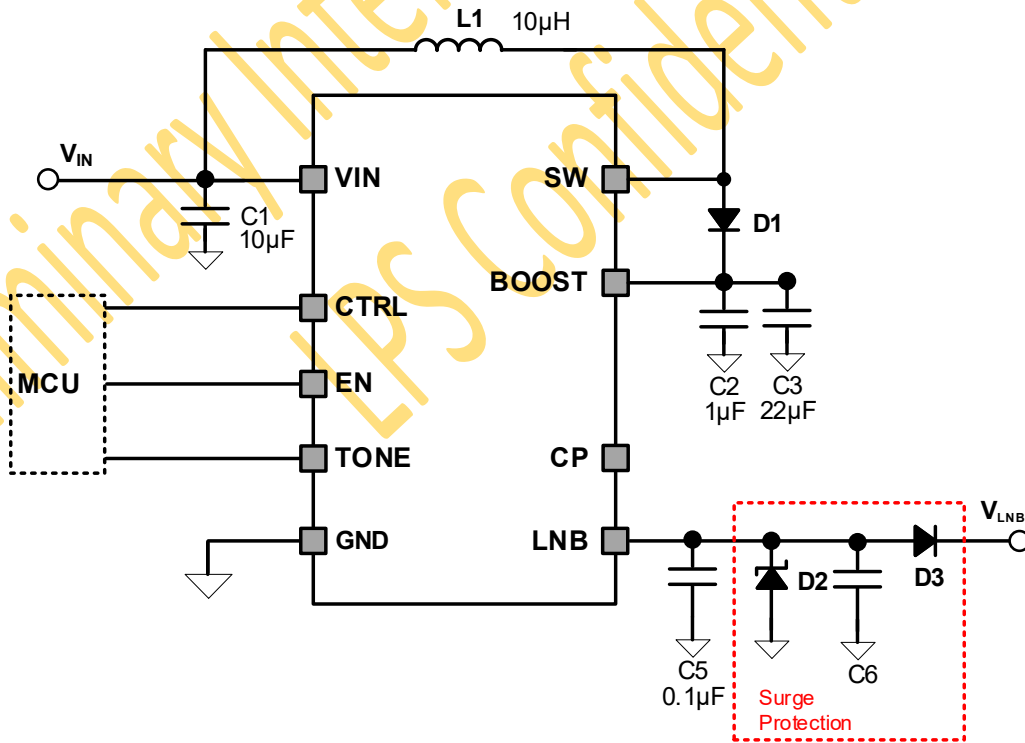


Figure 2 Typical Application Circuit



## Pin Diagram

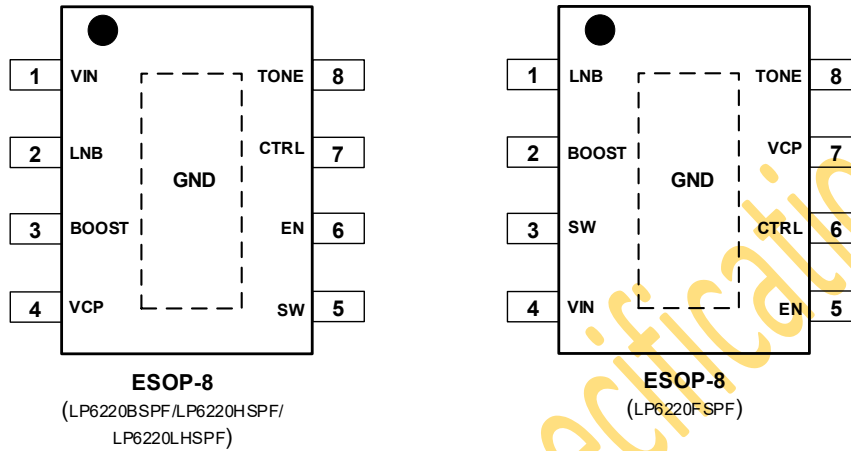


Figure 3 ESOP-8

## Pin Description

Part Number	Pin #	Name	I/O	Description
LP6220BSFP LP6220HSFP LP6220LSFP	1	VIN	Power	This is the input power for the internal linear regulator and boost converter.
	2	LNB	Power	Output of the LNB linear regulator. Connect this pin to satellite receiver or switch.
	3	BOOST	Power	Output of the boost converter and this is also the input of the charge pump and LNB linear regulator.
	4	VCP	-	No Connect
	5	SW	Power	Switching node of the boost converter.
	6	EN	I/O	Enable pin to enable the whole chip.
	7	CTRL	I/O	LNB output voltage selection: CTRL=0, LNB output 14V/14.6V; CTRL=1, LNB output 19V/19.4V.
	8	TONE	I/O	External tone logic input pin which activates the 22kHz tone output. Connect to low or high has no LNB modulation function.
	Thermal	GND	Ground	Ground.
LP6220FSFP	1	LNB	Power	Output of the LNB linear regulator. Connect this pin to satellite receiver or switch.
	2	BOOST	Power	Output of the boost converter and this is also the input of the charge pump and LNB linear regulator.
	3	SW	Power	Switching node of the boost converter.
	4	VIN	Power	This is the input power for the internal linear regulator and boost converter.
	5	EN	I/O	Enable pin to enable the whole chip.
	6	CTRL	I/O	LNB output voltage selection: CTRL=0, LNB output 14V; CTRL=1, LNB output 19V.
	7	VCP	-	No Connect
	8	TONE	I/O	External tone logic input pin which activates the 22kHz tone output. Connect to low or high has no LNB modulation function.
	Thermal	GND	Ground	Ground.

Table 2. Pin Description



## Absolute Maximum Ratings (Note)

VIN, SW, BOOST, LNB voltage to GND -----	-0.3V to 28V
EN, CTRL, TONE voltage to GND -----	-0.3V to 5.5V
CP voltage to BOOST -----	-0.3V to 5.5V
SW voltage to GND (20ns transient) -----	-5V to 28V
Operating Junction Temperature Range (TJ)-----	-40°C to 150°C
Maximum soldering temperature (at leads, 10 sec)-----	260°C

**Note:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD Ratings

HBM (Human Body Model) -----	+/-2kV
CDM (Charge Discharge Model) -----	+/-500V

## Thermal Information

$\theta_{JA}$ (Junction-to-Ambient Thermal Resistance) for ESOP-8 -----	65°C/W
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Preliminary Internal Specifications  
LPS Confidential



## Electrical Characteristics

(The specifications are at  $V_{IN}=12V$  and  $T_J=25^{\circ}C$  except otherwise specified.)

Symbol	Description	Conditions	Min	Typ.	Max	Units
<b>POWER SUPPLY</b>						
$V_{IN\_UVLO\_RISE}$	Under voltage lockout of $V_{IN}$	$V_{IN}$ rising threshold	7.7	8.0	8.3	V
$V_{IN\_UVLO\_FALL}$	Under voltage lockout of $V_{IN}$	$V_{IN}$ falling threshold	7.2	7.5	7.8	V
$I_{Q\_VIN}$	Input quiescent current at $V_{IN}$ pin	EN=1, TONE=0, VLNB=19V		3.5		mA
		EN=1, TONE=22K, VLNB=19V		4.7		mA
$I_{Q\_SD}$	Input shutdown current	$V_{EN}=0V$		100		$\mu A$
<b>LNB Regulator</b>						
$V_{CC}$	LDO output voltage	VLNB=14/19V, $T_J=25^{\circ}C$	-1.5%		+1.5%	V
$V_{RIPPLE}$	Ripple and noise on LNB	20MHz BW, VLNB=14V/19V, 0~600mA		40		mV
$R_{DSON}$	LDO Source FET on-resistance			0.7	1.0	$\Omega$
$I_{SOURCE}$	LDO source current limit	VLNB=14V*0.9 or VLNB=19V*0.9	600	700	800	mA
$V_{SCP\_RISE}$	Short circuit protection threshold	Rising		7.0		V
$V_{SCP\_FALL}$	Short circuit protection threshold	Falling Reference to VLNB target	6.0	6.5	7.0	V
$I_{SCP\_LIMIT}$	Short circuit current limit	Current limit after SCP	200	250	300	mA
$t_{on-hiccup}$	Hiccup on time [Note 1]	Not include the soft-time, VLNB is enabled and current limit time		10		ms
$t_{off-hiccup}$	Hiccup waiting time [Note 1]	VLNB is disabled time		2000		ms
<b>BOOST CONVERTER</b>						
$I_{LIM\_PEAK}$	Low-side peak current limit	$T_J=25^{\circ}C$		2.8		A
$F_{sw}$	Switching frequency	Default 1MHz		1		MHz
$D_{max}$	Maximum duty [Note 1]			80		%
<b>EN Logic and Soft-start</b>						
$V_H$	EN pin logic high threshold	EN Rising threshold	1.2			V
$V_L$	EN pin logic low threshold	EN Falling threshold			0.4	V
$T_{EN\_DEGLITCH}$	EN pin deglitch time			10		us
$I_{EN\_LEAK}$	EN Pin Input Leakage Current			4		$\mu A$
$t_d$	EN delay time [Note 1]	From EN high to LNB start		7.6		us
$t_{ss}$	Soft start time [Note 1]	From first switch to 90%* $V_{ref}$ ,		5		ms
<b>CTRL</b>						
$V_H$	CTRL pin logic high threshold	CTRL Rising threshold	1.2			V
$V_L$	CTRL pin logic low threshold	CTRL Falling threshold			0.4	V
$T_{DEGLITCH}$	CTRL pin deglitch time			10		us
<b>TONE</b>						
$V_H$	TONE pin logic high threshold	TONE Rising threshold	1.2			V
$V_L$	TONE pin logic low threshold	TONE Falling threshold			0.4	V
$F_{ton}$	Tone frequency range			22		kHz
$V_{TON\_PP}$	VLNB peak2peak amplitude when toning			700		mV
$T_{TONE\_RISE}$	VLNB rise time when toning			8		us
$T_{TONE\_FALL}$	VLNB fall time when toning			8		us



Symbol	Description	Conditions	Min	Typ.	Max	Units
ITONE_LEAK	TONE Pin Input Leakage Current			4		uA
<b>Thermal Protection</b>						
TOTP_RISE	Thermal shutdown threshold	Rising threshold		160		°C
TOTP_FALL	Thermal shutdown threshold	Falling threshold		130		°C

Table 3 Electrical Characteristics

Note 1: Not production tested. Guaranteed by design.

Preliminary Internal Specifications

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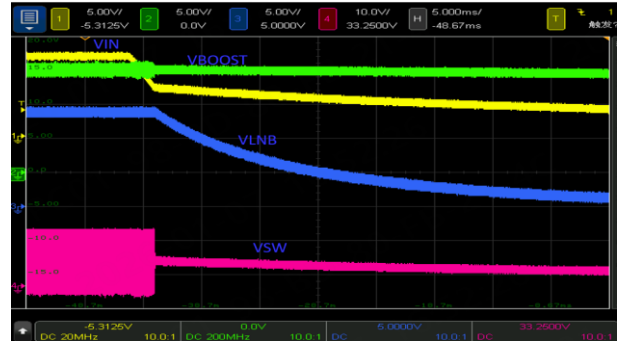


## Typical Characteristics

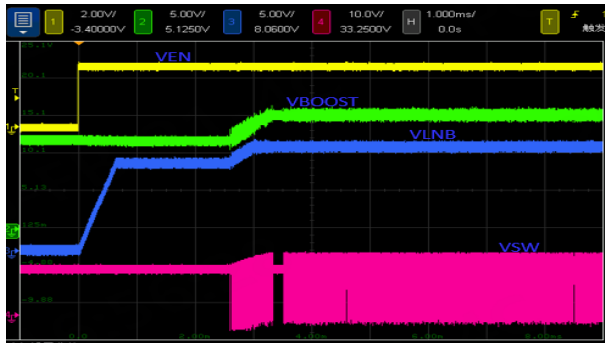
VIN=12V, Vout=19V, TA=25°C, unless otherwise noted.



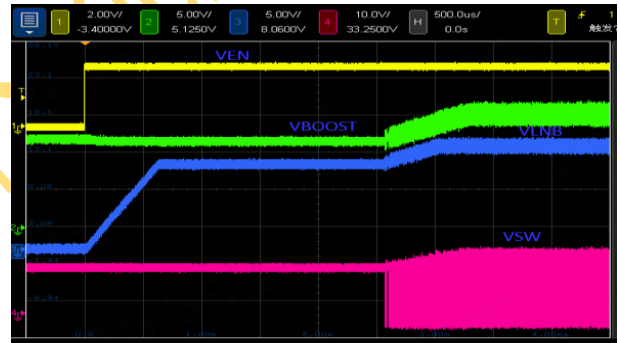
VIN=12V, EN=H, Power on with VIN



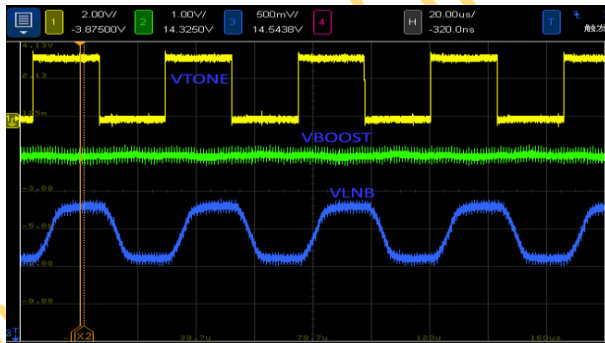
VIN=12V, EN=H, Power off with VIN



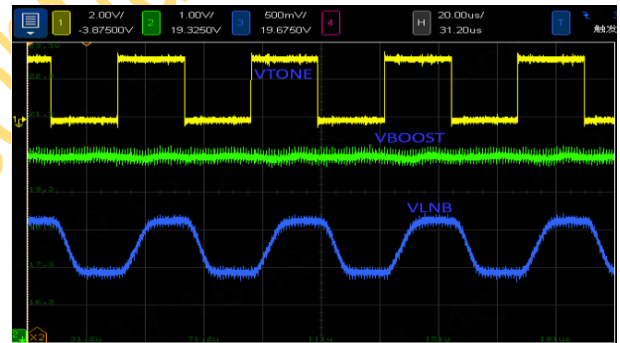
VIN=12V, EN=H, Power on with VEN, no load



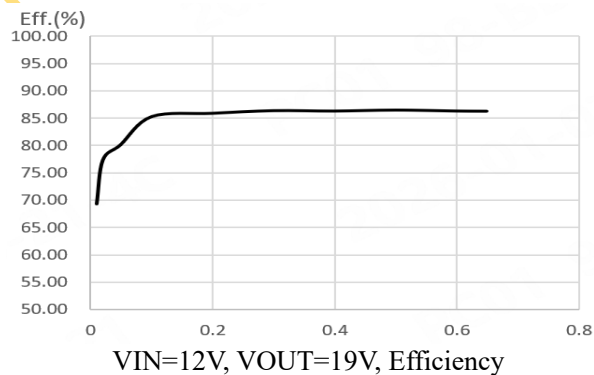
VIN=12V, EN=H, Power on with VEN, 51Ω load



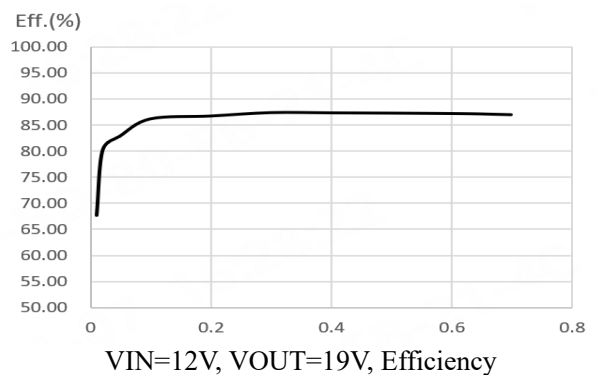
VIN=12V, TONE=22K, CTRL=L



VIN=12V, TONE=22K, CTRL=H



VIN=12V, VOUT=19V, Efficiency



VIN=12V, VOUT=19V, Efficiency





## Detailed Description

### Overview

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF is a monolithic voltage regulator to provide the 14V/19V power supply and the 22-kHz tone signaling to the LNB downconverter in the antenna dish or to the multi-switch box. It offers a complete solution with very low component count, low power dissipation together with simple design. The LP6220BSPF features high power efficiency. Drop out voltage at the linear regulator is 1.2V to minimize power loss. LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF provides multiple ways to generate the 22kHz signal. Integrated linear regulator with push-pull output stage generates clean 22kHz tone signal superimposed at the output even at zero loading.

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF also integrates multiple protection functions, i.e., over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), and short circuit protection (SCP).

### Under Voltage Lockout (VIN UVLO)

When the input voltage  $V_{IN}$  is lower than the  $V_{UVLO\_IN}$  threshold, all functions are shut down, the current into  $V_{IN}$  pin is less than 100 $\mu$ A. When the input voltage is higher than the  $V_{UVLO\_IN}$  rising threshold, the LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF can be enabled by the EN pin.

### Non-synchronous Boost Converter

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF integrates the peak current mode control scheme when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal oscillator block turns on the low-side MOSFET to start a switching cycle each cycle. The BOOST-pin voltage is divided internally and amplified by the error amplifier with a typical 1.2V reference voltage. Once the peak current of the inductor reaches the output voltage of the error amplifier, the LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF turns off the low-side MOSFET.

The boost converter tracks the LNB output voltage with a typical 1.2V voltage drop even at loading 600mA. Under conditions where the input voltage,  $V_{IN}$  is greater than boost output voltage ( $LNB+1.2V$ ), the boost converter stops switching and the LNB linear regulator drops the differential voltage. When operating in these conditions, care must be taken to ensure that the safe operating temperature range of the LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF is not exceeded. The boost converter operates at 1-MHz typical and has internal cycle-by-cycle current limit.



If two or more set top box LNB outputs are connected together, one output voltage could be set higher than others. The output with lower set voltage would be effectively turned off. Once the voltage drops to the set level, the LNB output with lower set output voltage returns to normal conditions.

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF implements a power save mode with pulse frequency modulation to improve efficiency at light load. When the load current decreases, the inductor peak current set by the output of the error amplifier declines to regulate the output voltage.

## LNB Linear Regulator

The linear regulator is used to generate the 22-kHz tone signal by changing the reference voltage (or resistor divider). The linear regulator features low drop out voltage to minimize power loss while keeps enough head room for the 700mV (V<sub>p-p</sub>), 22-kHz tone. It also implements a tight current limit for over current protection. The current limit is 700mA typically and the current limit drops to 250mA when SCP.

When LNB output voltage transits from 14V to 19V or vice versa by setting the CTRL pin from low to high or high to low, the output voltage of the boost converter follows the LNB voltage change.

In light load conditions (or no load), when LNB output voltage is set from 19V to 14V, the voltage might drop very slow, which might cause wrong logic detection at LNB side. The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF has the integrated a pull-down regulator to pull down the output during the transition. Meanwhile, when 22-kHz tone signal is superimposing on the LNB output voltage, the pull-down current can also provide square wave instead of a distorted waveform, which could cause another detection problem.

## Tone

A 22-kHz tone signal is superimposed at the LNB output voltage as a carrier for DiSEqC command. This tone signal can be generated by feeding an external 22-kHz clock at the TONE pin.

## EN Control and Soft Start

The EN pin is used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the V<sub>IN</sub> is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.2V typically), the LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF enables all the internal circuits, delays for t<sub>d</sub> time, and begins the soft-start.

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF integrates soft-start function with a typical time of t<sub>SS</sub>. After passing the UVLO threshold and enabled by the EN pin, the internal reference voltage ramps from zero to the 90%\*V<sub>ref</sub> in t<sub>SS</sub> and the output voltage ramps up accordingly. In this way, the inrush current is limited when big output capacitors are used.



The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF has a dedicated EN pin to disable and enable the LNB output. When the EN pin is pulled to high, the LNB output is enabled, when the EN pin is pull to low, the LNB output is disabled.

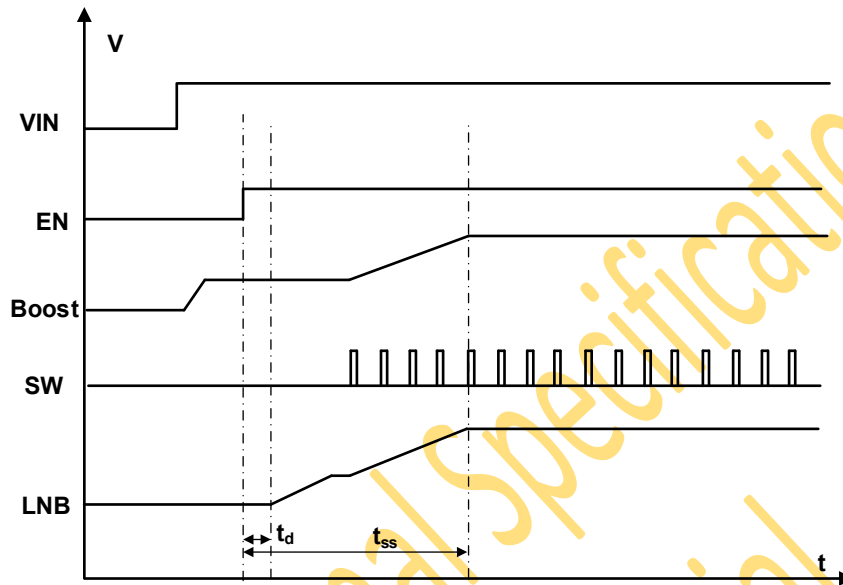


Figure 5. Soft Start Sequence

## Over Current Protection and Short Circuit Protection

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF protects an over current situation by limiting current of boost converter and LDO independently.

Boost Convert Current Limit:

The internal error amplifier output voltage of the boost converter is clamped when over current occurs. In this way, the inductor peak current is limited cycle by cycle. The current of high-side MOSFET is monitored all the time to sense the inductor peak current when the low-side MOSFET is turned on. The low-side MOSFET is turned off immediately if the peak current is higher than the COMP high clamp threshold, protecting the inductor current from further increasing.

Linear Regulator:

The LNB LDO has an internal current limit circuit that protects the regulator during transient high-load current faults or shorting events. The current limit is a brick-wall scheme. In a high-load current fault, the brick-wall scheme limits the output current to the current limit (700mA typically). The output voltage is not regulated when the device is in current limit. When a current limit event occurs, the device begins to heat up because of the increase in power dissipation. When the device is in brick-wall current limit, the pass transistor dissipates power. The SCP is realized by monitoring the LNB-pin voltage when the LDO current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the LNB voltage drops to 6.5 V and the current limit drops to 250mA. When SCP lasts for 10-ms, the LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF shuts down. The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF will restart after a typical 2000ms hiccup waiting time. If the SCP condition still holds after



soft-start (recovers to 700mA during soft start), the LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF shutdown again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

## Thermal Protection

The LP6220BSPF/LP6220HSPF/LP6220FSPF/LP6220LSPF has a thermal protection function. The device will shut down when the internal temperature is higher than 160°C and will restart after the temperature drops below 130°C.

## Application Information

### Design Requirements

The table 1 shows the design parameters for a typical 14/19V output voltage in the LNB application.

Parameter	Target
Input voltage range	12V typical, range: 8.5~16V
LNB Output voltage	14/19V
Load current	0~0.6A
Operating frequency	1MHz

Table 4 Design Parameters

### Inductor and Output Capacitor Setting

FSW	Inductor-L	Cboost1	Cboost2
1MHz	10μH typ. 6.8μH min 15μH max	1μF +22μF (MLCC) ESR=5mohm Effective capacitance: >5uF	1μF +100μF (Electrolytic) ESR-MLCC=5mohm ESR-Electrolytic=0.5 ohm Effective capacitance: 1μF +100μF

Table 5 Design Parameters



## PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

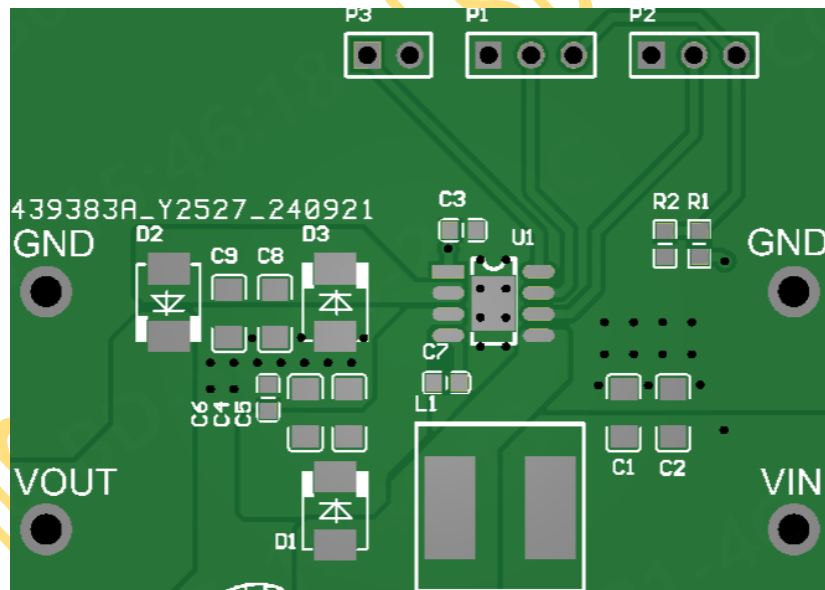
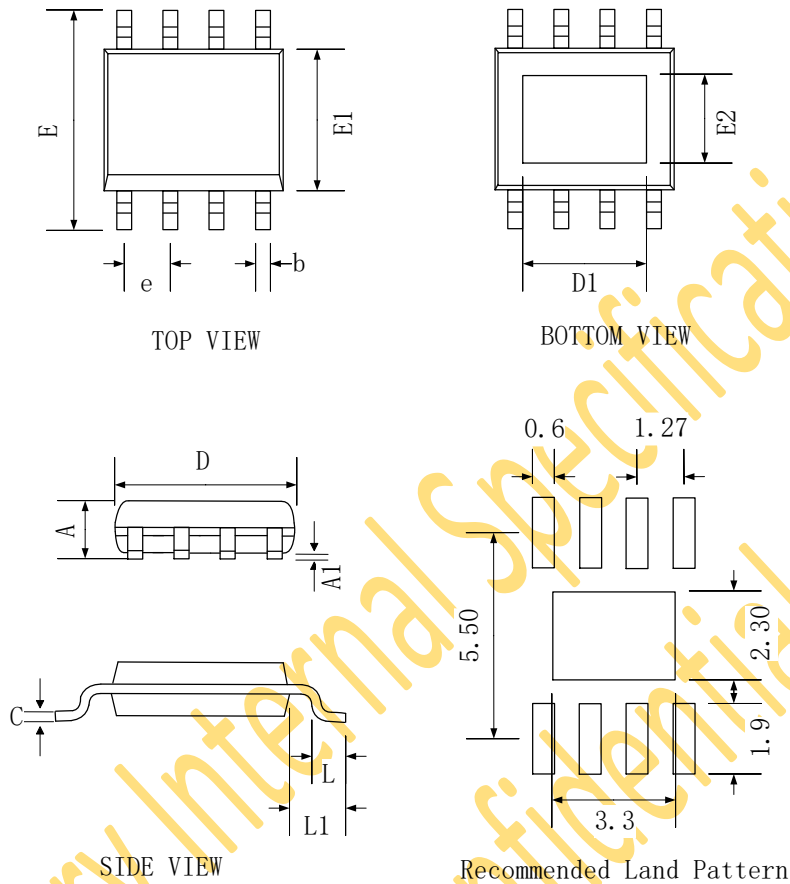


Figure 6. PCB layout



## Packaging Information

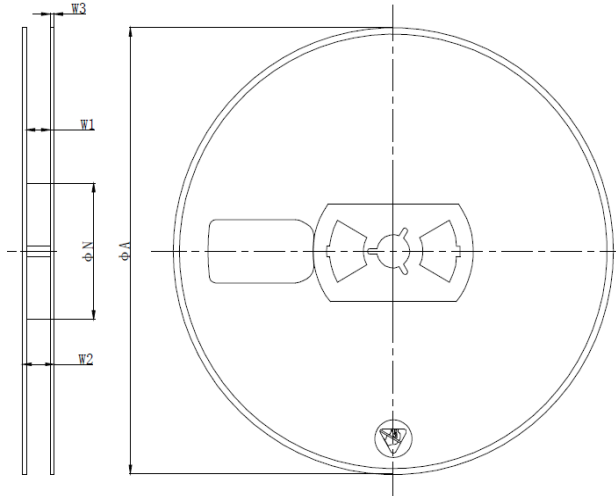


SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	1.35	-	1.75
A1	0.00	-	0.15
b	0.30	0.40	0.50
c	0.20 REF		
D	4.70	4.90	5.10
D1	3.2 REF		
E	5.70	6.00	6.30
E1	3.70	3.90	4.10
E2	2.30 REF		
e	1.27 BSC		
L	0.40	0.60	0.80
L1	1.05 REF		



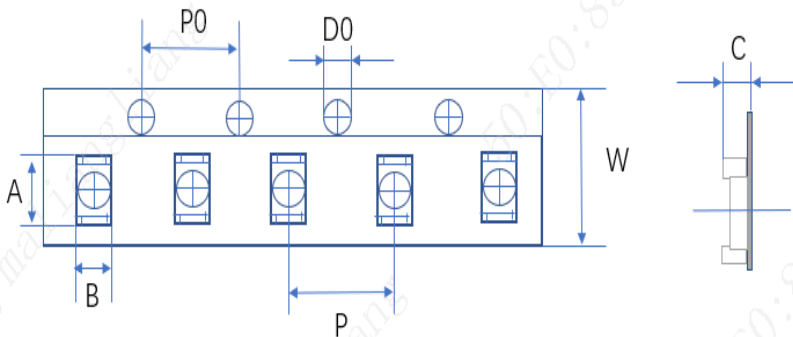
## Tape and Reel Information

### REEL DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	325.00	329.00	333.00
W2	15.00	17.00	19.00

### TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	6.20	6.60	7.00
B	5.10	5.50	5.90
P0	3.80	4.00	4.20
P	7.80	8.00	8.20
D0	1.30	1.50	1.70
W	11.90	12.00	12.30
C	1.90	2.10	2.30

### PIN1 AND TAPE FEEDING DIRECTION

