LP3995S

40V/500mA Low IQ High PSRR LDO

Features

- Wide Input Voltage Range: 2.7V to 40V
- Fixed Output Voltage: 2.5V, 2.8V, 3.0V, 3.3V, 3.6V, 5.0V, 8.0V, 9.0V, 12.0V
- Maximum Load Current Up to 500mA
- High PSRR: 75dB@1kHz, V_{OUT}=3.3V
- Low Quiescent Current: 2.5μA typical
- Low Dropout Voltage:
  - 250mV @ 100mA Load, V_{OUT}=3.3V
  - 780mV @ 500mA Load, V_{OUT}=3.3V
- Output Voltage Accuracy: ±2% @ 1mA typical
- Thermal Shutdown Protection
- Excellent Load/Line Transient Response
- Line Regulation: 0.005%/V typical
- Load Regulation: 25mV typical
- Robust ESD capability:
  - Human Body Model: 2kV
  - Charged Device Model: 1kV
- Package: SOT23-5, SOT23, SOT89-3
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Digital cameras
- Audio devices
- Set-top Box
- Television
- WIFI
- Portable and battery-powered equipment
- Post regulation

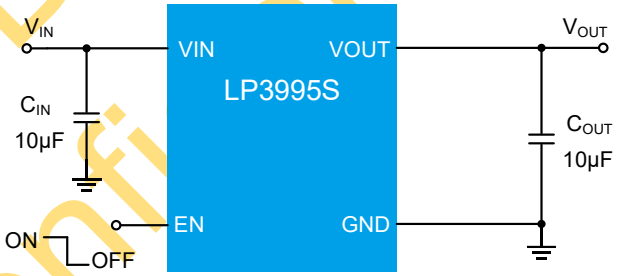
General Description

The LP3995S family are high performance low dropout (LDO) voltage regulators with wide input range, fast transient response, and low quiescent current. The devices are suitable for multitude of applications which require a regulate supplies of up to 500mA load current.

The LP3995S family include standard fixed voltage of 2.5V, 2.8V, 3.0V, 3.3V, 3.6V, 5.0V, 8.0V, 9.0V, and 12.0V. The devices are stable with low ESR ceramic output capacitor. The devices are protected from short circuit by a current limit function and from over-heating by a thermal overload protection.

The devices are available in standard SOT89-3, SOT23 and SOT23-5 packages.

Typical Application Circuit



Order Information

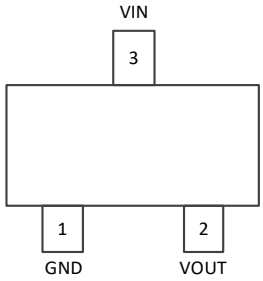
LP3995S-□□ □□ □

- F: Pb Free
- Package Type
  - B5: SOT23-5
  - B3: SOT23
  - X3: SO89-3
- OUT Voltage
  - 30: 3.0V
  - 33: 3.3V
  - 50: 5.0V
  - 12: 12.0V

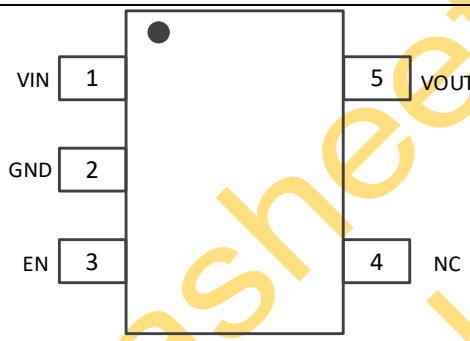
Device Information

Part Number	Top Marking	OUT Voltage	Moisture Sensitivity Level	Package	Shipping
LP3995S-33B5F	LPS 2EYWX	3.3V	MSL3	SOT23-5	3K/REEL
LP3995S-12X3F		3.3V	MSL3	SOT89-3(A)	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

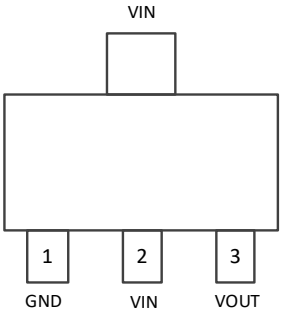
Pin Diagram



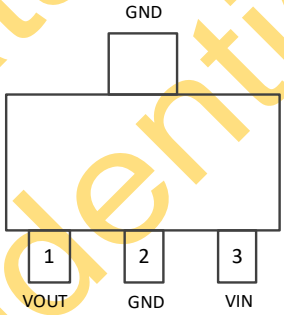
SOT23（top view）



SOT23-5（top view）



SOT89-3(A)(top view)



SOT89-3(B)(top view)

Pin Description

Pin				Name	Description
SOT23	SOT23-5	SOT89-3(A)	SOT89-3(B)		
2	5	3	1	VOUT	Output pin. Bypass with a ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin as possible.
1	2	1	2	GND	Ground.
-	3	-	-	EN	Enable pin. Active high. Driving EN over 1V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. EN pin is pulled high by internal 30nA current source.
3	1	2	3	VIN	Supply input pin. Must be closely decoupled to GND with a capacitor. Place the capacitor as close as to the pin as possible.
	4			NC	No connection.

Absolute Maximum Ratings (Note 1)

VIN to GND ---------- -0.3~44V
VOUT to GND ---------- -0.3~16V
EN to GND ---------- -0.3~6.5V
Maximum Junction Temperature (T_J) ---------- 150℃
Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

Thermal Resistance (SOT89-3, θ_{JA}) (Note 2) ---------- 128 °C/W
Thermal Resistance (SOT23-5, θ_{JA}) (Note 2) ---------- 203 °C/W
Thermal Resistance (SOT89-3, θ_{JC}) (Note 2) ---------- 43 °C/W
Thermal Resistance (SOT23-5, θ_{JC}) (Note 2) ---------- 55 °C/W

Note 2. Measured using 2S2P JEDEC standard PCB with ambient temperature < 25°C

ESD Susceptibility

HBM (Human Body Model) ---------- 2kV
CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions

Input Voltage ---------- 2.7 V to 40V
Operating Junction Temperature Range (T_J) ----------40℃ to 150℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(The specifications are at T_A=25℃,V_{EN}=5V, V_{IN} = 5V, V_{OUT}=3.3V, C_{IN}=C_{OUT}=10μF, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Operation Range		2.7		40	V
I_Q	DC Supply Quiescent Current	V_{EN}=V_{IN}, I_{LOAD}=0mA		2.5	5	μA
I_{SD}	Shutdown Current	V_{EN}=0V		0.3	1	μA
OUTPUT VOLTAGE AND CURRENT						
ACC_{VOUT}	Output Voltage Accuracy	I_{LOAD}=1mA	-2%		2%	
$\frac{\Delta V_{LINE}}{\Delta V_{IN} \times V_{OUT}}$	Output Voltage Line Regulation	V_{IN}=V_{OUT}+0.5V~6V I_{LOAD}=1mA		0.005		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{LOAD} from 1mA to 300mA		25		mV
I_{OUT_MAX}	Max Load Current	V_{EN}=V_{IN}	500			mA
I_{LIMIT}	Load Current Limit	V_{OUT}=0.9*$V_{OUT(Nom)}$	550	600		mA
I_{SHORT}	Short Current Limit	V_{OUT} short to GND		150		mA
V_{DROP}	Dropout Voltage	V_{OUT}=3.3V, I_{LOAD}=100mA		250		mV
		V_{OUT}=3.3V, I_{LOAD}=500mA		780		mV
PSRR	Power Supply Rejection Ratio	V_{IN}=(V_{OUT}+1V)$_{DC}$+0.2V_{P-P}, I_{OUT}=50mA, V_{OUT}=3.3V, f=1kHz		75		dB
		f=10kHz		50		dB
		f=100kHz		36		dB
R_{DIS}	Auto-Discharge Resistance			150		Ω
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			150		℃
T_{SD_HYS}	Thermal Shutdown Hysteresis			40		℃
EN LOGIC						
V_{ENH}	EN Logic High Voltage		1.5			V
V_{ENL}	EN Logic Low Voltage				0.4	V

Typical Characteristics

(T_J = 25℃, LP3995S-33B5F, V_{IN} = 5V , V_{EN} = 5V, V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 10μF, unless otherwise noted.)

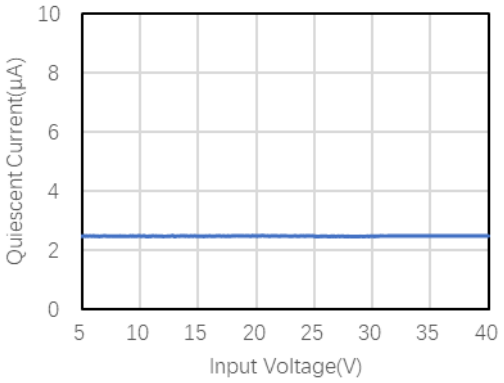


Figure 1 Quiescent Current vs Input Voltage,

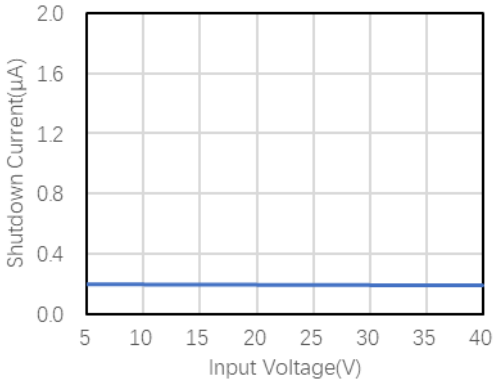


Figure 2 Shutdown Current vs Input Voltage

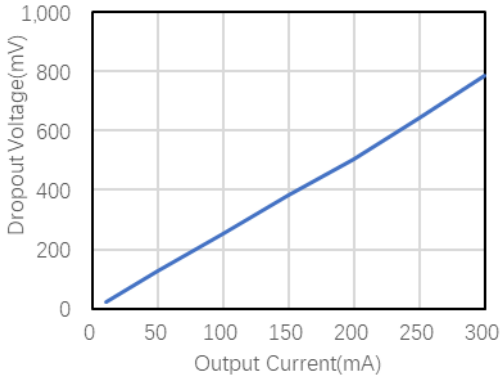


Figure 3 Dropout Voltage vs Output Current

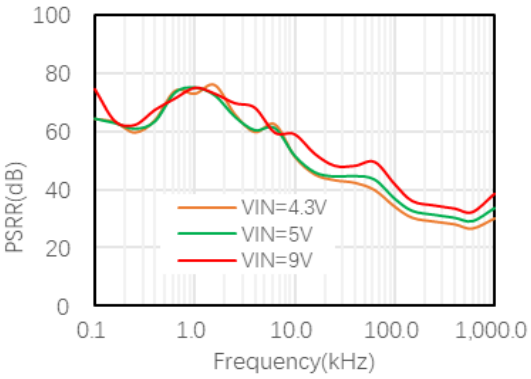


Figure 4 PSRR vs Frequency, I_{OUT}=50mA

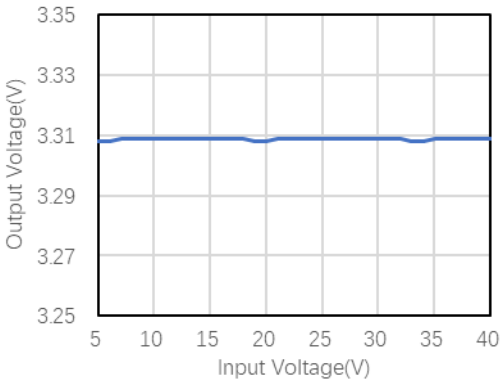


Figure 5 Output Voltage vs Input Voltage

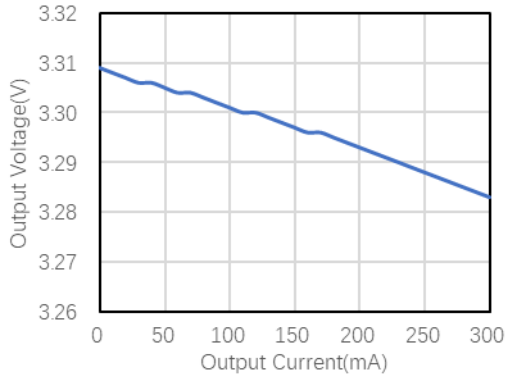


Figure 6 Output Voltage vs Output Current

Typical Characteristics(continued)

Start-up and Shutdown Waveform

(T_J = 25℃, LP3995S-33B5F, V_{IN} = 5V, V_{EN} = 5V, V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 10μF, I_{OUT}=1mA, unless otherwise noted.)

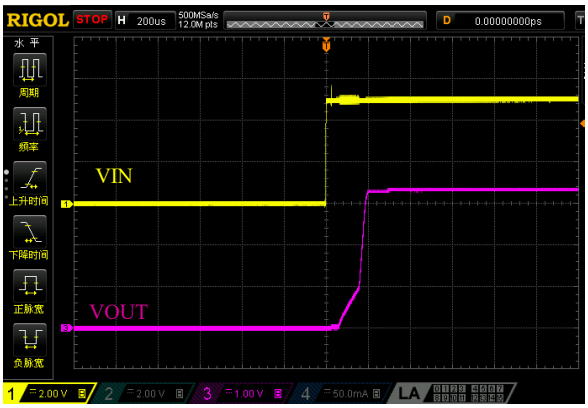


Figure 7 Start-up with VIN on，EN floating

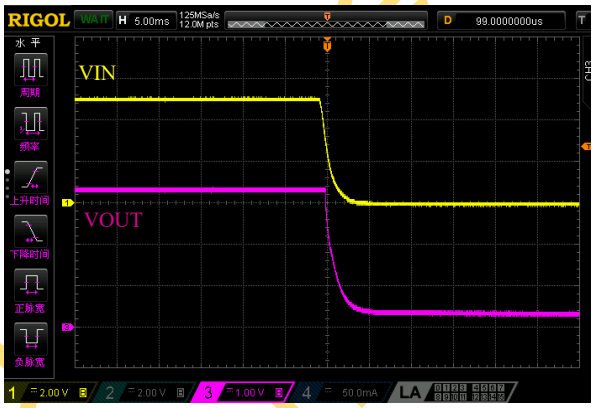


Figure 8 Shutdown with VIN off，EN floating

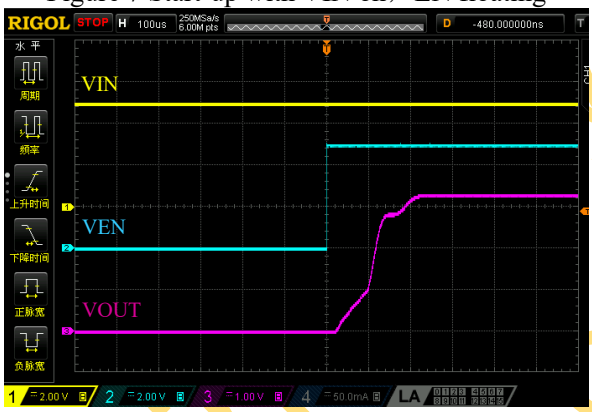


Figure 9 Start-up with EN on

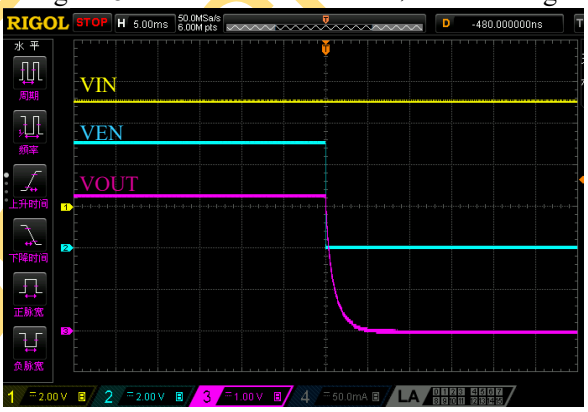


Figure 10 Shutdown with EN off

Typical Characteristics(continued)

Line Transient Response

(T_J = 25℃, LP3995S-33B5F, V_{IN} = 5V, V_{EN} = 5V, V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 10μF, I_{OUT}=1mA, unless otherwise noted.)

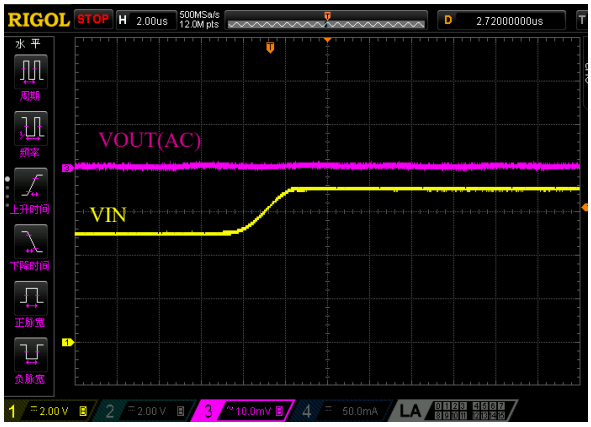


Figure 11 Line Transient Vin=5V ->7V with I_{OUT}=1mA

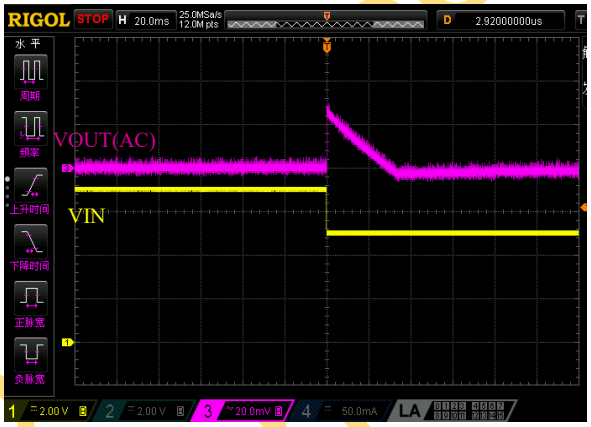


Figure 12 Line Transient Vin=7V ->5V with I_{OUT}=1mA

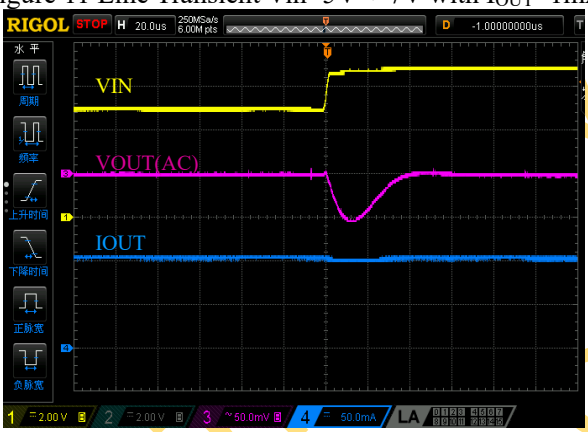


Figure 13 Line Transient Vin=5V ->7V with I_{OUT}=100mA

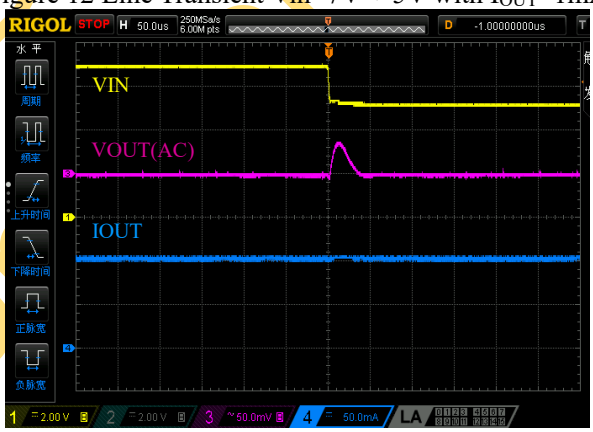


Figure 14 Line Transient Vin=7V ->5V with I_{OUT}=100mA

Typical Characteristics(continued)

Load Transient Waveform

(T_J = 25℃, LP3995S-33B5F, V_{IN} = 5V, V_{EN} = 5V, V_{OUT} = 3.3V, C_{IN} = C_{OUT} = 10μF, unless otherwise noted.)

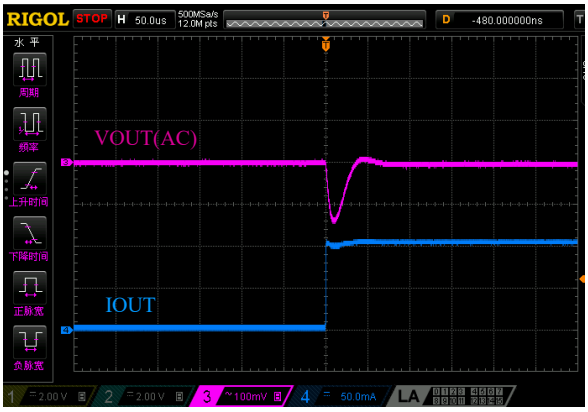


Figure 15 Load Transient I_{OUT}=1->100mA with VIN=5V

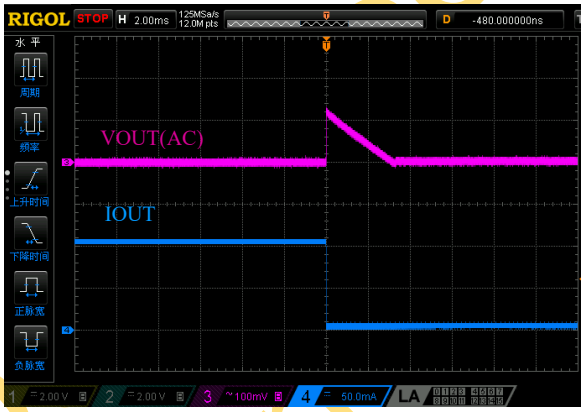


Figure 16 Load Transient I_{OUT}=100->1mA with VIN=5V

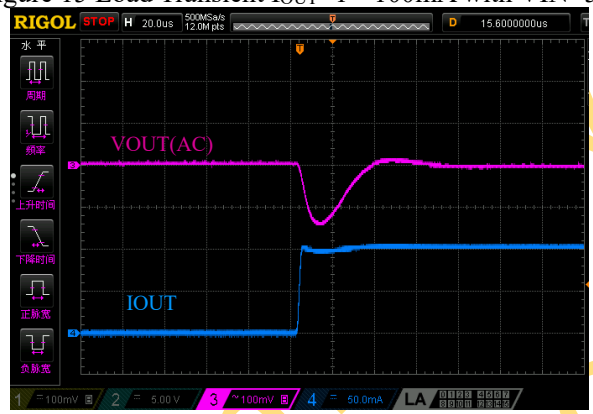


Figure 17 Load Transient I_{OUT}=1->100mA with VIN=12V

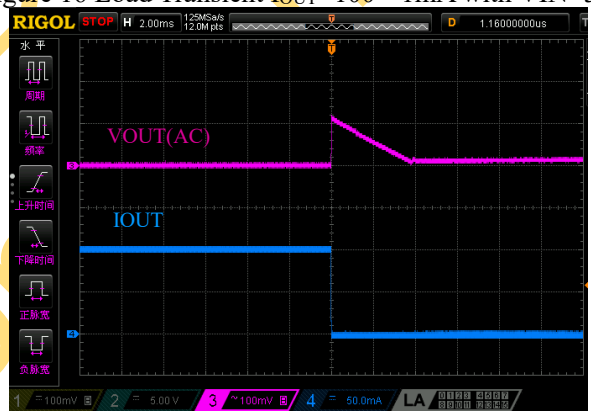


Figure 18 Load Transient I_{OUT}=100->1mA with VIN=12V

Functional Block Diagram

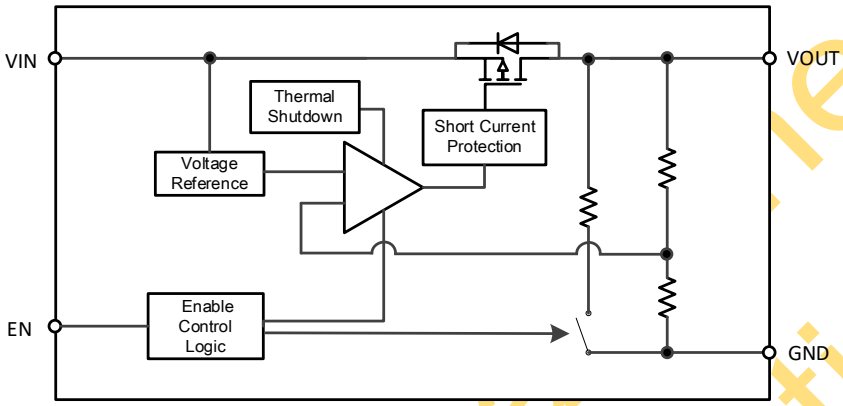


Figure 19. LP3995S-XX functional block diagram

Detailed Description

Overview

The LP3995S family are wide input range 2.7V to 40V, low dropout linear regulators with fixed 2.5V to 12.0V output voltages and up to 500mA output current capability. Optimized for using with ceramic capacitors, the device provides excellent transient performance and suitable for powering digital circuits.

Internally, the devices consist of a voltage reference, an enable control logic, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares a reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

Enable Function

The EN pin is a high active logic input pin. The internal power element is turned off when EN pin is tied low. When the EN pin is pulled high or left floating, the LP3995S will be activated.

Auto Discharge

The LP3995S has a quick discharge function. When the device is disabled by the pulled-down EN pin, a discharge resistor is connected between VOUT and GND. The resistance is 150Ω typically.

Short Current Limit Protection

When the output current at the VOUT pin is higher than current limit threshold or the VOUT pin is short to GND, the short current limit protection will be triggered and clamp the output current to approximately 150mA to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

When the internal junction temperature of LP3995S family devices exceed the junction thermal shutdown threshold (150℃ typical), the devices will shut down the output, after the junction temperature falls below 110℃ , the VOUT voltage will resume.

Application Description

Thermal Consideration

The reason that causes thermal shutdown protection of an LP3995S device is the power dissipation. Nearly all of the power dissipation is generated by the internal PMOS pass device. The power dissipation can be calculated approximately as,

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

where P_D is the power dissipation.

For example, when the device has an input voltage of 40V, an output voltage of 5.0V, and the load current of 300mA. In this situation, the device dissipates the power calculated as below,

$$P_{Dmax} = (40V - 5V) \times 300mA = 10.5W$$

This power dissipation of the LDO device in the SOT23-5 or SOT89-3 package will trigger thermal shutdown protection at high ambient temperature. Then a trade-off must be made between the output current, cost, and thermal requirements of the application.

Input Capacitor

Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. A 1μF-10uF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitches and noise. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

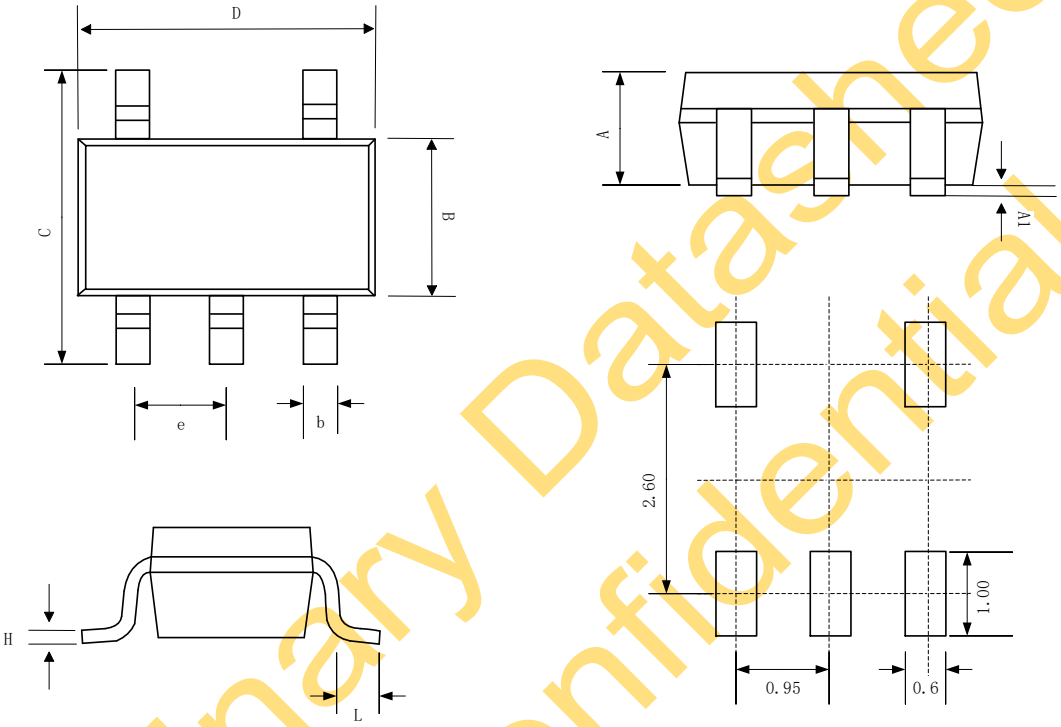
The LP3995S requires a minimum output capacitance of 1μF for output voltage stability. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitor should be located as close to the LDO output as practically possible.

Layout Considerations

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practically possible to the respective LDO pins. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible with a wide and component-side copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB, opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device.

Packaging Information

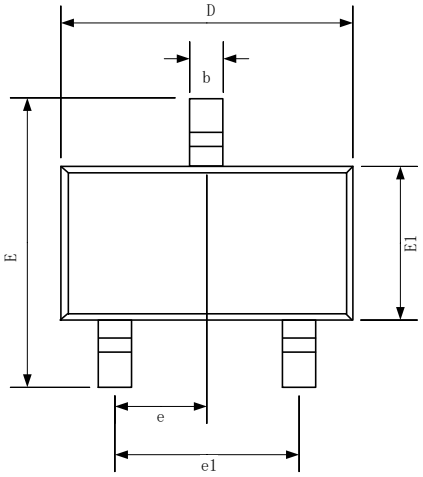
SOT23-5

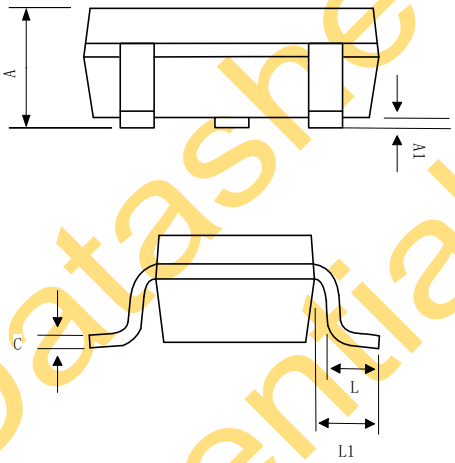


Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

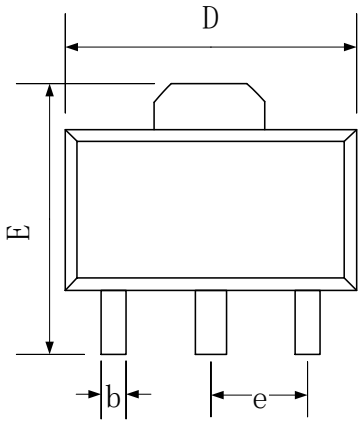
SOT23



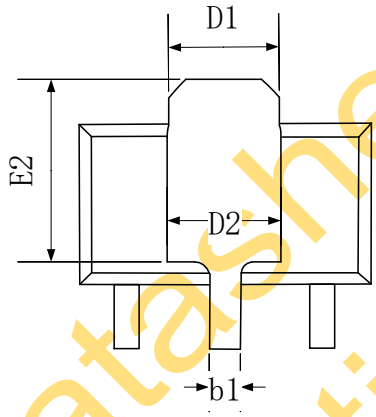


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.000	1.150	1.330
A1	0.000	0.050	0.130
b	0.300	0.380	0.450
c	0.110	0.150	0.190
D	2.820	2.920	3.020
E	2.600	2.800	3.000
E1	1.400	1.600	1.800
e		0.950BSC	
e1		1.900BSC	
L	0.300	0.450	0.600
L1		0.600REF	

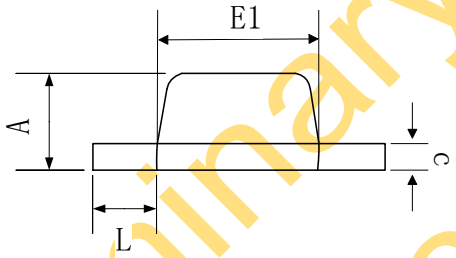
SOT89-3



TOP VIEW



BOTTOM VIEW



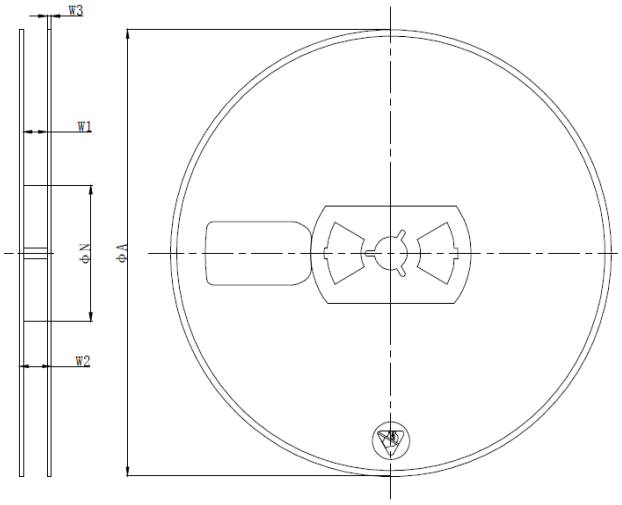
SIDE VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.40	1.50	1.60
b	0.32	0.42	0.52
b1	0.36	0.48	0.56
c	0.35	-	0.44
D	4.39	4.50	4.60
D1	1.55 REF		
D2	1.63 REF		
E	3.9	4.20	4.40
E1	2.30	2.45	2.60
E2	2.75 REF		
e	1.50 BSC		
L	0.78	1.00	1.20

Tape and Reel Information

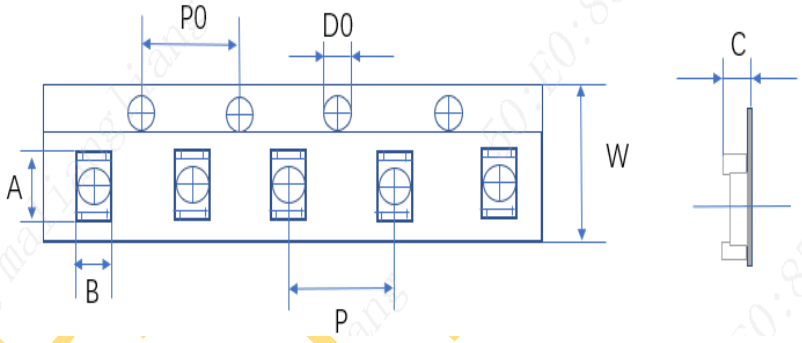
SOT23-5

REEL DIMENSIONS



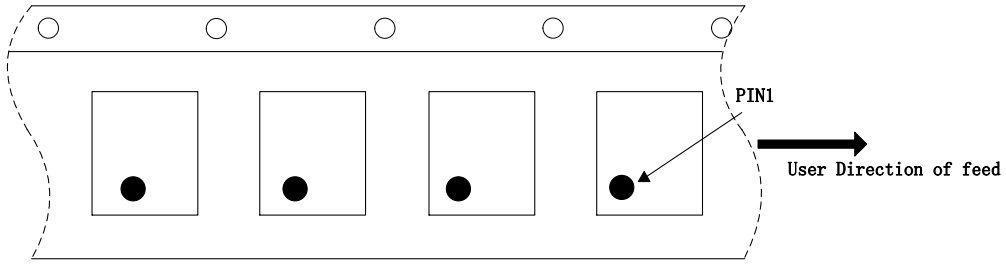
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



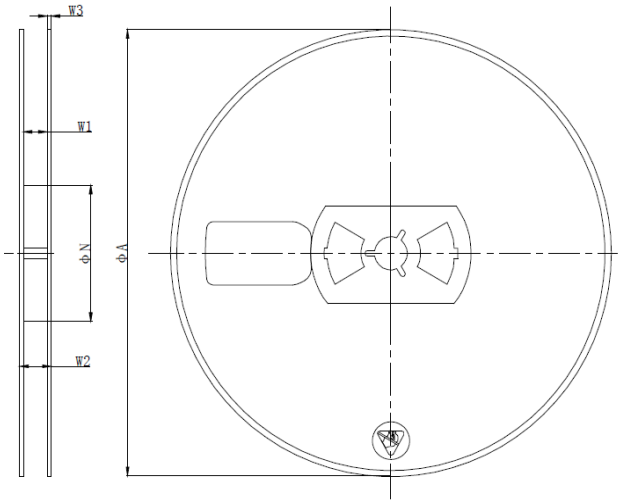
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.00	3.20	3.40
B	3.06	3.26	3.46
P0	3.90	4.00	4.10
P	3.90	4.00	4.10
D0	1.35	1.50	1.65
W	7.70	8.00	8.30
C	1.20	1.40	1.60

PIN1 AND TAPE FEEDING DIRECTION



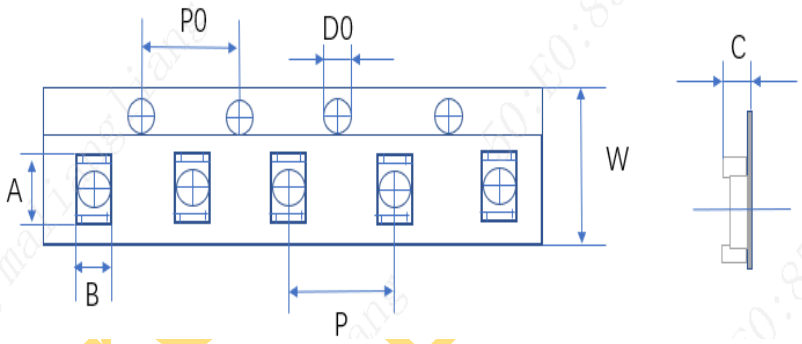
SOT23

REEL DIMENSIONS



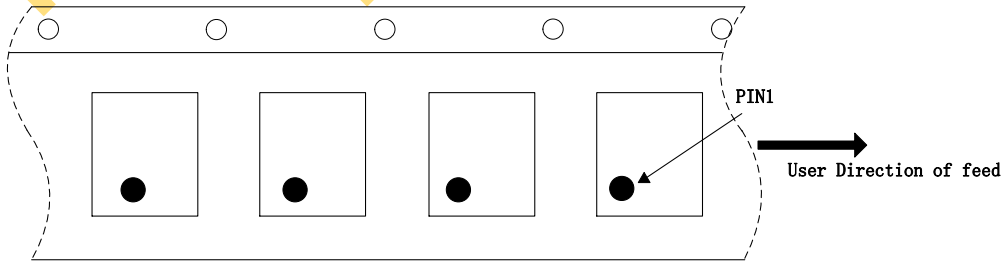
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



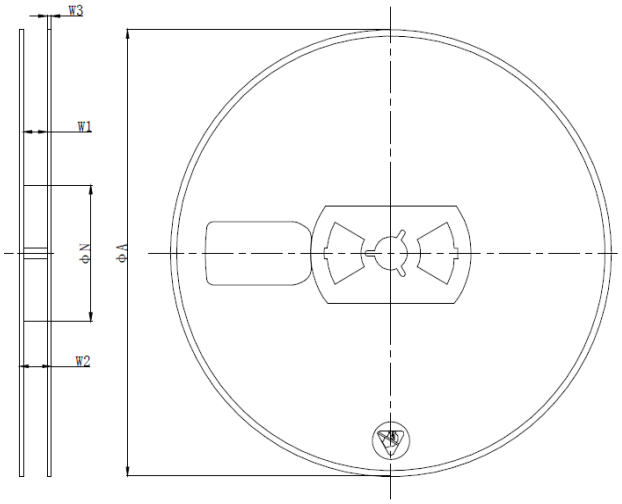
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.00	3.20	3.40
B	2.65	3.15	3.65
P0	3.80	4.00	4.20
P	3.80	4.00	4.20
D0	1.30	1.50	1.70
W	7.70	8.00	8.30
C	0.90	1.30	1.70

PIN1 AND TAPE FEEDING DIRECTION



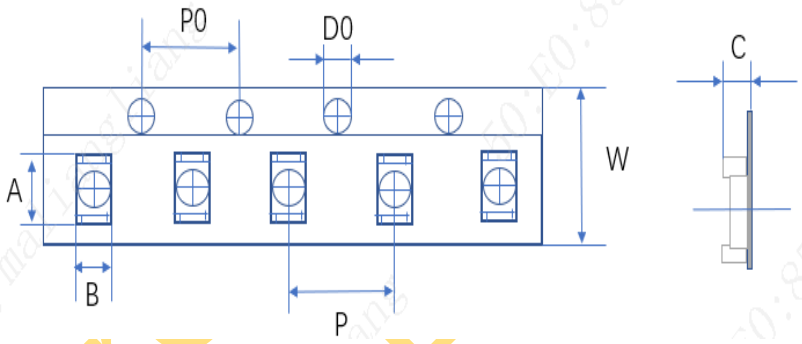
SOT89-3

REEL DIMENSIONS



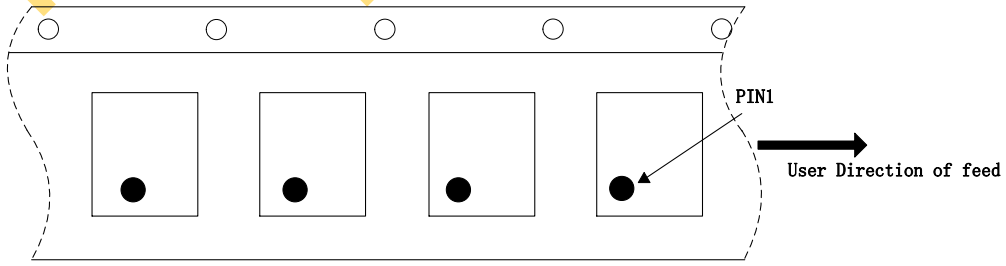
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	11.00	13.00	15.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	4.23	4.43	4.63
B	4.60	4.80	5.00
P0	3.90	4.00	4.10
P	7.80	8.00	8.20
D0	1.30	1.50	1.70
W	11.70	12.00	12.30
C	1.65	1.85	2.05

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350~2000	Volume mm³ ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

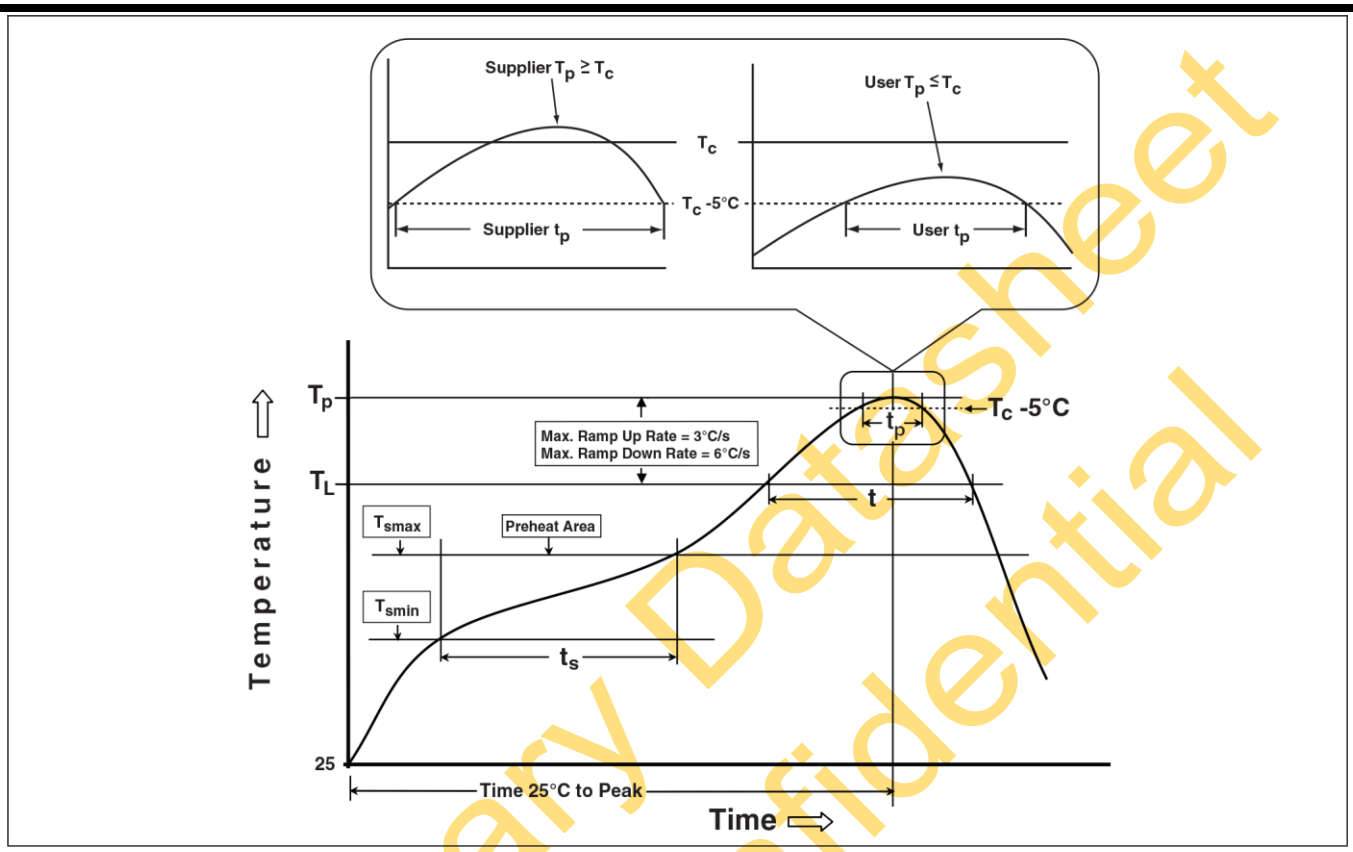


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;