LP6278

19 Channel Level Shift for GOA TFT-LCD Panel

Features

- **DVDD Input Supply Range**
  2.5V to 5.5V
- **VGH1/VGH2 Input Supply Range**
  8.0V to 40V
- **LVGL/VGL Input Supply Range**
  -3.0V to -18V
- **19-Channel Level Shifter:**
  12-ch CLK output (CLK1 to CLK12)
  3-ch STV output (STV0, STV1A, STV1B)
  LC1/LC2 Low frequency output channel
  LS_LVGL and LS_VGL Low voltage output channel
- **Level Shifter output function**
  CLK support programmable phase output
  (6-phase/8-phase/10-phase/12-phase)
  CLK11/12 can be used as a low frequency output channel(CLK configured to 6-/8-/10-phase)
  CLK support multiple DLG mode output
  CLK support multiple Rotate mode output
  LC1/LC2 support multiple Initialize mode output
  CPV1/CPV2 support three input signal modes
  (only rising only falling and rising falling both trigger)
- **Programmable output shutdown discharge function**
  CLK1-CLK12 and LC1/LC2 are a group
  STV0 is a group
  STV1A and STV1B are a group
  LS_LVGL is a group
- **Protection fucntion**
  Input under voltage lockout (UVLO)
  Thermal overload protection (OTP)
  Over current protection (OCP)
  Short circuit protection (SCP)
- **Integrated MTP Non-Volatile Memory**
- **IIC Compatible Interface for Register Control**
- **RoHS compliant and 100% Lead(Pb)-Free**
- **Available in 5.0mmX5.0mm 40-pin QFN Package**

General Description

The LP6278 includes 19-channel high-voltage level shifter. This device is suitable for GOA TFT-LCD panel application. It converts logic level signals from Timing Controller(T-CON) to high level signals used by the LCD panel. The outputs are switching from VGL/LVGL to VGH1/VGH2, with capacitive loads up to 4.7nF.

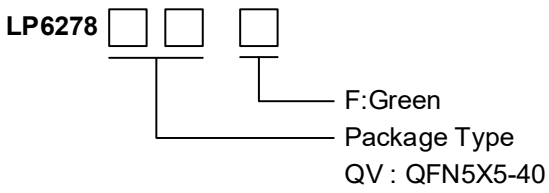
The LP6278 transform the logic-level controlled signals, which are generated by the display timing controller (TCON), into the high-level signals needed by LCD panel. It provides outputs (STV0, STV1A, STV1B, LC1, LC2, CLK1~CLK12, LS_VGL, LS_LVGL) witch are switching from VGL/LVGL to VGH1/VGH2, it also integrates Terminate function.

The LP6278 features extensive protection functions that include UVLO, OTP, SCP and OCP. The device operates over the -40°C to +85°C. It is available in 5mmx5mm, 40-lead QFN package.

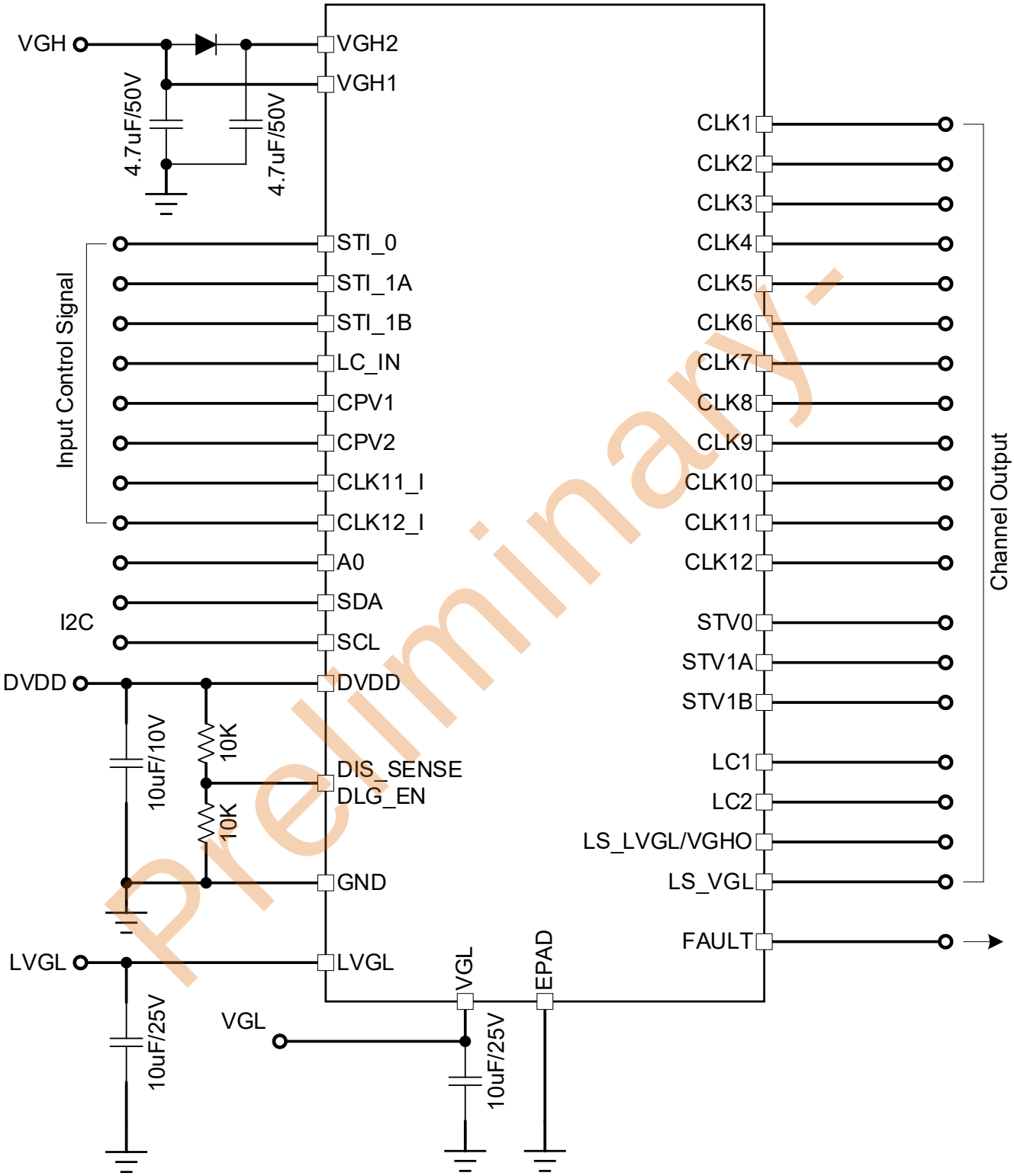
Applications

- **GOA TFT-LCD Panel**

Order Information



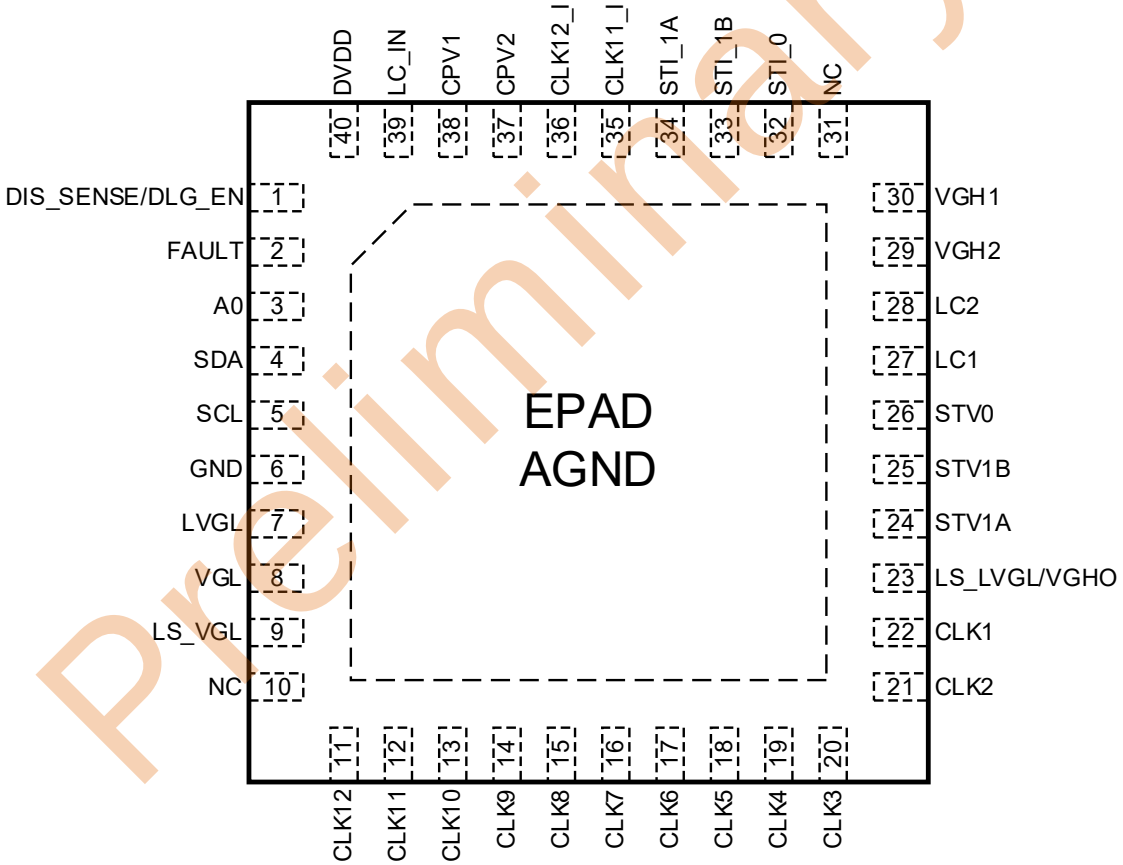
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6278QVF	LPS LP6278 YWX	MSL3	QFN5X5-40	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



QFN5X5-40

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Pin Description

Pin#	Name	Description
1	DIS_SENSE /DLG_EN	0x00h[2]=0, Level shifter input discharge sensing voltage. 0x00h[2]=1, and 0x00h[1:0]=00, DLG enter/exit control function
2	FAULT	FAULT Terminal.
3	A0	Device Address select A0=Low, Address=0x50h, A0=Floating/High, Address=0x52h
4	SDA	I2C - Compatible serial bidirectional data line.
5	SCL	I2C – Compatible clock input.
6	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum dissipation.
7	LVGL	LS_LVGL, CLK1 ~ CLK12, STV0, STV1A, STV1B, LC1/LC2 negative power supply. Please refer to function block and application circuit. The voltage of LVGL must be lower (or equal) than VGL.
8	VGL	Low level of LS_VGL circuit. Please refer to the function block and application circuit.
9	LS_VGL	Discharge function for liquid crystal capacitor.
10	NC	No Connected
11	CLK12	Level Shift Output Channel.
12	CLK11	Level Shift Output Channel.
13	CLK10	Level Shift Output Channel.
14	CLK9	Level Shift Output Channel.
15	CLK8	Level Shift Output Channel.
16	CLK7	Level Shift Output Channel.
17	CLK6	Level Shift Output Channel.
18	CLK5	Level Shift Output Channel.
19	CLK4	Level Shift Output Channel.
20	CLK3	Level Shift Output Channel.

Pin Description(continued)

Pin#	Name	Description
21	CLK2	Level Shift Output Channel.
22	CLK1	Level Shift Output Channel.
23	LS_LVGL /VGHO	Discharge function for liquid crystal capacitor. @0x04h [3] = 0 VGHO output channel @0x04h [3] = 1
24	STV1A	Level Shifter Output Signal. (Start pulse for GOA).
25	STV1B	Level Shifter Output Signal. (Start pulse for GOA).
26	STV0	Level Shifter Output Signal. (GOA reset signal).
27	LC1	Level Shifter Output Signal. (Low frequency LC1).
28	LC2	Level Shifter Output Signal. (Low frequency LC2).
29	VGH2	LC1, LC2, STV0 positive power supply. Please refer to function block and application circuit.
30	VGH1	LS_VGL, LS_LVGL, CLK1 to CLK12, STV1A and STV1B positive power supply. Please refer to function block and application circuit.
31	NC	No Connected
32	STI_0	Level shifter input signal. (GOA reset signal) rising/falling edge trigger
33	STI_1B	Level shifter input signal. (Start pulse for GOA) rising/falling edge trigger
34	STI_1A	Level shifter input signal. (Start pulse for GOA) rising/falling edge trigger
35	CLK11_I	Level shifter input signal. CLK11 rising/falling edge trigger *- Only 0x00h[3]=1 and The CLK output is not 12 phase
36	CLK12_I	Level shifter input signal. CLK12 rising/falling edge trigger *- Only 0x00h[3]=1 and The CLK output is not 12 phase
37	CPV2	Level shifter input signal rising/falling edge trigger.
38	CPV1	Level shifter input signal rising/falling edge trigger.
39	LC_IN	Level shifter input signal. (Low frequency clock) rising/falling edge trigger
40	DVDD	Supply voltage input.
41	EPAD	The E-Pad should be connected to ground for maximum dissipation.

Absolute Maximum Ratings (Note1)

SDA, SCL to GND ---------- -0.3V to +7.0V
DIS_SENSE/DLG_EN to GND ---------- -0.3V to +7.0V
A0, FAULT to GND ---------- -0.3V to +7.0V
STI_0, STI_1A, STI_1B, CPV1, CPV2, LC_IN to GND ---------- -0.3V to +7.0V
CLK11_IN, CLK12_IN to GND ---------- -0.3V to +7.0V
DVDD to GND ---------- -0.3V to +7.0V
LVGL to GND ---------- -20V to +0.3V
VGL to GND ---------- -20V to +0.3V
LS_VGL to GND ---------- (-0.3+VGL)V to +VGH1
LS_LVGL/VGHO to GND ---------- (-0.3+LVGL)V to +VGH1
CLK1-CLK12 to GND ---------- (-0.3+LVGL)V to +VGH1
STV1A, STV1B to GND ---------- (-0.3+LVGL)V to +VGH1
STV0, LC1, LC2 to GND ---------- (-0.3+LVGL)V to +VGH2
VGH1, VGH2 to GND ---------- -0.3V to +45V
LVGL,VGL to GND ---------- -22V to +0.3V
VGH1, VGH2 to LVGL, VGL ---------- -0.3V to +60V

Note1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 2KV
CDM (Charge Discharge Model) ---------- 750V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ---------- 150℃
Operating Junction Temperature Range (TJ) ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range ---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- TBD℃/W

Recommended Operating Conditions

Over Operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	Def.	MAX	UNIT
DVDD	DVDD supply voltage		2.5	3.3	5.5	V
VGH1	VGH1 input voltage range		10		40	V
VGH2	VGH2 input voltage range		10		40	V
LVGL	LVGL input voltage range		-18		-3	V
VGL	VGL input voltage range		-18		-3	V
$DVDD_{UVLOR}$	DVDD under voltage rising		2.3	2.4	2.5	V
$DVDD_{UVLOF}$	DVDD under voltage falling		1.7	1.8	1.9	V
$VGH2_{UVLOR}$	VGH2 under voltage rising	0x03h[0]=0	7	7.5	8.0	V
$VGH2_{UVLOR}$	VGH2 under voltage rising	0x03h[0]=1	14	15	16	V
$VGH2_{UVLOF}$	VGH2 under voltage falling		3	4	5	V
XON_{DET_VR1}	XON detect voltage rising1	0x00h[1:0]=00, Rising Detect DVDD uvlo rising	2.3	2.4	2.5	V
XON_{DET_VF1}	XON detect voltage falling1	0x00h[1:0]=00, Falling Detect DVDD uvlo falling	1.7	1.8	1.9	V
XON_{DET_VR2}	XON detect voltage rising2	0x00h[1:0]=01, Rising	2.4	2.5	2.6	V
XON_{DET_VF2}	XON detect voltage falling2	0x00h[1:0]=01, Falling	2.2	2.3	2.4	V
XON_{DET_VR3}	XON detect voltage rising3	0x00h[1:0]=10, Rising	0.9	1.0	1.1	V
XON_{DET_VF3}	XON detect voltage falling3	0x00h[1:0]=10, Falling	0.7	0.8	0.9	V
XON_{DET_VR4}	XON detect voltage rising4	0x00h[1:0]=11, Rising	2.6	2.7	2.8	V
XON_{DET_VF4}	XON detect voltage falling4	0x00h[1:0]=11, Falling	2.4	2.5	2.6	V

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
V_{DVDD}	DVDD supply voltage	DVDD	2.5	3.3	5.5	V
$V_{VGH1/2}$	VGH1/2 supply voltage		10		40	V
V_{LVGL}	LVGL supply voltage		-18		-3	V
V_{VGL}	VGL supply voltage		-18		-3	V
VGH-VGL	VGH1/2 – LVGL/VGL voltage range				60	V
V_{DVDD_UVLOR}	DVDD under voltage lockout	Rising Reset Voltage MTP load voltage	2.3	2.4	2.5	V
V_{DVDD_UVLOF}	DVDD under voltage lockout	Falling Threshold Voltage	1.7	1.8	1.9	V
$VGH2_{UVLOR}$	VGH2 under voltage lockout	Rising Reset Voltage 0x03h[0]=1	14	15	16	V
$VGH2_{UVLOR}$	VGH2 under voltage lockout	Rising Reset Voltage 0x03h[0]=0	7.0	7.5	8.0	V
$VGH2_{UVLOF}$	VGH2 under voltage lockout	Falling Threshold Voltage	3	4	5	V
I_{Q_DVDD}	DVDD quiescent current			1.3		mA
I_{Q_VGH1}	VGH1 quiescent current			0.2		mA
I_{Q_VGH2}	VGH2 quiescent current			0.5		mA
I_{Q_VGL}	VGL quiescent current			50		uA
I_{Q_LVGL}	LVGL quiescent current			0.3		mA
T_{SD}	Over temperature shutdown protect	Junction temperature	145	155	165	℃
TSD_{HYS}	Thermal shutdown hysteresis recover	Falling triger		20		℃
$BLANK_{TIME}$	Power on blanking time	0x04h[7]=0		0		mS
$BLANK_{TIME}$	Power on blanking time	0x04h[7]=1		150		mS

*. The sequence of LVGL must be earlier (or equal) than VGL in the application.
And the voltage of LVGL must be lower (or equal) than VGL

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Signals (CPV1, CPV2, LC_IN, STI_0, STI_1A, STI_1B, A0, FAULT)						
$CPV1_{PD\_R}$	CPV1 internal pull low resistor	Internal pull low to GND		100		KΩ
$CPV2_{PD\_R}$	CPV2 internal pull low resistor	Internal pull low to GND		100		KΩ
$LC\_IN_{PD\_R}$	LC_IN internal pull low resistor	Internal pull low to GND		100		KΩ
$STI\_0_{PD\_R}$	STI_0 internal pull low resistor	Internal pull low to GND		100		KΩ
$STI\_1A_{PD\_R}$	STI_1A internal pull low resistor	Internal pull low to GND		100		KΩ
$STI\_1B_{PD\_R}$	STI_1B internal pull low resistor	Internal pull low to GND		100		KΩ
DLG_EN	DLG_EN internal pull low resistor	Internal pull low to GND @0x00h[1:0]=00		100		KΩ
CLK11_I	CLK11_I internal pull low resistor	Internal pull low to GND		100		KΩ
CLK12_I	CLK12_I internal pull low resistor	Internal pull low to GND		100		KΩ
$FAULT_{PU\_R}$	FAULT internal pull up resistor	Internal pull up to DVDD		200		KΩ
$A0_{PU\_R}$	A0 internal pull up resistor	Internal pull up to DVDD		200		KΩ
$FOSC_{CPV}$	CPV1/CPV2 operating frequency	Maximum frequency	1200			KHz
VIW	Input signal Minimum pulse width	DVDD=2.5V to 5.0V	200			nS
VIH	Input signal high level voltage	DVDD=2.5V to 5.0V	1.2			V
VIL	Input signal low level voltage	DVDD=2.5V to 5.0V			0.6	V

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel (CLK1 to CLK12)						
RON_{HMOS}	CLK1~CLK12 high-side PMOS Ron	I_{LOAD}=10mA		8	15	Ω
RON_{LMOS}	CLK1~CLK12 low-side NMOS Ron	I_{LOAD}=10mA		8	15	Ω
CLK_{PHASE}	CLK phase output select	0x00h[7:6]=00		6		Ph
CLK_{PHASE}	CLK phase output select	0x00h[7:6]=01		8		Ph
CLK_{PHASE}	CLK phase output select	0x00h[7:6]=10		10		Ph
CLK_{PHASE}	CLK phase output select	0x00h[7:6]=11		12		Ph
T_{R1}	CLK1~CLK12 rising slew rate1	0x00h[5:4]=00 R_L=51R, C_L=4.7nF		1000		V/us
T_{R2}	CLK1~CLK12 rising slew rate2	0x00h[5:4]=01 R_L=51R, C_L=4.7nF		700		V/us
T_{R3}	CLK1~CLK12 rising slew rate3	0x00h[5:4]=10 R_L=51R, C_L=4.7nF		400		V/us
T_{R4}	CLK1~CLK12 rising slew rate4	0x00h[5:4]=11 R_L=51R, C_L=4.7nF		100		V/us
T_{F1}	CLK1~CLK12 falling slew rate1	0x00h[5:4]=00 R_L=51R, C_L=4.7nF		1000		V/us
T_{F2}	CLK1~CLK12 falling slew rate2	0x00h[5:4]=01 R_L=51R, C_L=4.7nF		700		V/us
T_{F3}	CLK1~CLK12 falling slew rate3	0x00h[5:4]=10 R_L=51R, C_L=4.7nF		400		V/us
T_{F4}	CLK1~CLK12 falling slew rate4	0x00h[5:4]=11 R_L=51R, C_L=4.7nF		100		V/us
T_{PR}	CLK1~CLK12 rising delay	50% input to 10% output		80	150	nS
T_{PF}	CLK1~CLK12 falling delay	50% input to 90% output		80	150	nS

*. Rising/Falling time measure point is before RC.

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel (STV0, STV1A, STV1B)						
RON_{HMOS}	STV0 high-side PMOS Ron	I_{LOAD}=10mA		8	15	Ω
RON_{LMOS}	STV0 low-side NMOS Ron	I_{LOAD}=10mA		8	15	Ω
T_R	STV0 rising slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_F	STV0 falling slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_{PR}	STV0 rising delay	50% input to 10% output		80	150	nS
T_{PF}	STV0 falling delay	50% input to 90% output		80	150	nS
AUP_{TIME}	STV0 autopulse time	0x04h[4]=1	220	260	300	uS
RON_{HMOS}	STV1A high-side PMOS Ron	I_{LOAD}=10mA		8	15	Ω
RON_{LMOS}	STV1A low-side NMOS Ron	I_{LOAD}=10mA		8	15	Ω
T_R	STV1A rising slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_F	STV1A falling slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_{PR}	STV1A rising delay	50% input to 10% output		80	150	nS
T_{PF}	STV1A falling delay	50% input to 90% output		80	150	nS
RON_{HMOS}	STV1B high-side PMOS Ron	I_{LOAD}=10mA		8	15	Ω
RON_{LMOS}	STV1B low-side NMOS Ron	I_{LOAD}=10mA		8	15	Ω
T_R	STV1B rising slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_F	STV1B falling slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_{PR}	STV1B rising delay	50% input to 10% output		80	150	nS
T_{PF}	STV1B falling delay	50% input to 90% output		80	150	nS

*. Rising/Falling time measure point is before RC.

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel (LC1, LC2)						
RON_{HMOS}	LC1 high-side PMOS Ron	I_{LOAD}=10mA		8	15	Ω
RON_{LMOS}	LC1 low-side NMOS Ron	I_{LOAD}=10mA		8	15	Ω
T_R	LC1 rising slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_F	LC1 falling slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_{PR}	LC1 rising delay	50% input to 10% output		80	150	nS
T_{PF}	LC1 falling delay	50% input to 90% output		80	150	nS
RON_{HMOS}	LC2 high-side PMOS Ron	I_{LOAD}=10mA		8	15	Ω
RON_{LMOS}	LC2 low-side NMOS Ron	I_{LOAD}=10mA		8	15	Ω
T_R	LC2 rising slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_F	LC2 falling slew rate	R_L=51R, C_L=4.7nF		300		V/us
T_{PR}	LC2 rising delay	50% input to 10% output		80	150	nS
T_{PF}	LC2 falling delay	50% input to 90% output		80	150	nS

*. Rising/Falling time measure point is before RC.

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel (LS_LVGL, LS_VGL)						
RON_{HMOS}	LS_LVGL high-side PMOS Ron	I_{LOAD}=10mA		10	18	Ω
RON_{LMOS}	LS_LVGL low-side NMOS Ron	I_{LOAD}=10mA		10	18	Ω
XON_{DLY}	LS_LVGL rising propagation time	XON trigger		0.2	0.5	uS
T_R	LS_LVGL rising slew rate	R_L=51R, C_L=4.7nF			1	uS
VGH1O	VGH1O delay autopulse time	STV0 autopulse end	4.4	5.4	6.4	uS
VGH1O	VGH1O power on delay time	0x04h[1:0]=00		0		mS
VGH1O	VGH1O power on delay time	0x04h[1:0]=01		50		mS
VGH1O	VGH1O power on delay time	0x04h[1:0]=10		100		mS
VGH1O	VGH1O power on delay time	0x04h[1:0]=11		150		mS
RON_{HMOS}	LS_VGL high-side PMOS Ron	I_{LOAD}=10mA		10	18	Ω
RON_{LMOS}	LS_VGL low-side NMOS Ron	I_{LOAD}=10mA		10	18	Ω
XON_{DLY}	LS_VGL rising propagation time	XON trigger		0.2	0.5	uS
T_R	LS_VGL rising slew rate	R_L=51R, C_L=4.7nF			1	uS

*. Rising/Falling time measure point is before RC.

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel OCP Level (CLK1 to CLK12)						
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=000 SCP detect level	200			mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=000 SCP detect level	200			mA
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=001	20	30		mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=001	20	30		mA
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=010	30	40		mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=010	30	40		mA
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=011	40	50		mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=011	40	50		mA
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=100	60	70		mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=100	60	70		mA
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=101	75	90		mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=101	75	90		mA
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=110	100	120		mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=110	100	120		mA
OCP+	CLK1~CLK12 PMOS current detect	0x02h[5:3]=111	135	160		mA
OCP-	CLK1~CLK12 NMOS current detect	0x02h[5:3]=111	135	160		mA

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel OCP Time (CLK1 to CLK12)						
OCP_DC	CLK1~CLK12 OCP detect count	0x02[7:6]=00		4		Time
OCP_DC	CLK1~CLK12 OCP detect count	0x02[7:6]=01		8		Time
OCP_DC	CLK1~CLK12 OCP detect count	0x02[7:6]=10		16		Time
OCP_DC	CLK1~CLK12 OCP detect count	0x02[7:6]=11		32		Time
OCP_BT	CLK1~CLK12 OCP blanking time	0x01h[2]=0	1.2	2		uS
OCP_BT	CLK1~CLK12 OCP blanking time	0x01h[2]=1	3.2	4		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=000, ±40%	0.6	1		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=001, ±40%	1.2	2		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=010, ±20%	2.4	3		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=011, ±20%	3.2	4		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=100, ±20%	4	5		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=101, ±20%	4.8	6		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=110, ±20%	5.6	7		uS
OCP_DT	CLK1~CLK12 OCP detect time	0x02h[2:0]=111, ±20%	6.4	8		uS
SCP+	CLK1~CLK12 PMOS SCP detect		200	300		mA
SCP-	CLK1~CLK12 NMOS SCP detect		200	300		mA
SCP_DTH	CLK1~CLK12 PMOS SCP time	Detect high-side PMOS	40	50		uS
SCP_DTL	CLK1~CLK12 LMOS SCP time	Detect low-side NMOS	40	50		uS

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel OCP Level (LC1, LC2, STV0, STV1A, STV1B, LS_LVGL, LS_VGL)						
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=000 OCP disable	200			mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=000 OCP disable	200			mA
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=001	20	30		mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=001	20	30		mA
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=010	30	40		mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=010	30	40		mA
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=011	40	50		mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=011	40	50		mA
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=100	60	70		mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=100	60	70		mA
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=101	75	90		mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=101	75	90		mA
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=110	100	120		mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=110	100	120		mA
OCP+	CHn Excluded PMOS current detect	0x01h[5:3]=111	135	160		mA
OCP-	CHn Excluded NMOS current detect	0x01h[5:3]=111	135	160		mA

Electrical Characteristics

DVDD = 3.3V, VGH1=VGH2=30V, LVGL=-10V, VGL=-6V, GND=0V, T_A=25℃
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

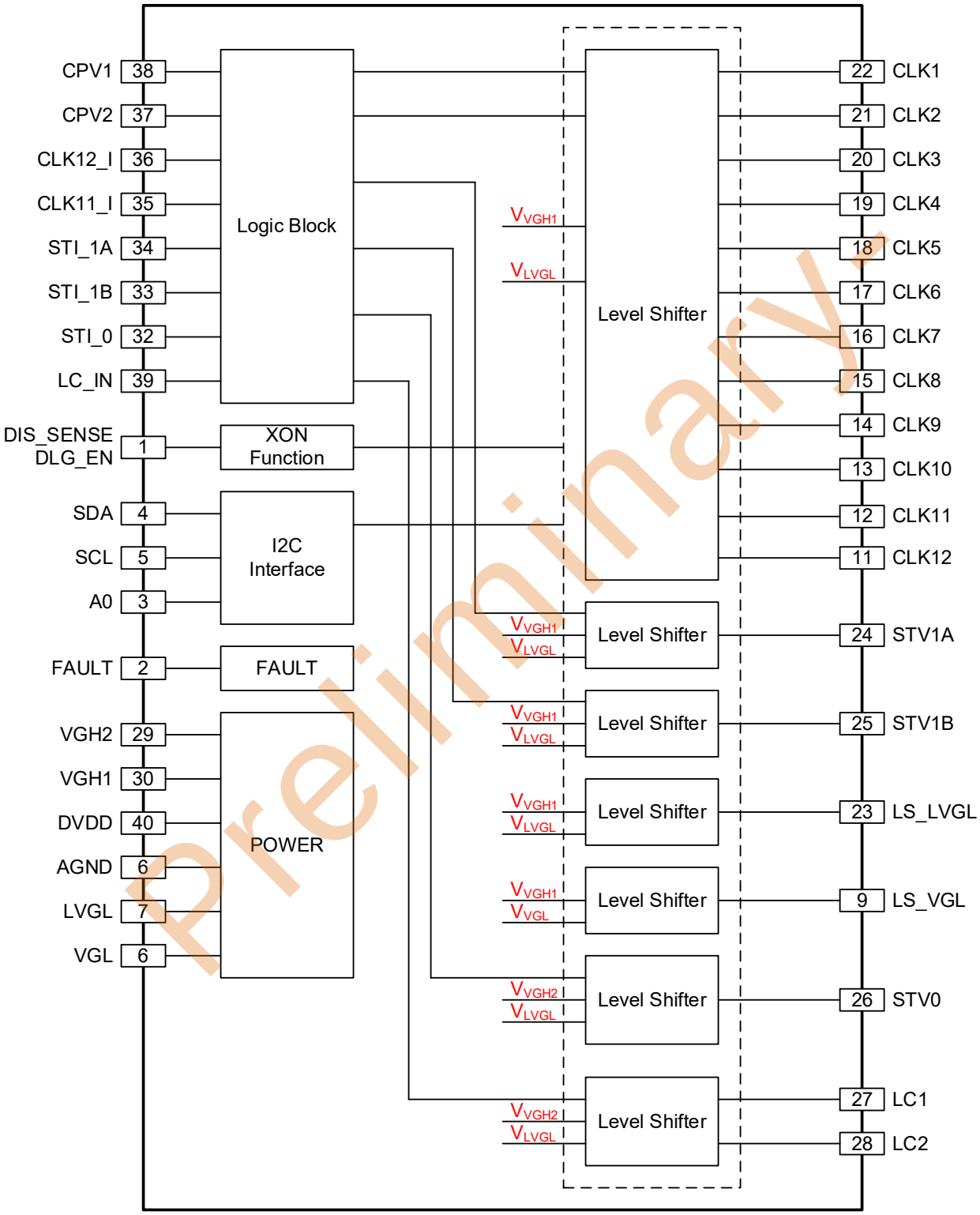
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Channel OCP Time (LC1, LC2, STV0, STV1A, STV1B, LS_LVGL, LS_VGL)						
OCP_DC	CHn Excluded OCP detect count	0x01[7:6]=00		4		Time
OCP_DC	CHn Excluded OCP detect count	0x01[7:6]=01		8		Time
OCP_DC	CHn Excluded OCP detect count	0x01[7:6]=10		16		Time
OCP_DC	CHn Excluded OCP detect count	0x01[7:6]=11		32		Time
OCP_BT	ALL channel high and low side OCP Blanking time	0x01h[2]=0	1.2	2		uS
OCP_BT	ALL channel high and low side OCP Blanking time	0x01h[2]=1	3.2	4		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=000, ±30%	0.6	1		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=001, ±25%	1.2	2		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=010, ±20%	2.4	3		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=011, ±20%	3.2	4		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=100, ±20%	4	5		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=101, ±20%	4.8	6		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=110, ±20%	5.6	7		uS
OCP_DT	STVn High-Side OCP detect time	0x02h[2:0]=111, ±20%	6.4	8		uS
OCP_DT	CHn Excluded Low OCP detect time	0x01h[1:0]=00, ±20%	32	40		uS
OCP_DT	CHn Excluded Low OCP detect time	0x01h[1:0]=01, ±20%	64	80		uS
OCP_DT	CHn Excluded Low OCP detect time	0x01h[1:0]=10, ±20%	96	120		uS
OCP_DT	CHn Excluded Low OCP detect time	0x01h[1:0]=11, ±20%	128	160		uS
SCP+	CHn Excluded PMOS SCP detect		200	300		mA
SCP-	CHn Excluded NMOS SCP detect		200	300		mA
SCP_DTH	CHn Excluded PMOS SCP time	Detect high-side PMOS	40	50		uS
SCP_DTL	CHn Excluded LMOS SCP time	Detect low-side NMOS	40	50		uS

Electrical Characteristics

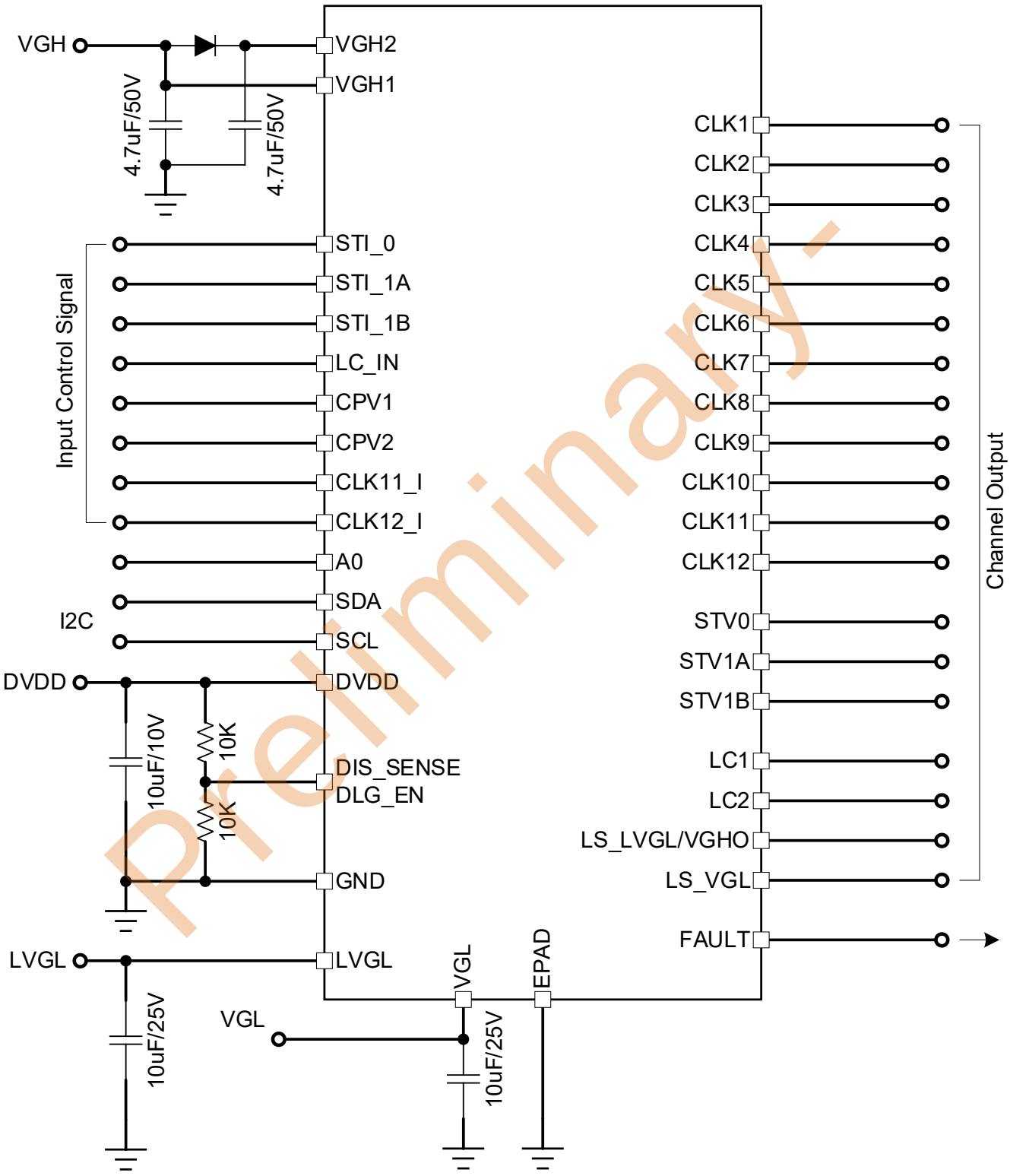
The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
IIC INTERFACE(SDA,SCL)						
V_{IH}	High Level Input Voltage		1.5	---	---	V
V_{IL}	Low Level Input Voltage		---	---	0.5	V
IIC TIMING CHARCTERISTICS						
f_{SCL}	Serial-Clock Frequency		10	---	400	KHz
t_{BUF}	Bus Free Time Between STOP and START Conditions		1300	---	---	nS
$t_{HD.STA}$	Hold Time(Repeated) START Condition		600	---	---	nS
t_{LOW}	SCL Pulse-Width Low		1300	---	---	nS
t_{HIGH}	SCL Pulse-Width High		600	---	---	nS
$t_{SU.STA}$	Setup Time for a Repeated START Condition		600	---	---	nS
$t_{HD.DAT}$	Data Hold Time		50	---	800	nS
$t_{SU.DAT}$	Data Setup Time		100	---	---	nS
t_R	SDA and SCL Receiving Rise Time	CB is IN pF	20+ 0.1CB	---	300	nS
t_F	SDA and SCL Receiving Fall Time	CB is IN pF	20+ 0.1CB	---	300	nS
CIN	SDA and SCL Input Capacitance			---	400	pF
$t_{SU.STO}$	Setup Time for STOP Condition		600	---	---	nS
t_{AA}	Clock Low to Data Out Valid		100	---	900	nS
	Program MTP Blanking Time			200		ms

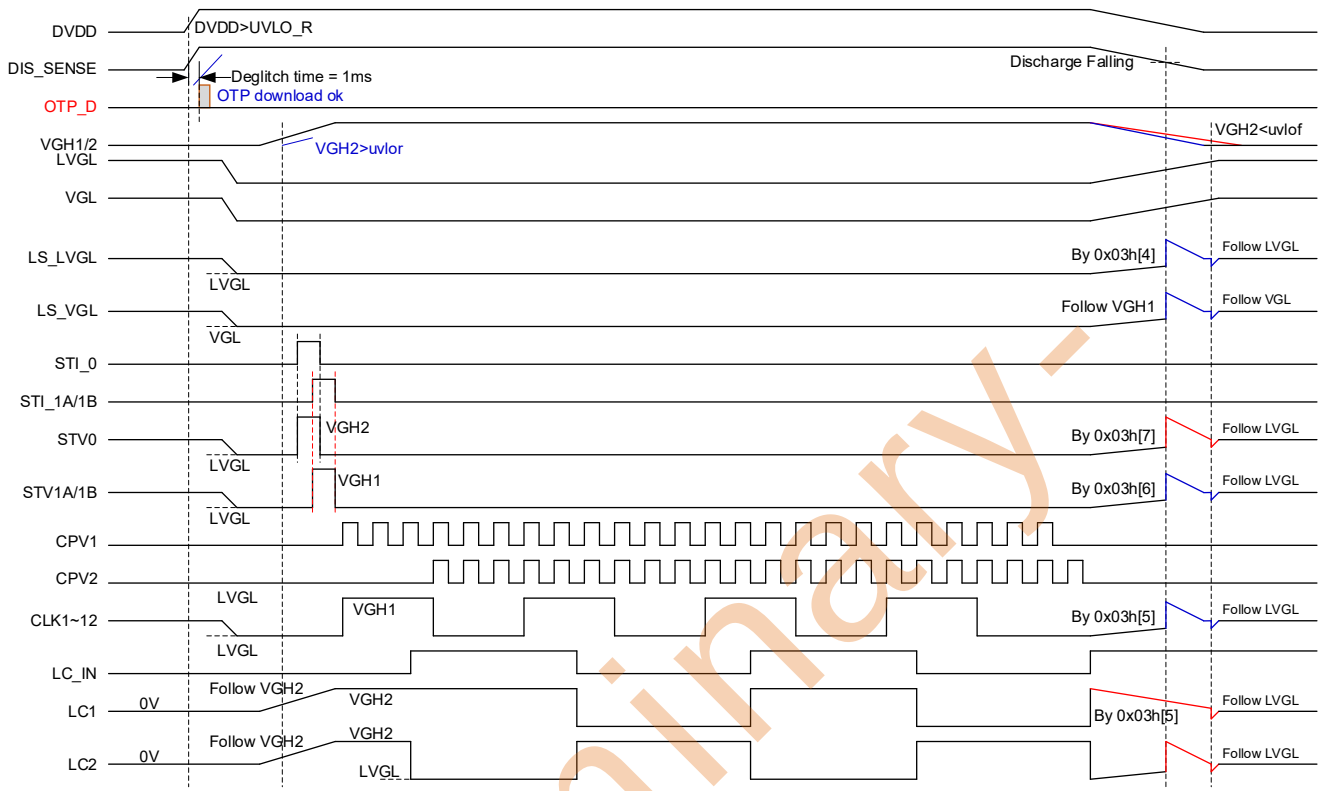
Functional Block Diagram



Typical Application Circuit



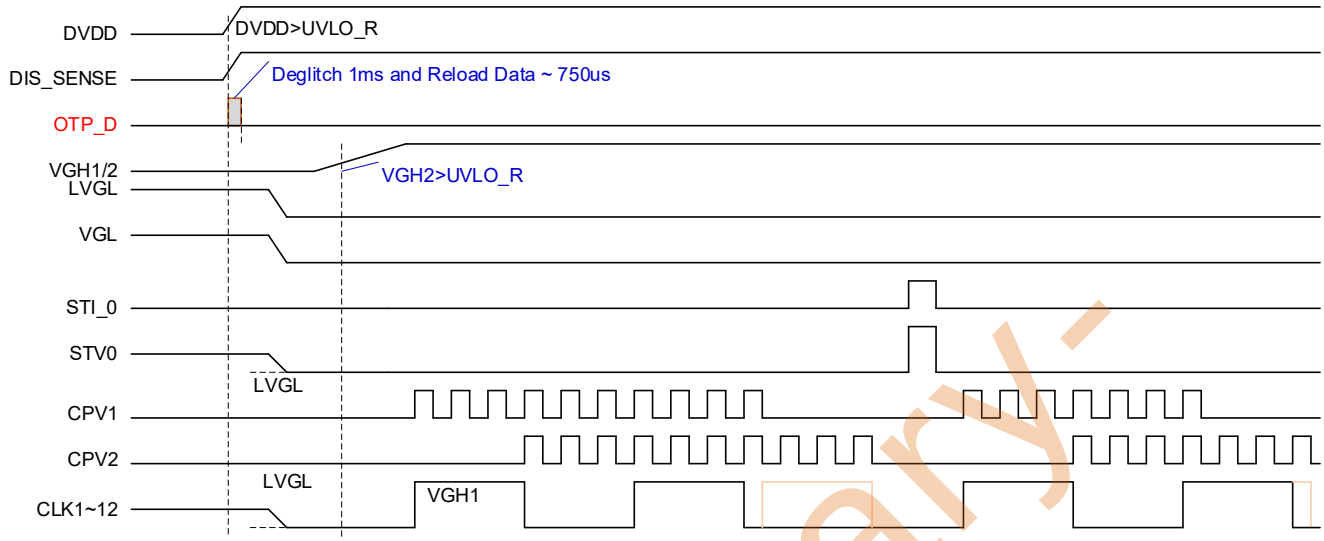
Timing Diagram



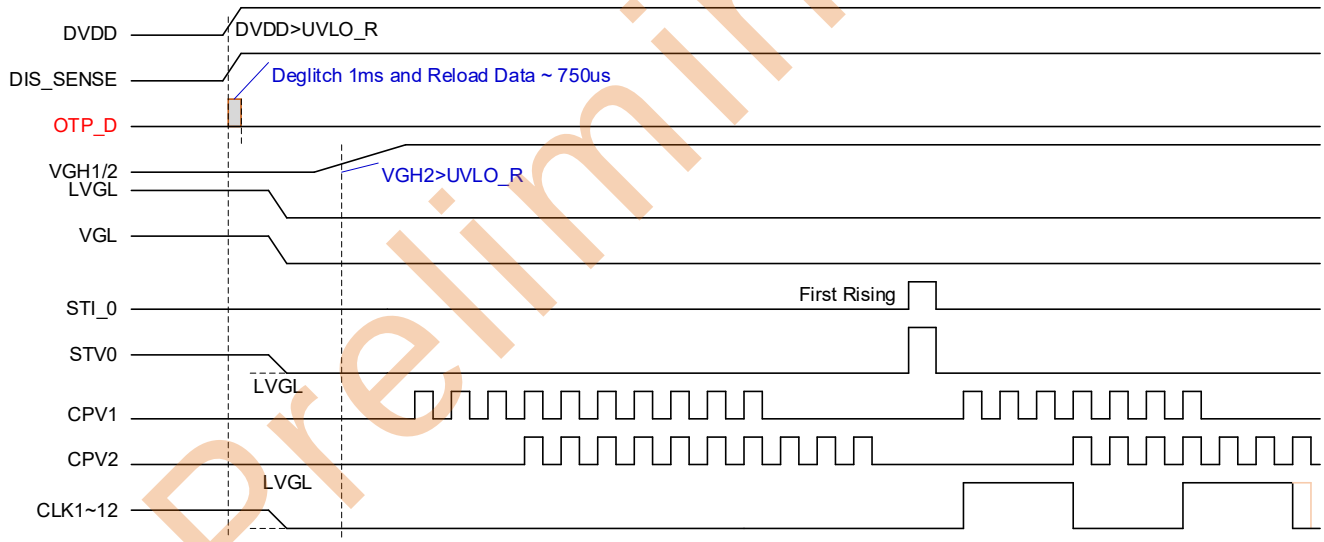
CLK1 to CLK12 output referred to for more detailed illustrations

CLK Enable Control – 0x05h[6]

Type1: STI_0 First Rising Don't control CLK output – 0x05h[6]=0



Type2: STI_0 First Rising Control CLK output – 0x05h[6]=1



CLK Output Control – Phase, Rotate, DLG and CPV control

Phase and Rotate setting

PHASE	0x06h[3:2] setting rotate mode			
	ROTATE MODE1	ROTATE MODE2	ROTATE MODE3	ROTATE MODE4
6Phase	1-2-3-4-5-6-1	4-5-6-1-2-3-4	3-2-1-6-5-4-3	6-5-4-3-2-1-6
8Phase	1-2-3-4-5-6-7-8-1	5-6-7-8-1-2-3-4-5	4-3-2-1-8-7-6-5-4	8-7-6-5-4-3-2-1-8
10Phase	1-2-3-4-5-6-7-8-9-10-1	6-7-8-9-10-1-2-3-4-5-6	5-4-3-2-1-10-9-8-7-6-5	10-9-8-7-6-5-4-3-2-1-10
12Phase	1-2-3-4-5-6-7-8-9-10-11-12-1	7-8-9-10-11-12-1-2-3-4-5-6-7	6-5-4-3-2-1-12-11-10-9-8-7-6	12-11-10-9-8-7-6-5-4-3-2-1-12

DLG mode 1

PHASE	Enter DLG mode by 0X08h or DLG_EN PIN, and 0x06h[1:0]=00(DLG MODE1)			
	ROTATE MODE1	ROTATE MODE2	ROTATE MODE3	ROTATE MODE4
6Phase	1=2	4=5	3=2	6=5
	3=4	6=1	1=6	4=3
	5=6	2=3	5=4	2=1
	1=2	4=5	3=2	6=5
8Phase	1=2	5=6	4=3	8=7
	3=4	7=8	2=1	6=5
	5=6	1=2	8=7	4=3
	7=8	3=4	6=5	2=1
	1=2	5=6	4=3	8=7
10Phase	1=2	6=7	5=4	10=9
	3=4	8=9	3=2	8=7
	5=6	10=1	1=10	6=5
	7=8	2=3	9=8	4=3
	9=10	4=5	7=6	2=1
	1=2	6=7	5=4	10=9
12Phase	1=2	7=8	6=5	12=11
	3=4	9=10	4=3	10=9
	5=6	11=12	2=1	8=7
	7=8	1=2	12=11	6=5
	9=10	3=4	10=9	4=3
	11=12	5=6	8=7	2=1
	1=2	7=8	6=5	12=11

DLG mode 2

PHASE	Enter DLG mode by 0X08h or DLG_EN PIN, and 0x06h[1:0]=01(DLG MODE2)			
	ROTATE MODE1	ROTATE MODE2	ROTATE MODE3	ROTATE MODE4
6Phase	1=4	4=1	3=6	6=3
	2=5	5=2	2=5	5=2
	3=6	3=6	1=4	4=1
	1=4	4=1	3=6	6=3
8Phase	1=5	5=1	4=8	8=4
	2=6	6=2	3=7	7=3
	3=7	7=3	2=6	6=2
	4=8	8=4	1=5	5=1
	1=5	5=1	4=8	8=4
10Phase	1=6	6=1	5=10	10=5
	2=7	7=2	4=9	9=4
	3=8	8=3	3=8	8=3
	4=9	9-4	2=7	7=2
	5=10	10=5	1=6	6=1
	1=6	6=1	5=10	10=5
12Phase	1=7	7=1	6=12	12=6
	2=8	8=2	5=11	11=5
	3=9	9=3	4=10	10=4
	4=10	10=4	3=9	9=3
	5=11	11=5	2=8	8=2
	6=12	12=6	1=7	7=1
	1=7	7=1	6=12	12=6

DLG mode 3

PHASE	Enter DLG mode by 0X08h or DLG_EN PIN, and 0x06h[1:0]=10(DLG MODE3)			
	ROTATE MODE1	ROTATE MODE2	ROTATE MODE3	ROTATE MODE4
8Phase	1=3	5=7	4=2	8=6
	2=4	6=8	3=1	7=5
	5=7	1=3	8=6	4=2
	6=8	2=4	7=5	3=1
	1=3	5=7	4=2	8=6
12Phase	1=3	7=9	6=4	12=10
	2=4	8=10	5=3	11=9
	5=7	11=1	2=12	8=6
	6=8	12=2	1=11	7=5
	9=11	3=5	10=8	4=2
	10=12	4=6	9=7	3=1
	1=3	7=9	6=4	12=10

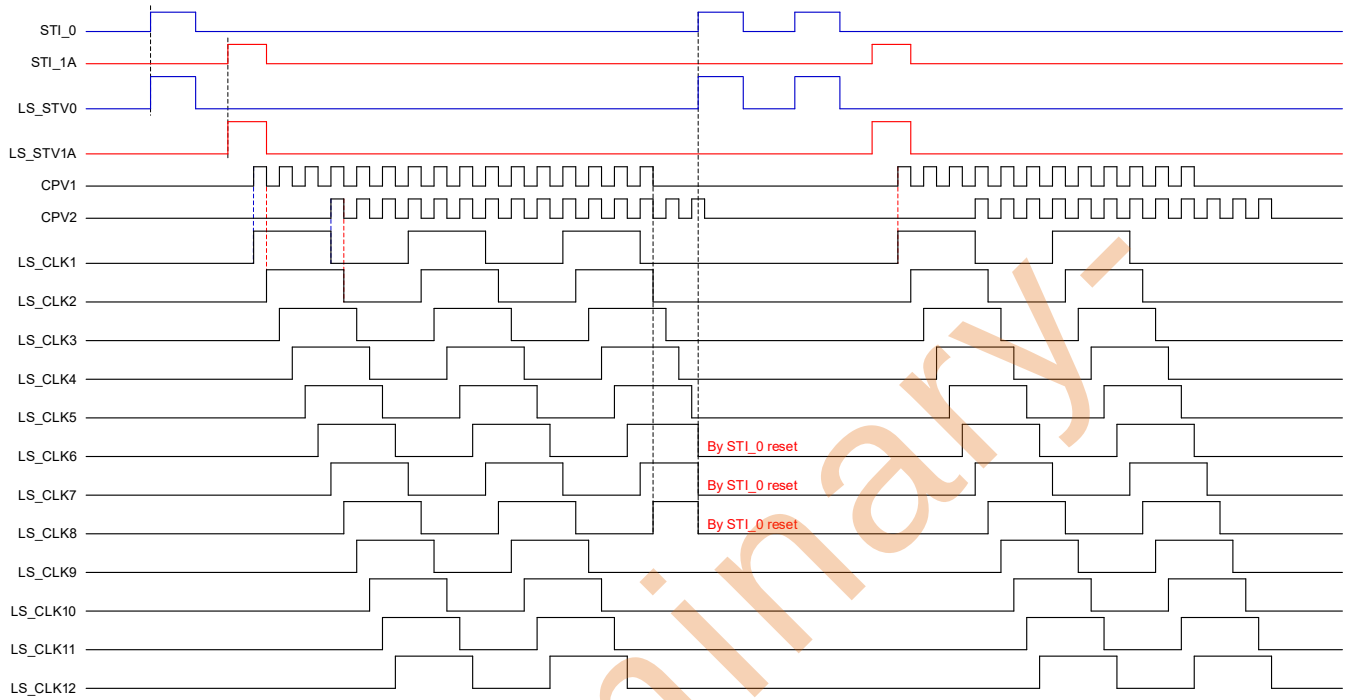
DLG mode 4

PHASE	Enter DLG mode by 0X08h or DLG_EN PIN, and 0x06h[1:0]=11(DLG MODE4)			
	ROTATE MODE1	ROTATE MODE2	ROTATE MODE3	ROTATE MODE4
12Phase	1=4	7=10	6=3	12=9
	2=5	8=11	5=2	11=8
	3=6	9=12	4=1	10=7
	7=10	1=4	12=9	6=3
	8=11	2=5	11=8	5=2
	9=12	3=6	10=7	4=1
	1=4	7=10	6=3	12=9

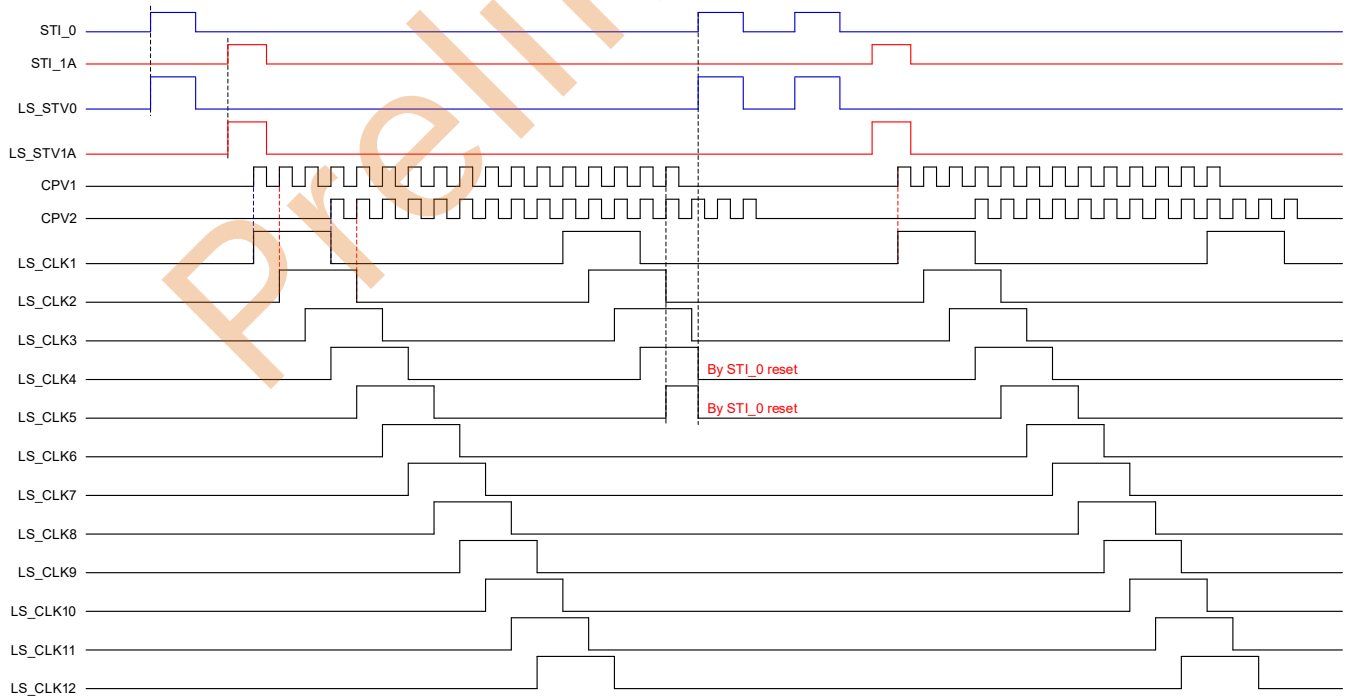
CLK Typical output waveform

1. Example of CPV input excitation pattern

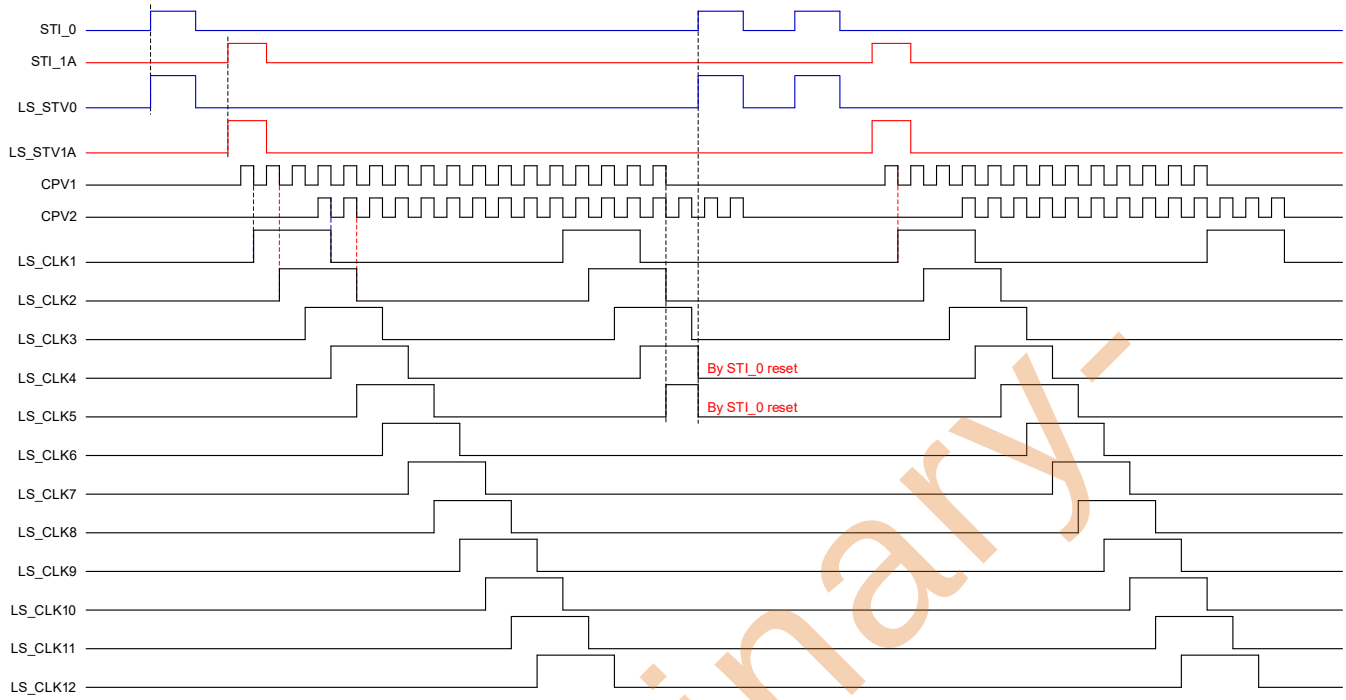
Type: 12-phase, CPV Rising and Falling control



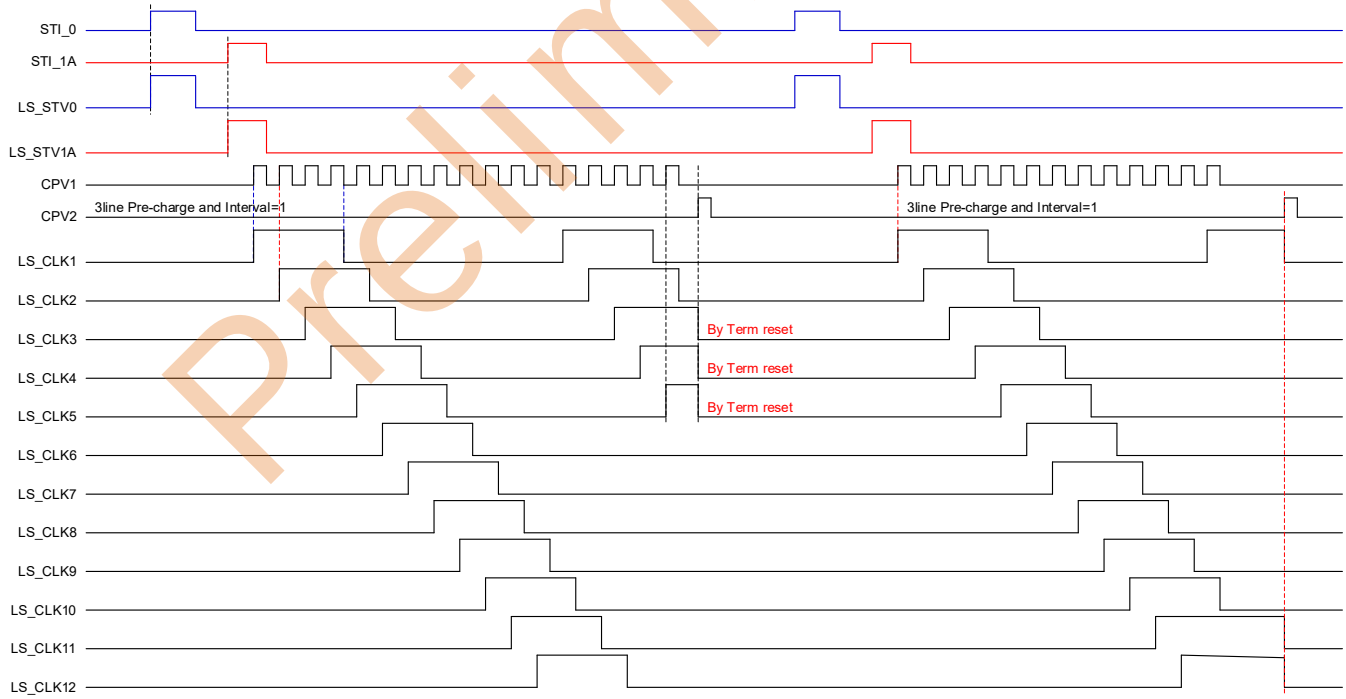
Type: 12-phase, CPV Only Rising control



Type: 12-phase, , CPV Only Falling control

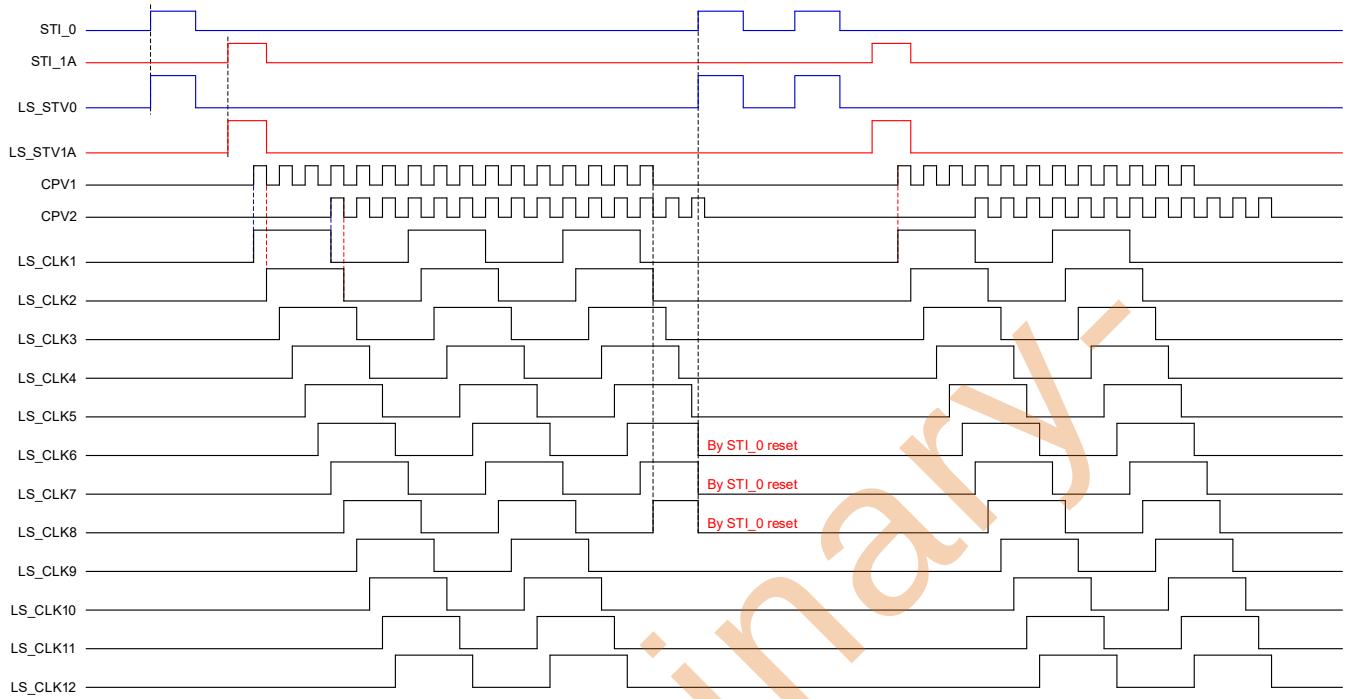


Type: 12-phase, , 1line Input Control Only CPV1 control, CPV2 is Terminal Function

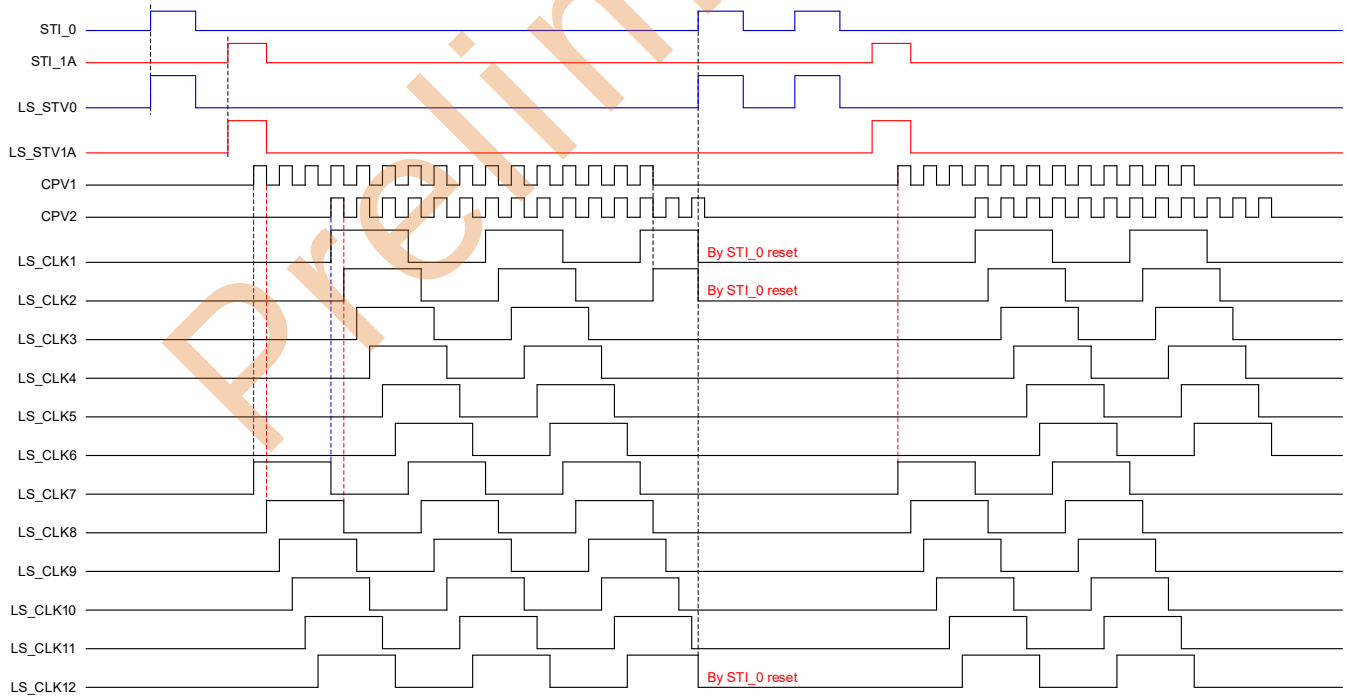


2. Example of CLK Rotate mode

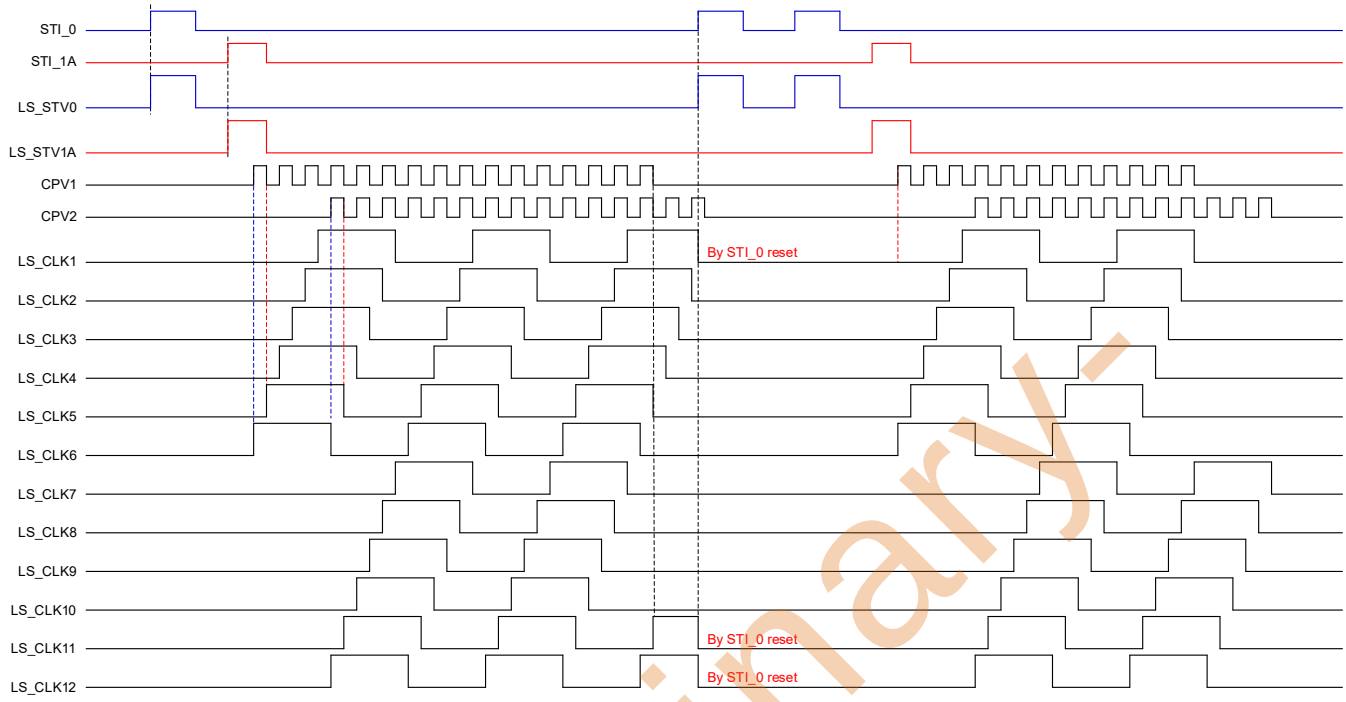
Type: 12-phase, CPV rising and Falling control, Rotate mode1



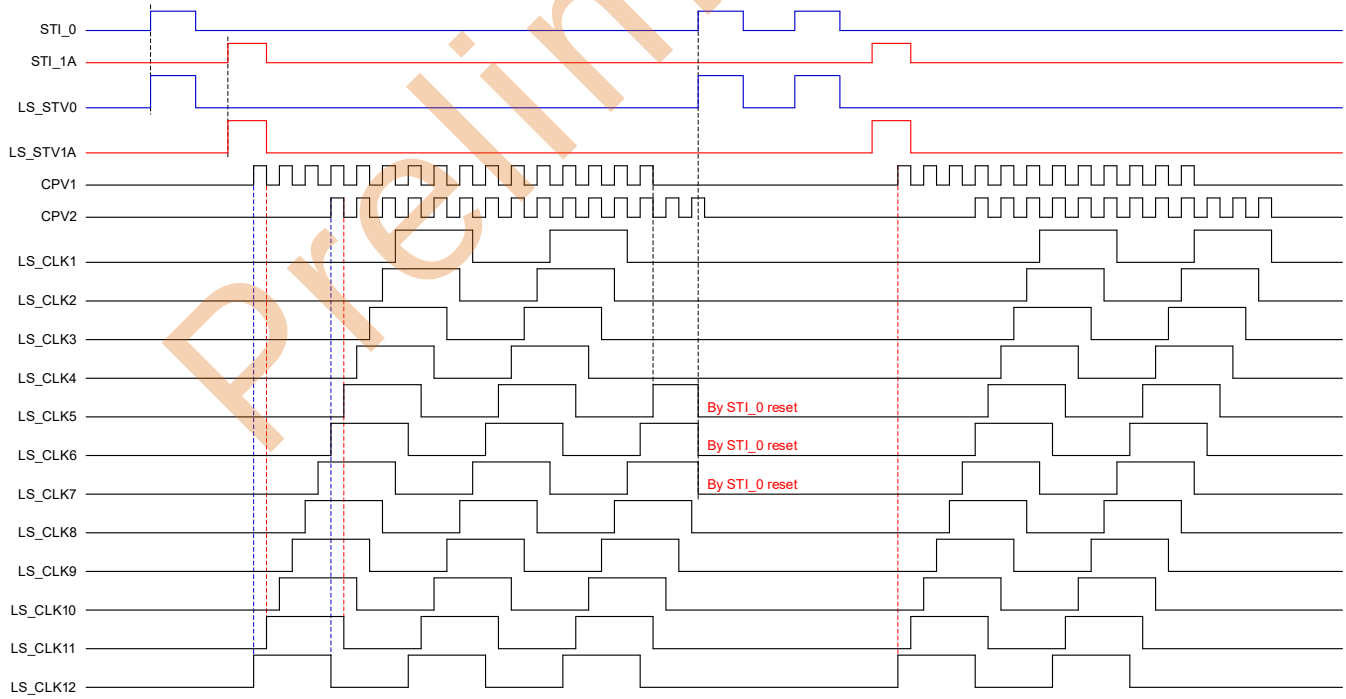
Type: 12-phase, CPV rising and Falling control, Rotate mode2



Type: 12-phase, CPV rising and Falling control, Rotate mode3

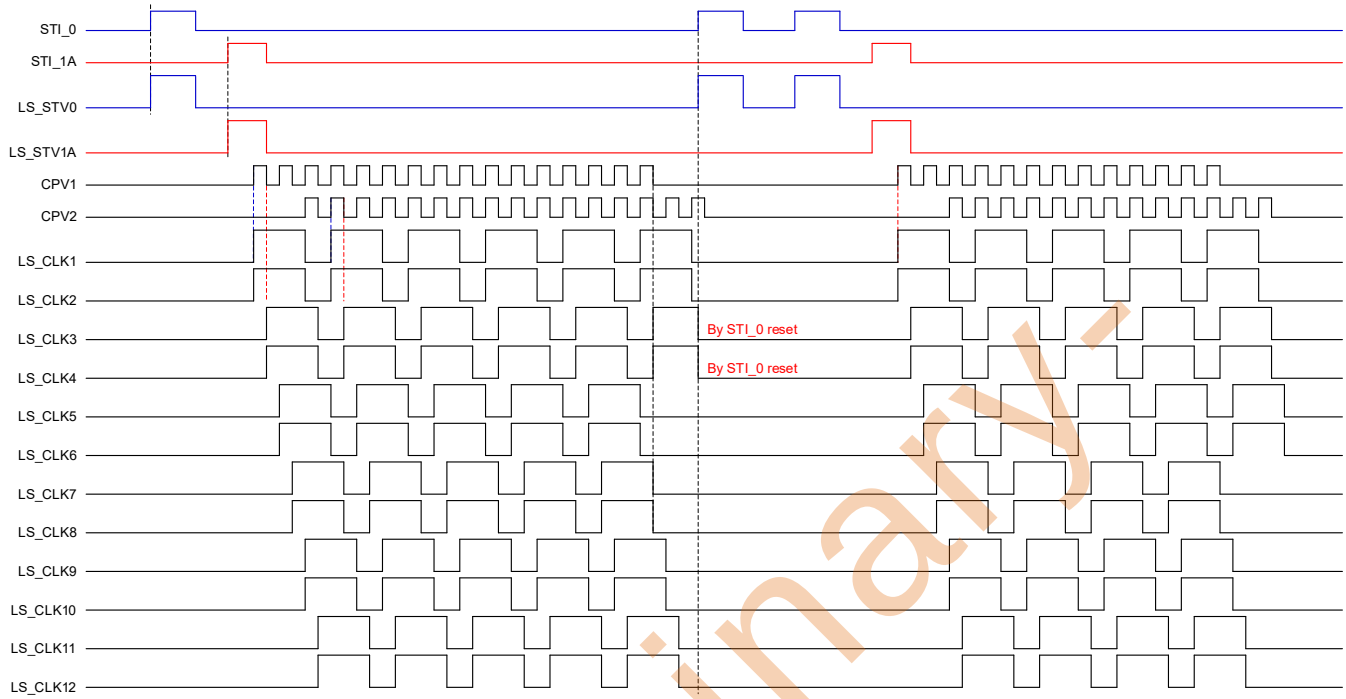


Type: 12-phase, CPV rising and Falling control, Rotate mode4

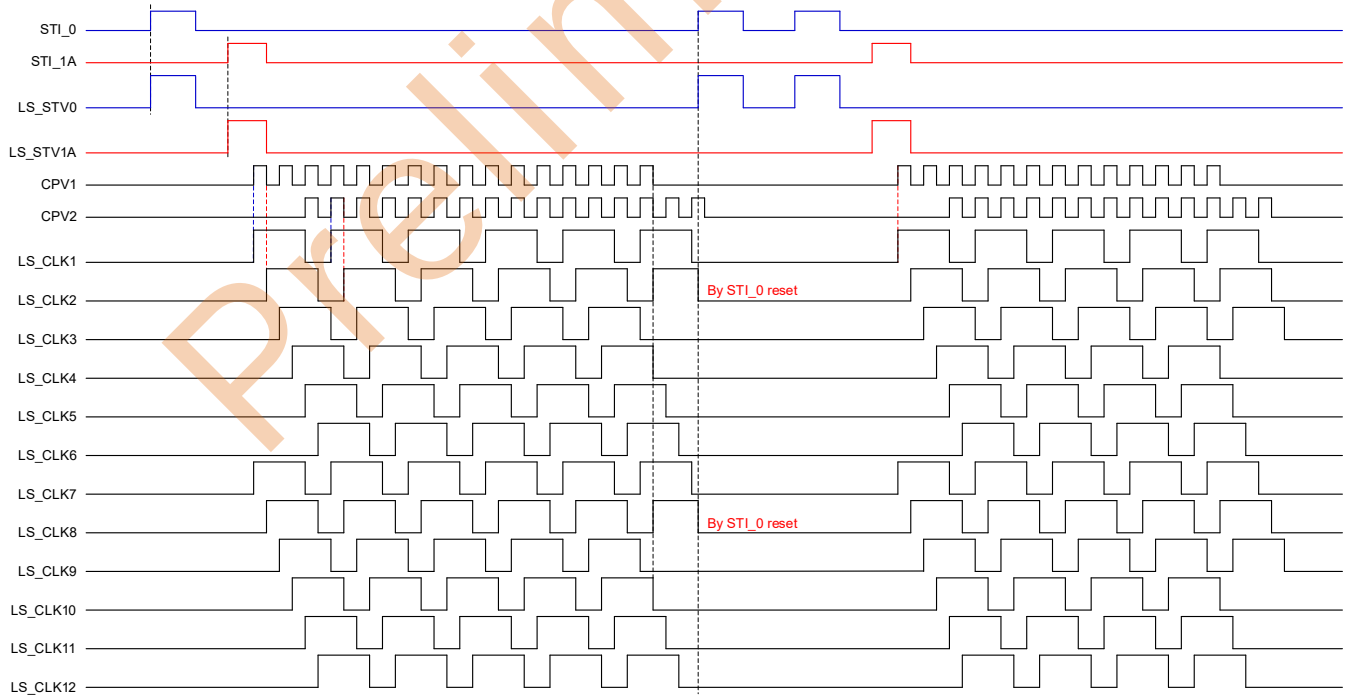


3. Example of CLK DLG mode@Rotate mode1

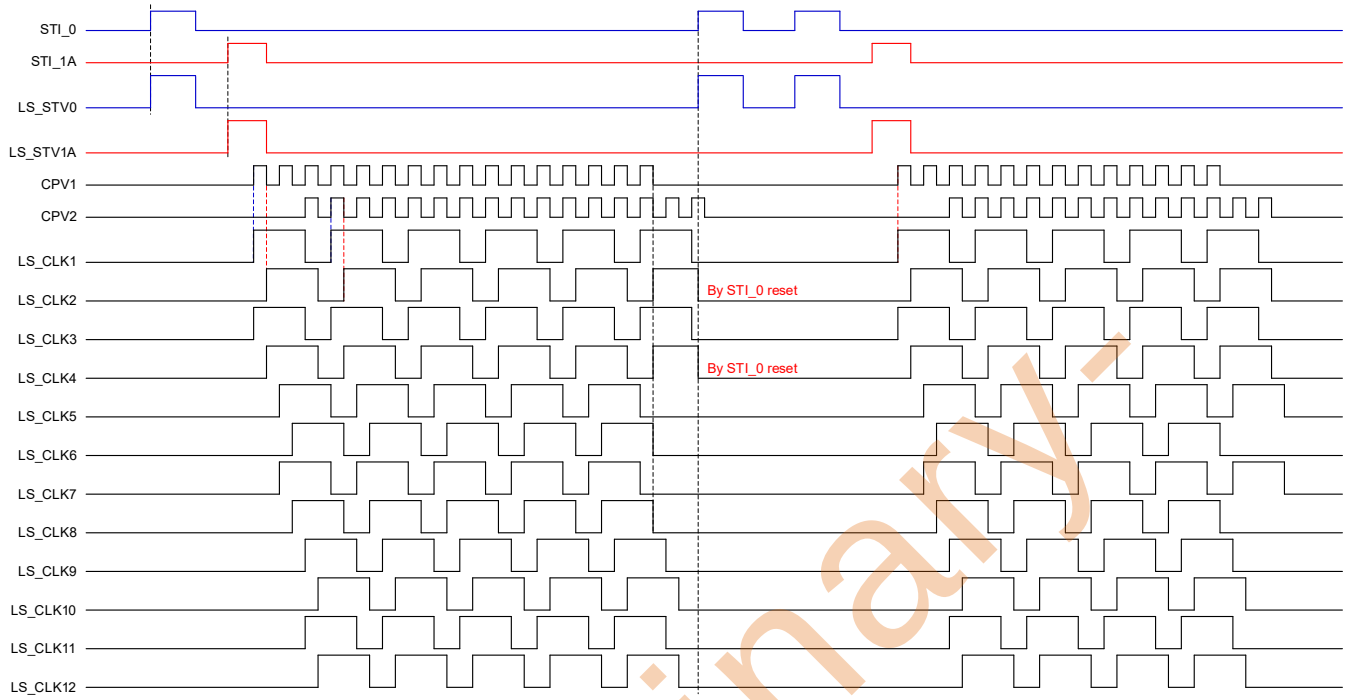
Type: 12-phase, DLG mode1, CPV rising and Falling control, Rotate mode1



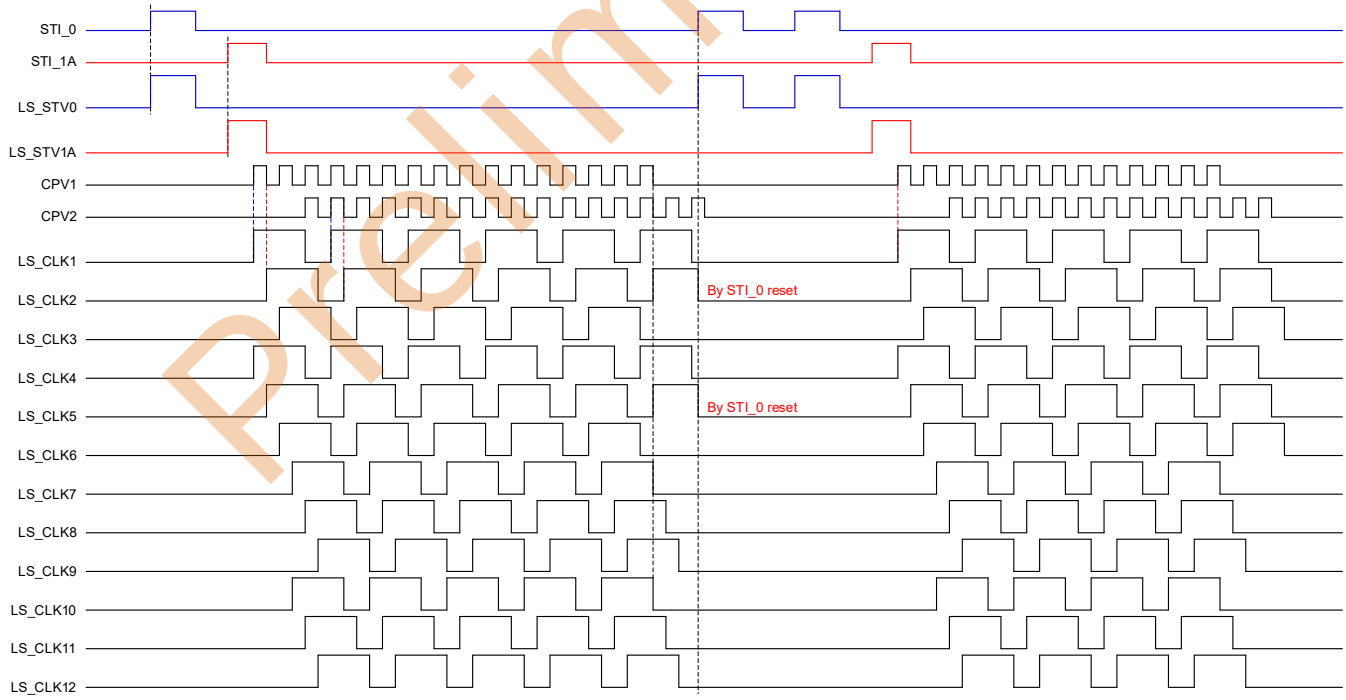
Type: 12-phase, DLG mode2, CPV rising and rising control, Rotate mode1



Type: 12-phase, DLG mode3, CPV rising and falling control, Rotate mode1

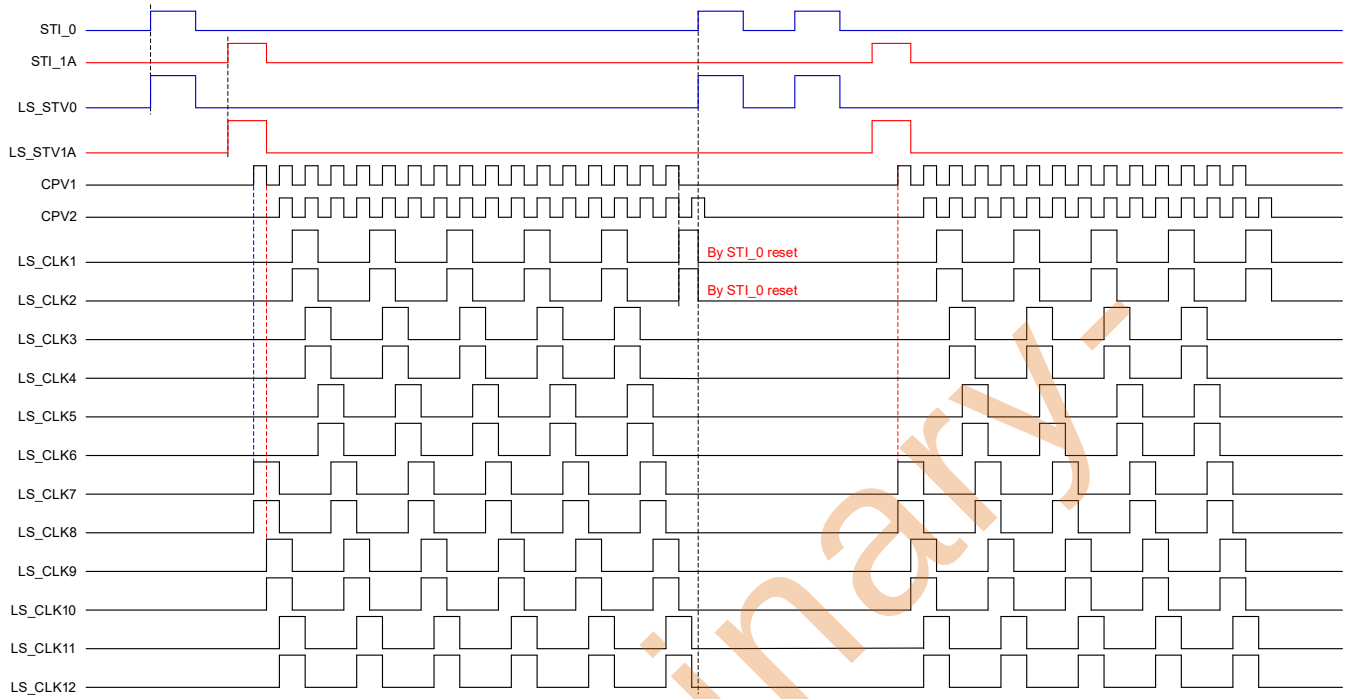


Type: 12-phase, DLG mode3, CPV rising and falling control, Rotate mode1

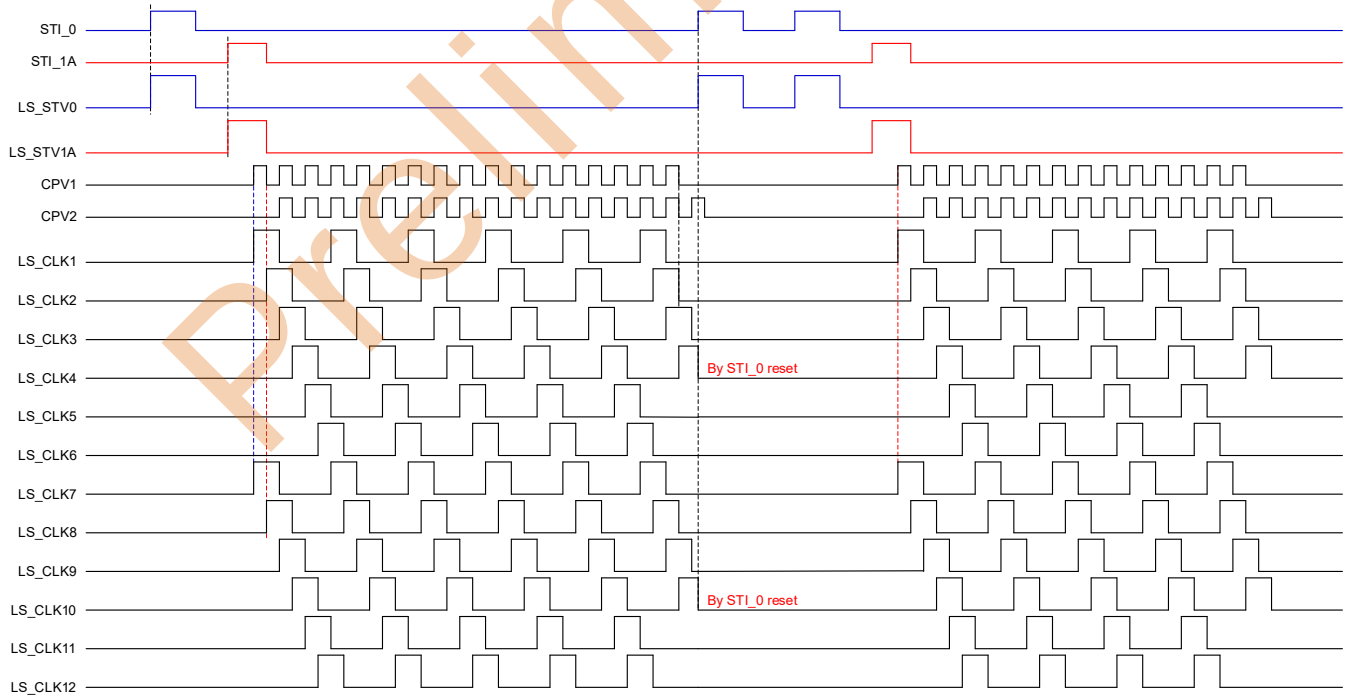


4. Example of CLK DLG mode@Rotate mode2

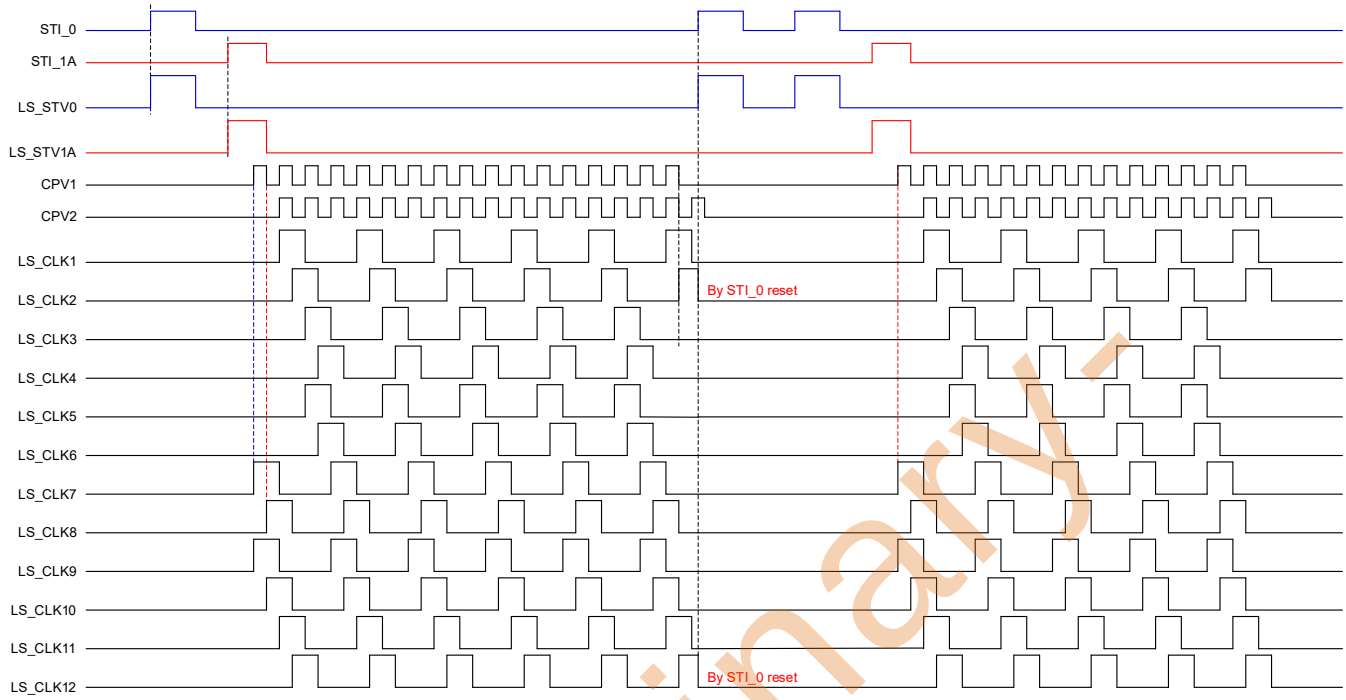
Type: 12-phase, DLG mode1, CPV rising and Falling control, Rotate mode2



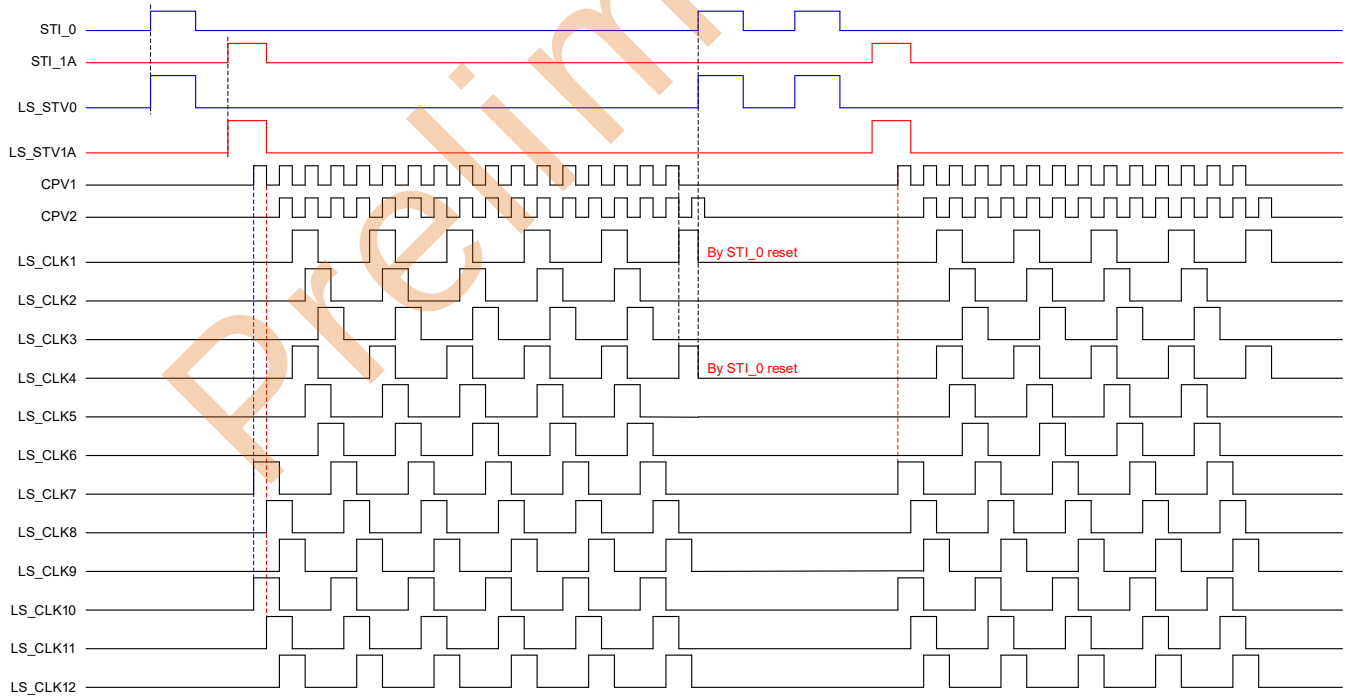
Type: 12-phase, DLG mode2, CPV rising and Falling control, Rotate mode2



Type: 12-phase, DLG mode3, CPV rising and Falling control, Rotate mode2

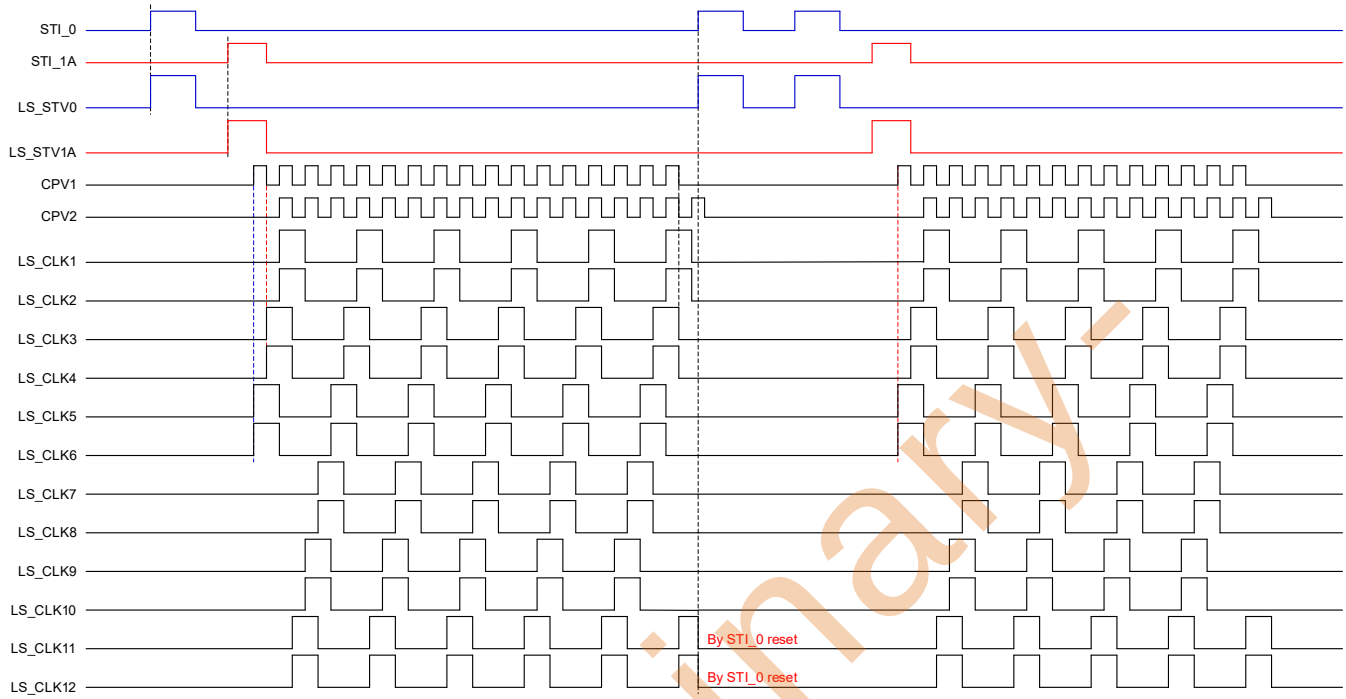


Type: 12-phase, DLG mode4, CPV rising and Falling control, Rotate mode2

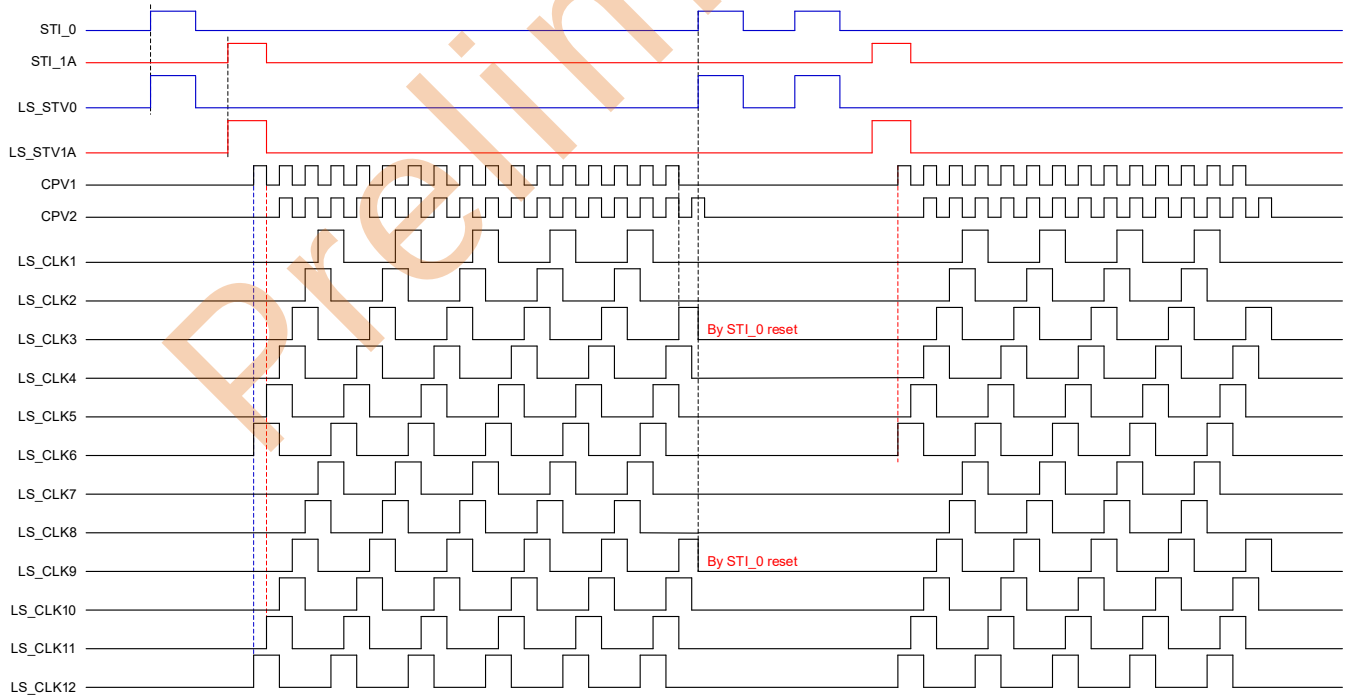


5. Example of CLK DLG mode@Rotate mode3

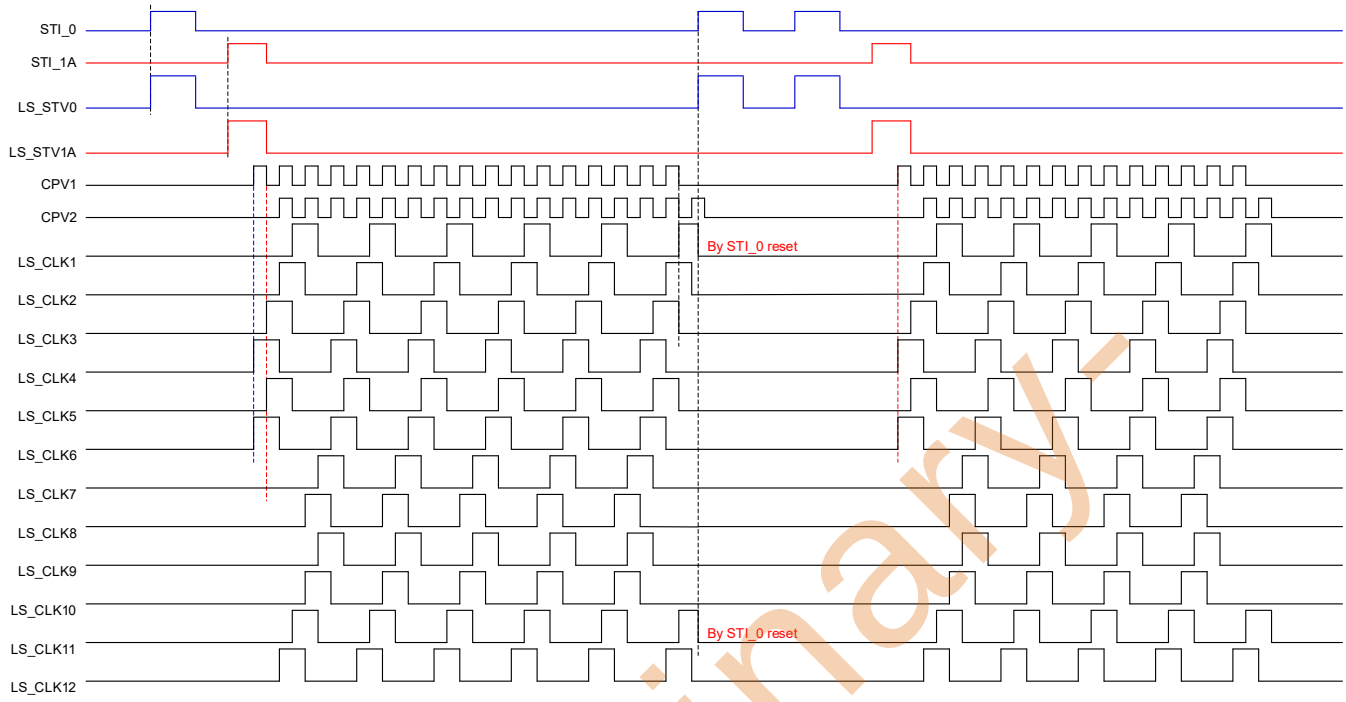
Type: 12-phase, DLG mode1, CPV rising and Falling control, Rotate mode3



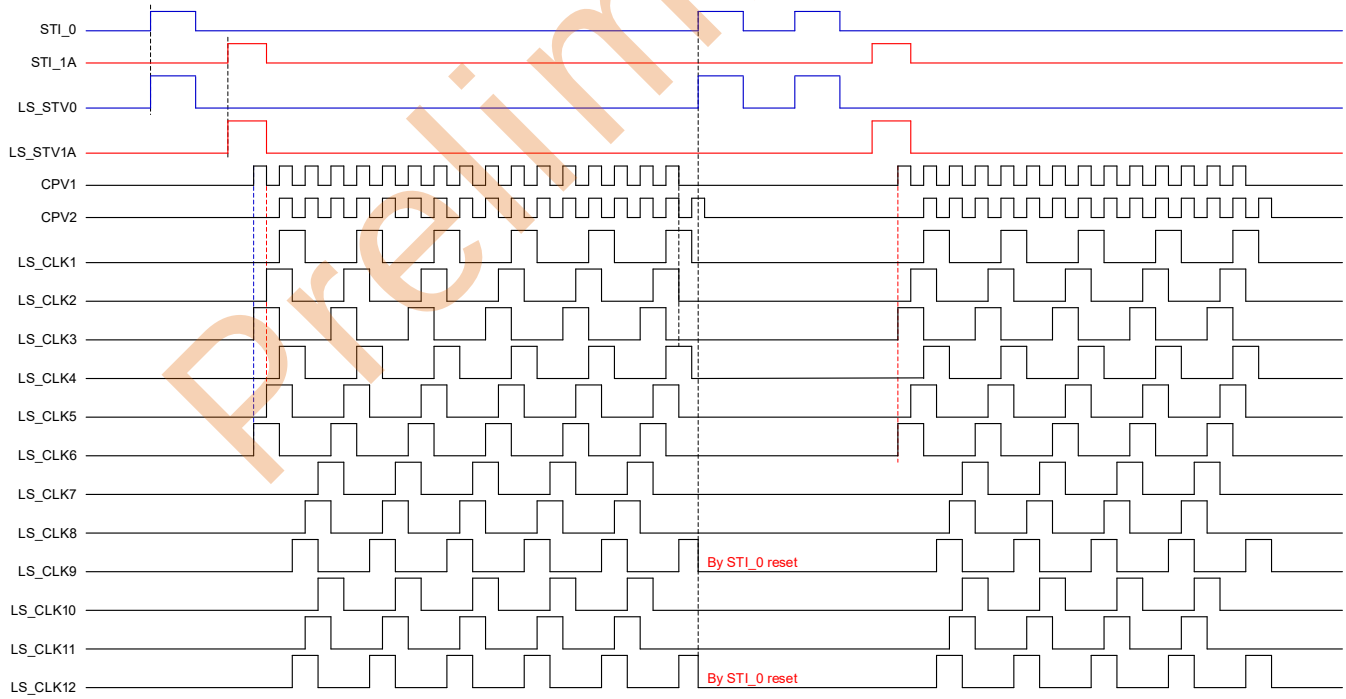
Type: 12-phase, DLG mode2, CPV rising and Falling control, Rotate mode3



Type: 12-phase, DLG mode3, CPV rising and Falling control, Rotate mode3

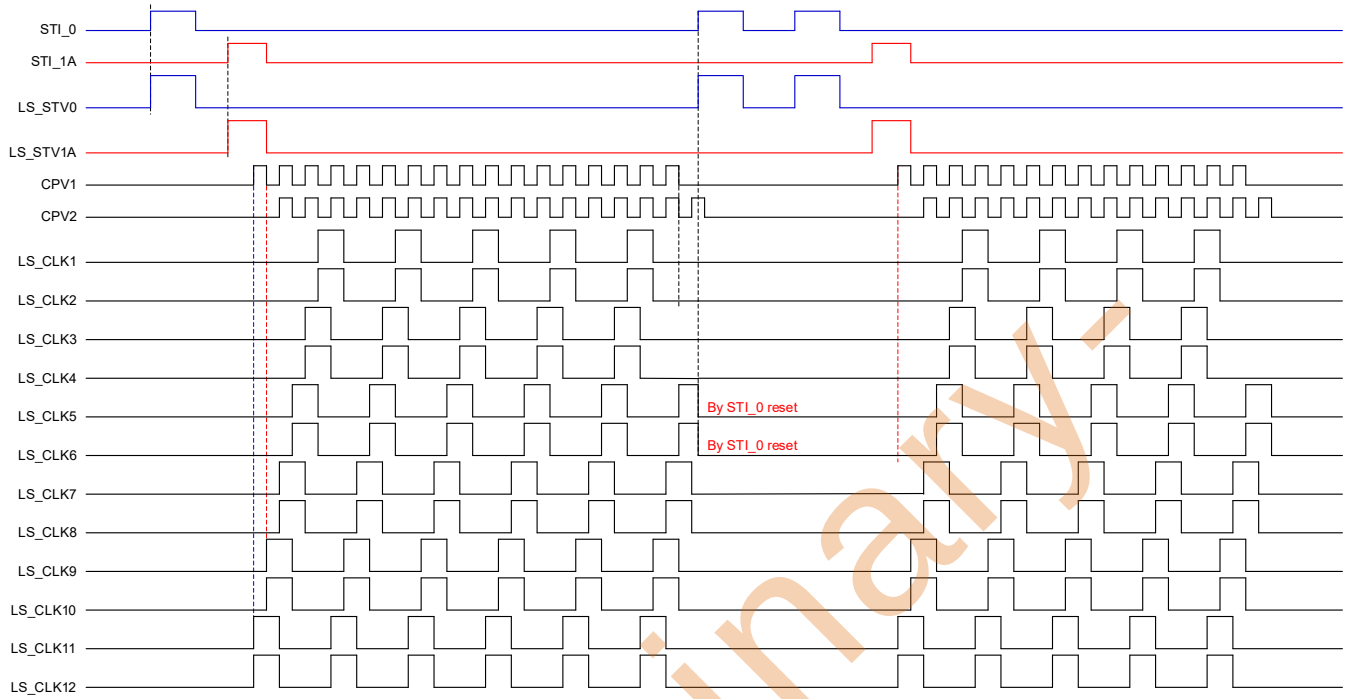


Type: 12-phase, DLG mode4, CPV rising and Falling control, Rotate mode3

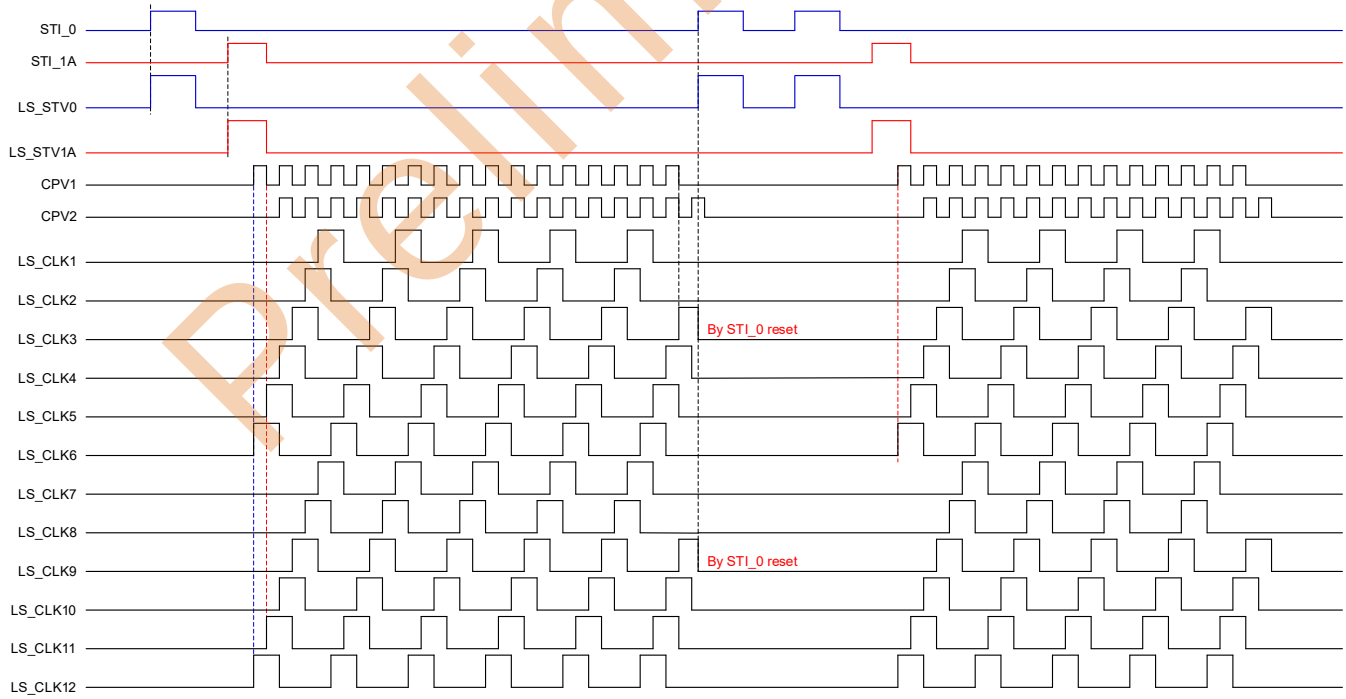


6. Example of CLK DLG mode@Rotate mode4

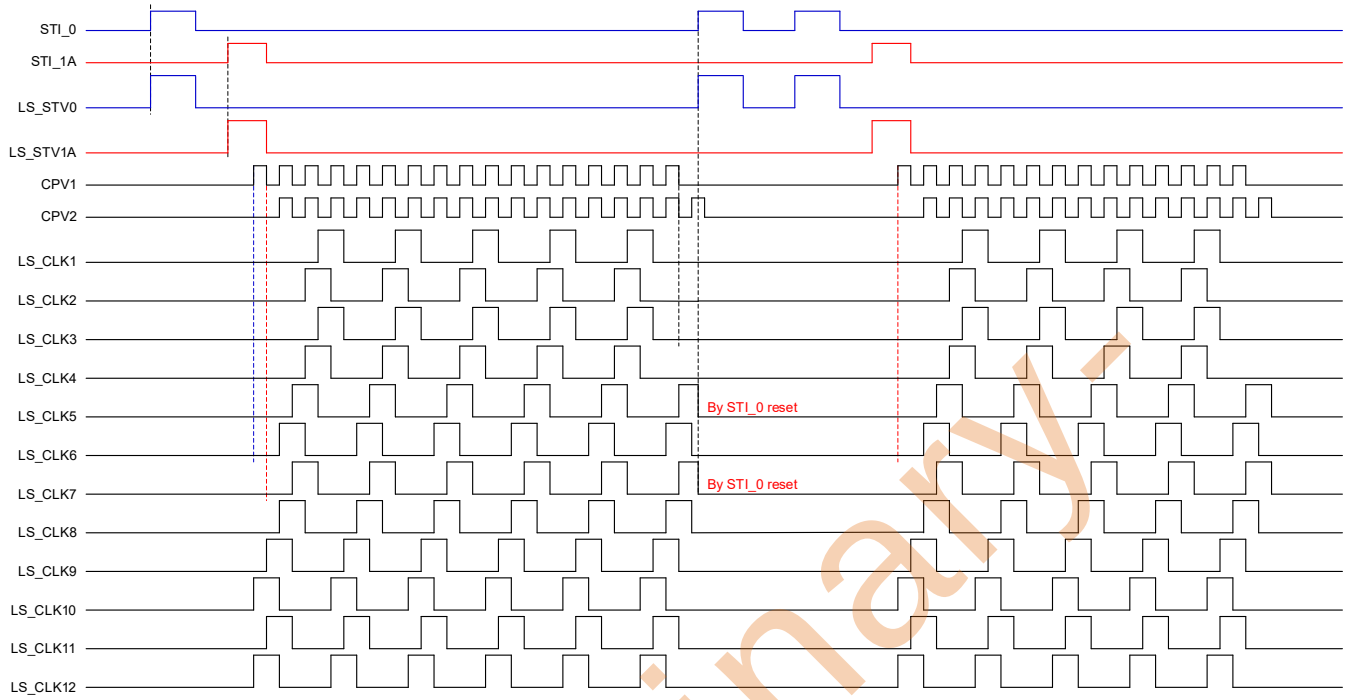
Type: 12-phase, DLG mode1, CPV rising and Falling control, Rotate mode4



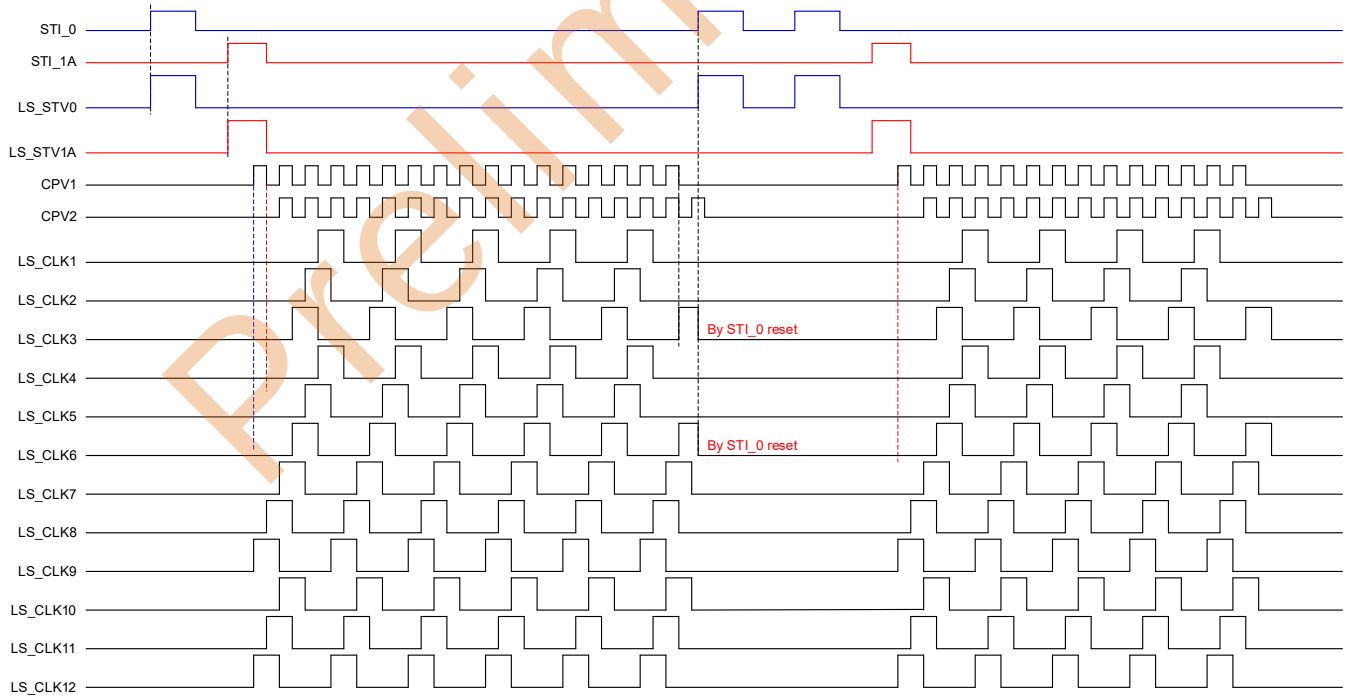
Type: 12-phase, DLG mode2, CPV rising and Falling control, Rotate mode4



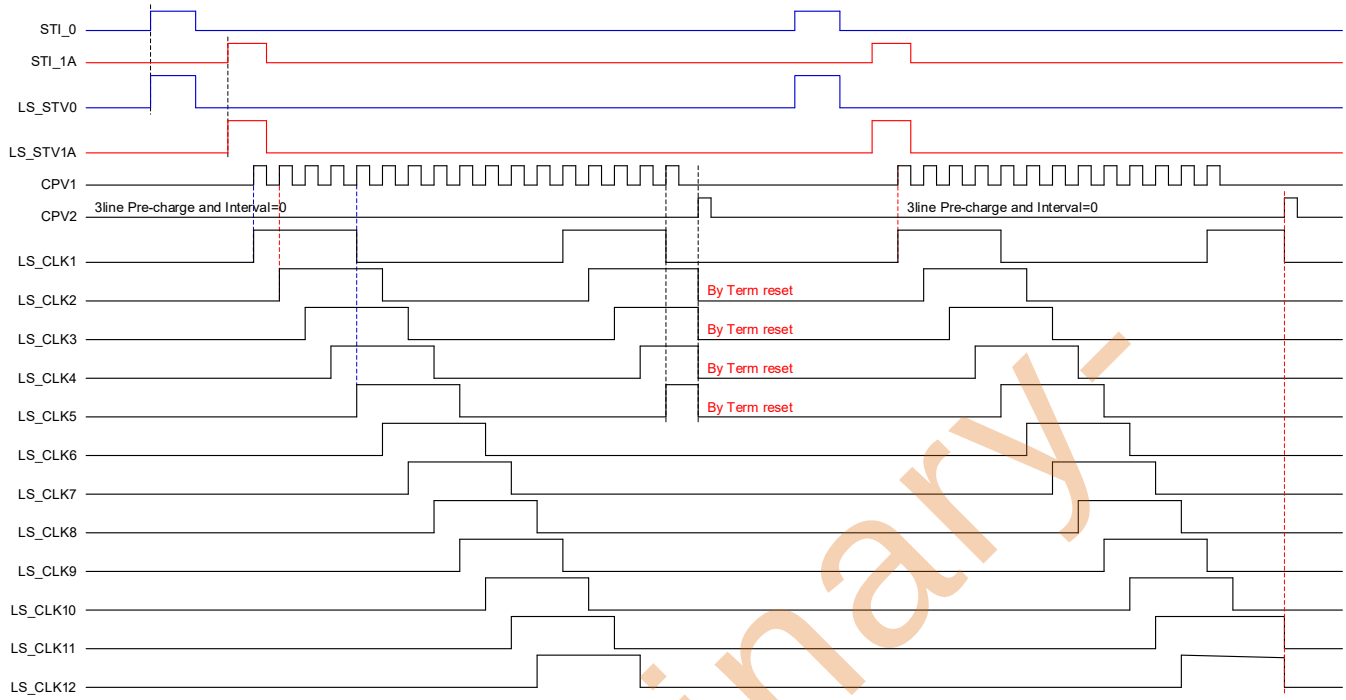
Type: 12-phase, DLG mode3, CPV rising and Falling control, Rotate mode4



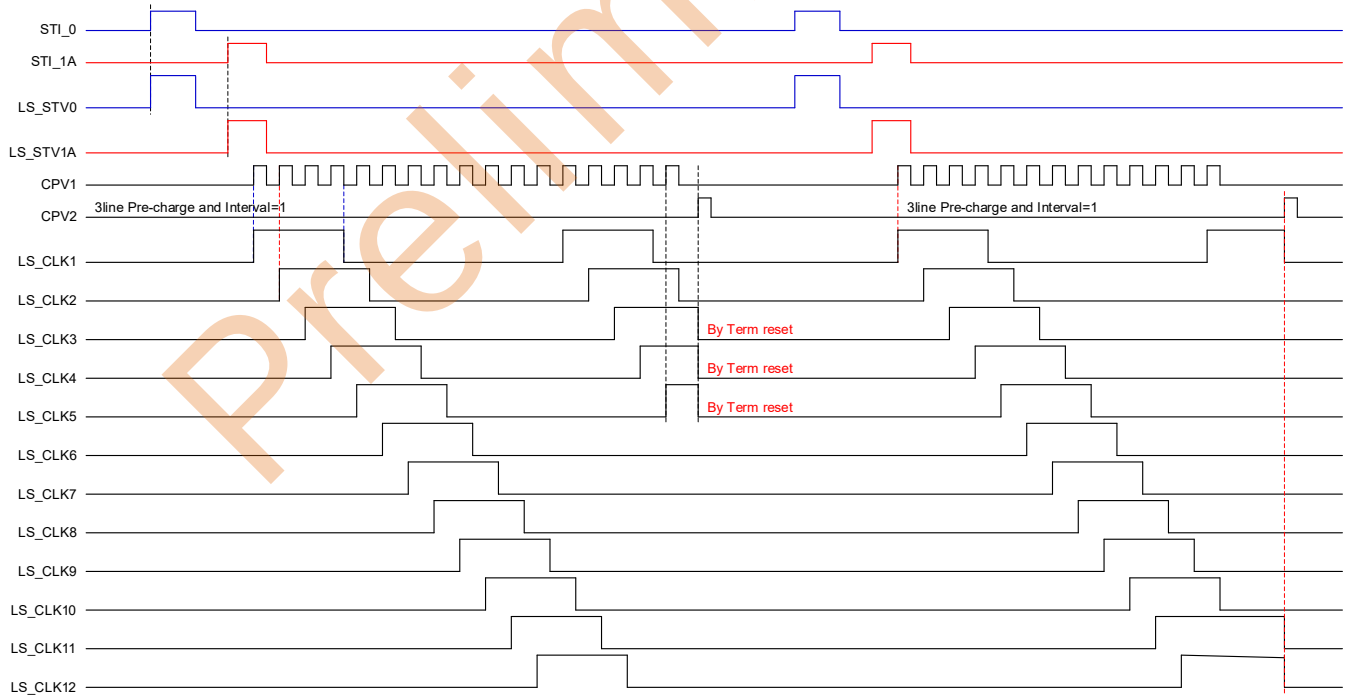
Type: 12-phase, DLG mode4, CPV rising and Falling control, Rotate mode4



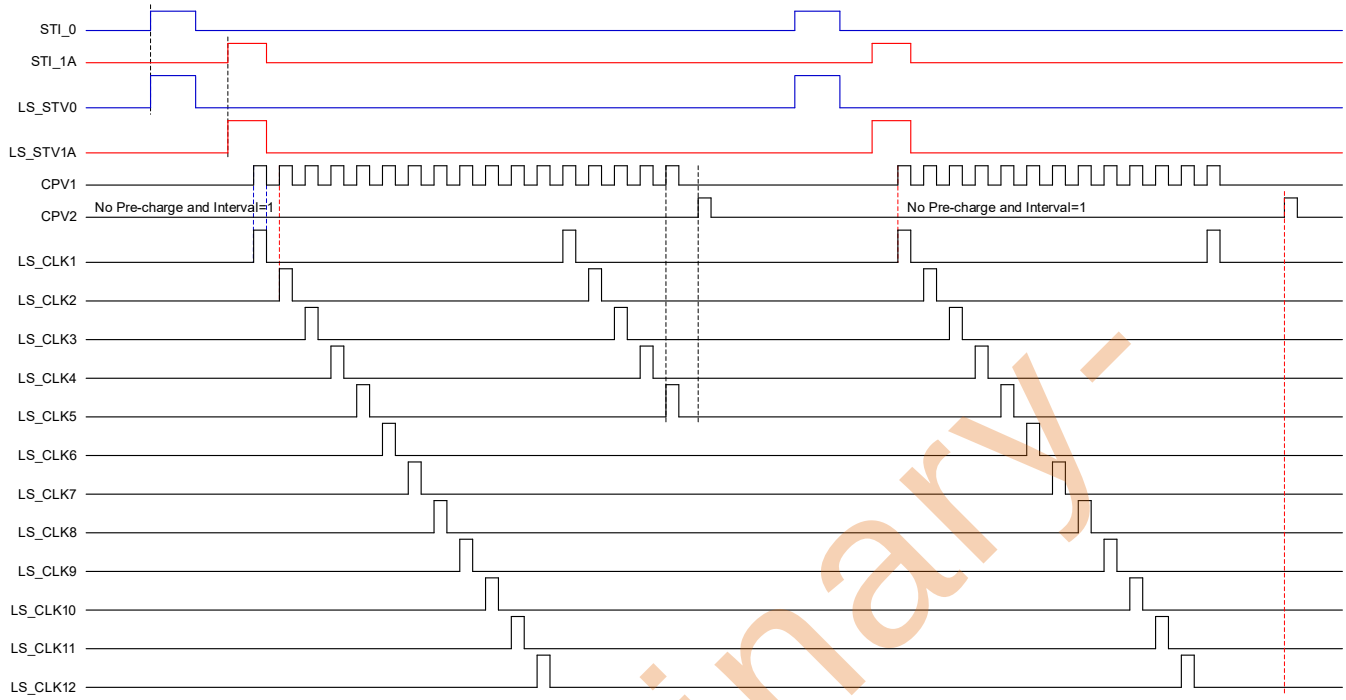
Type: 12-phase, 1line input mode and pre-charge select – No interval =0



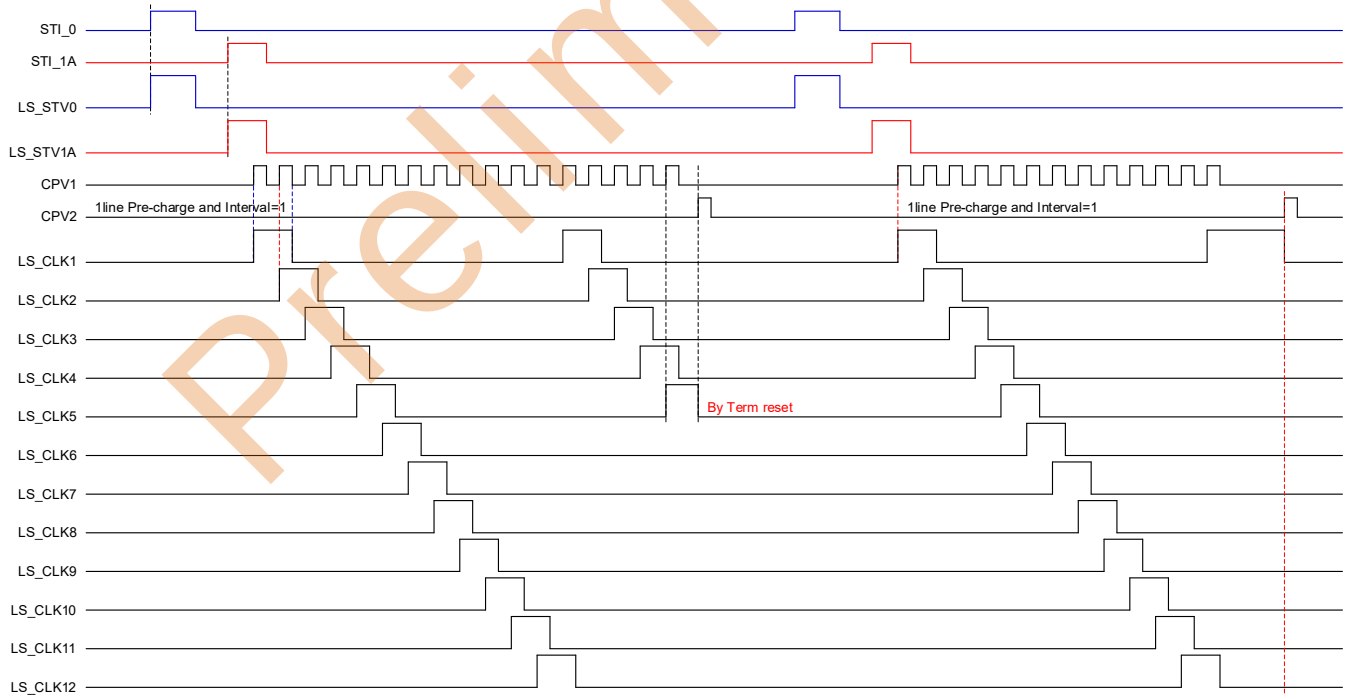
Type: 12-phase, 1line input mode and pre-charge select – Interval =1



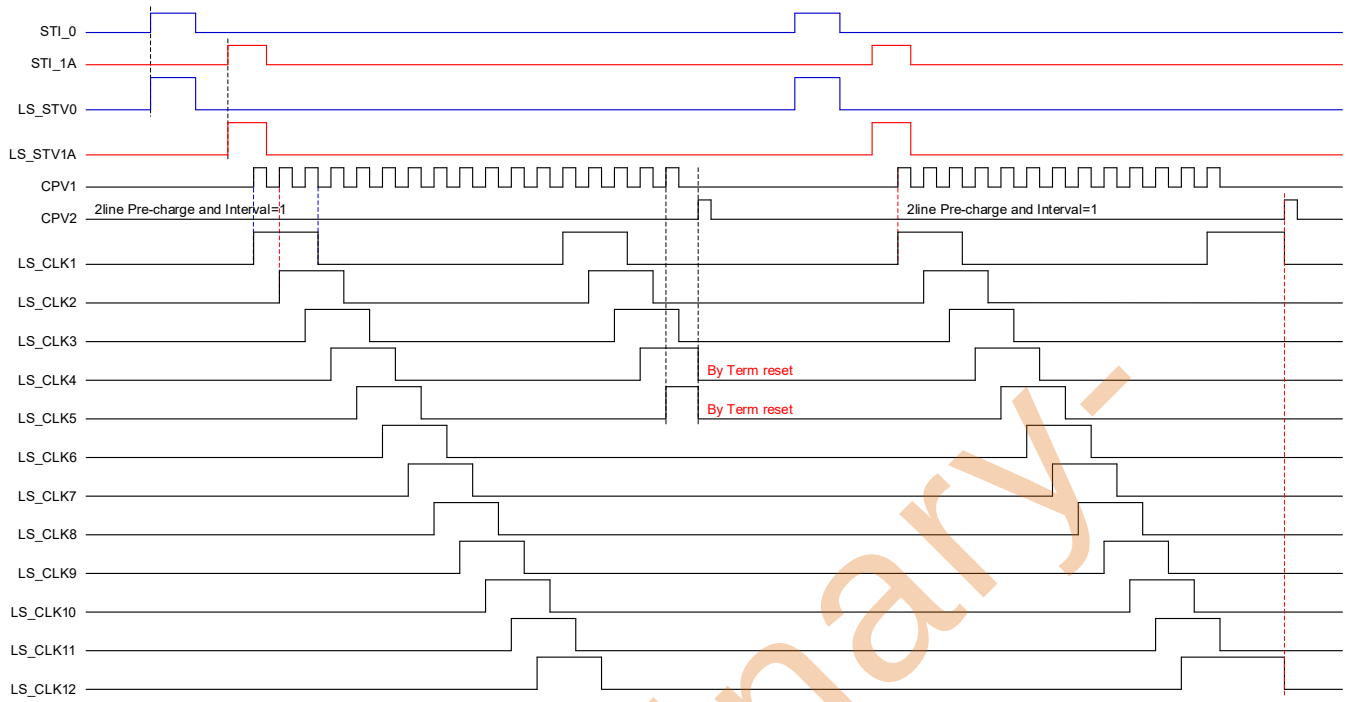
Type: 12-phase, 1line input mode and No pre-charge



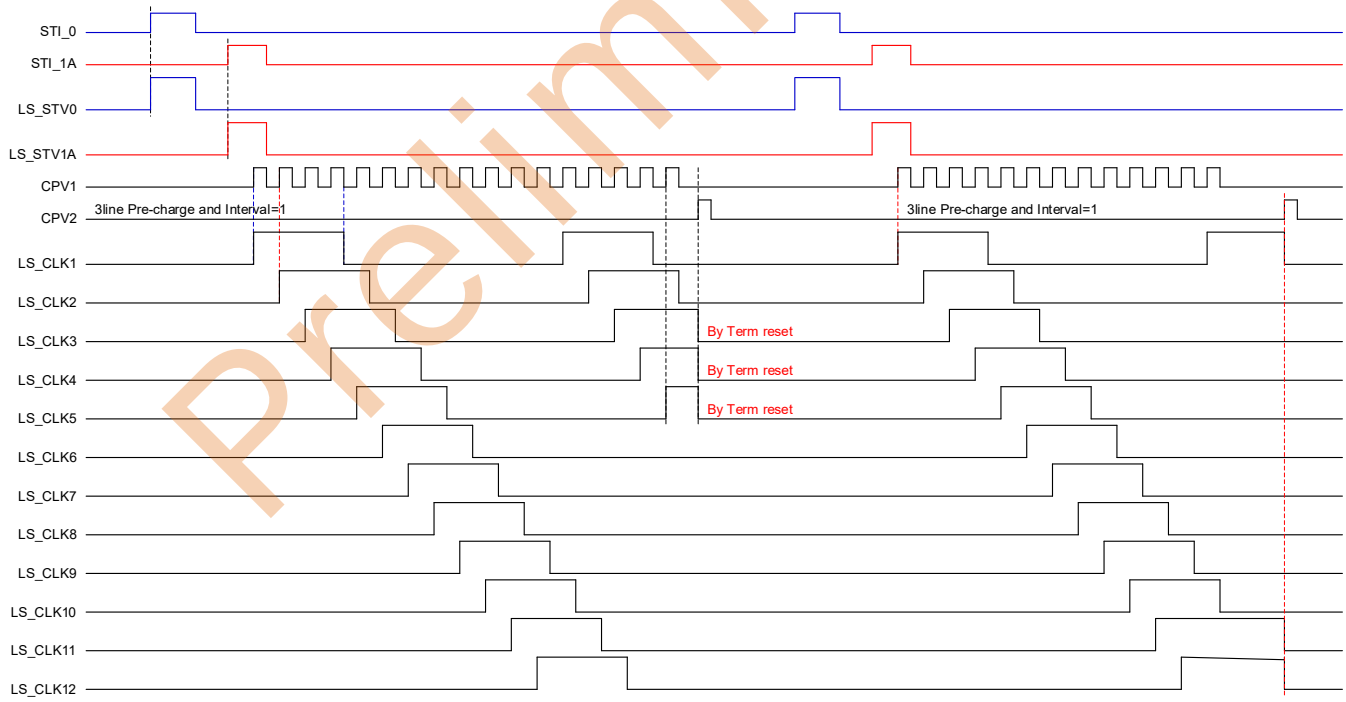
Type: 12-phase, 1line input mode and 1line pre-charge



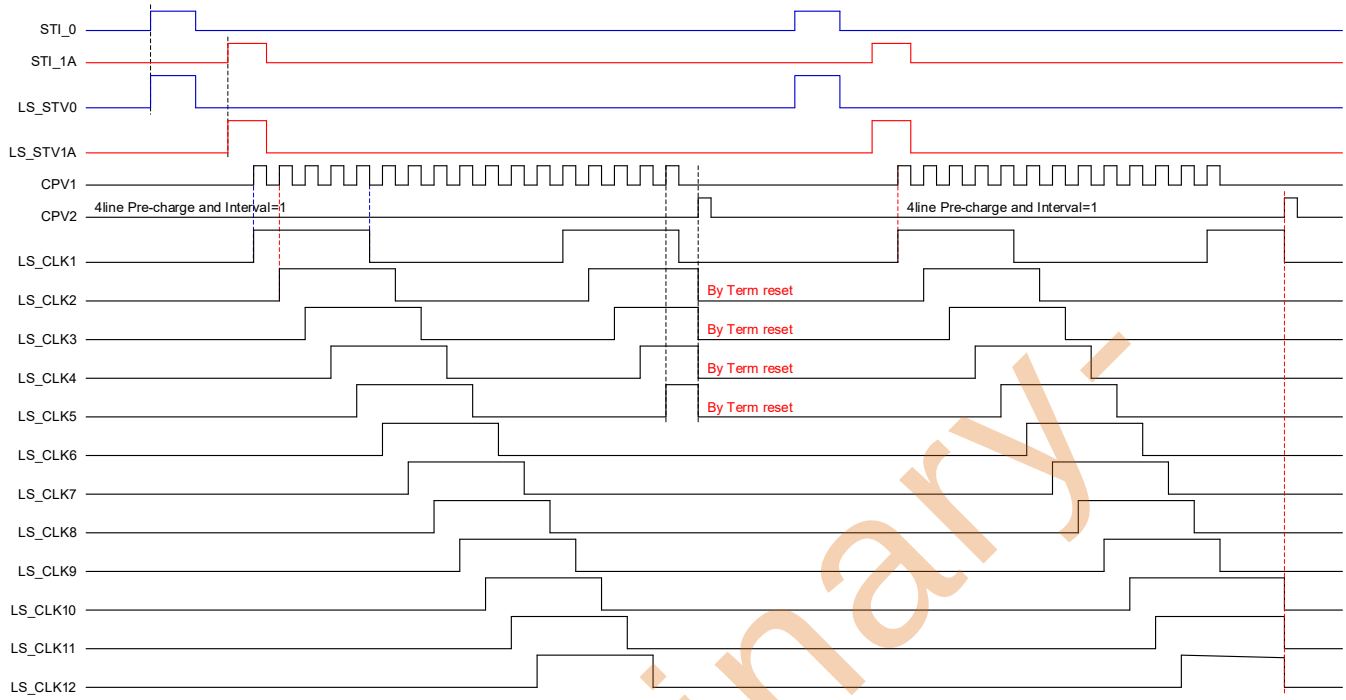
Type: 12-phase, 1line input mode and 2line pre-charge



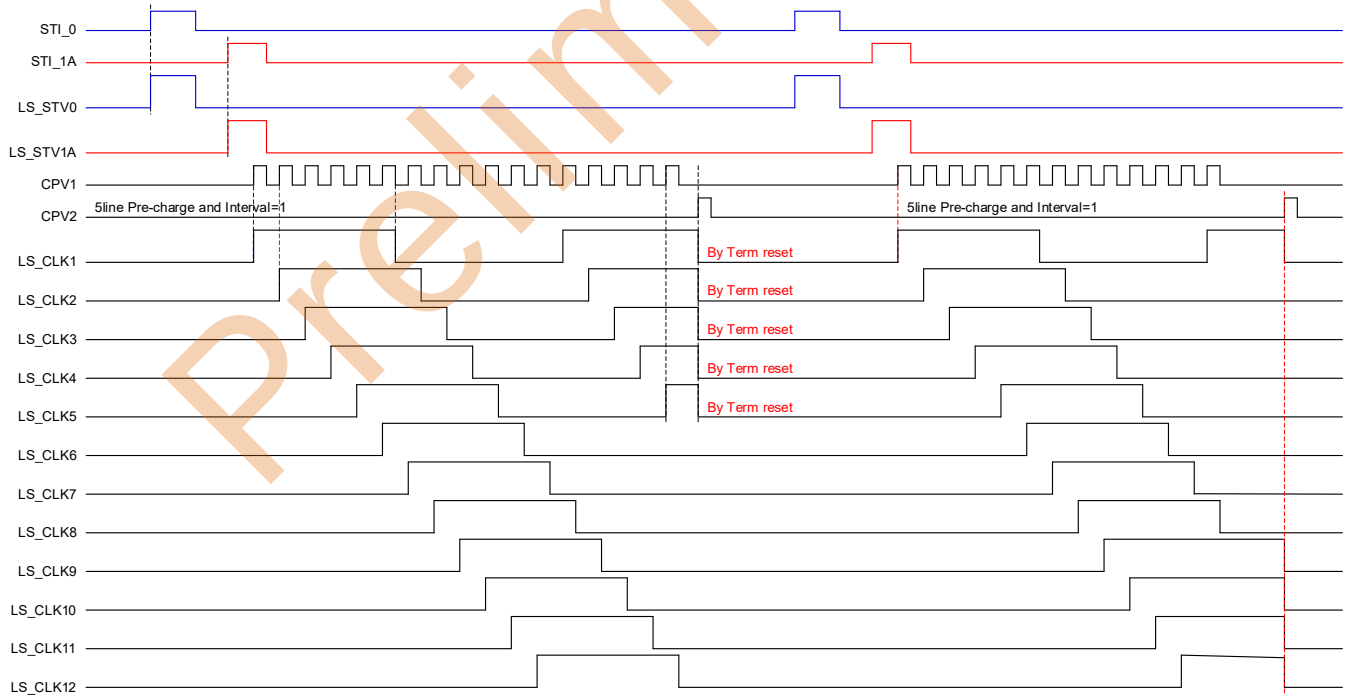
Type: 12-phase, 1line input mode and 3line pre-charge



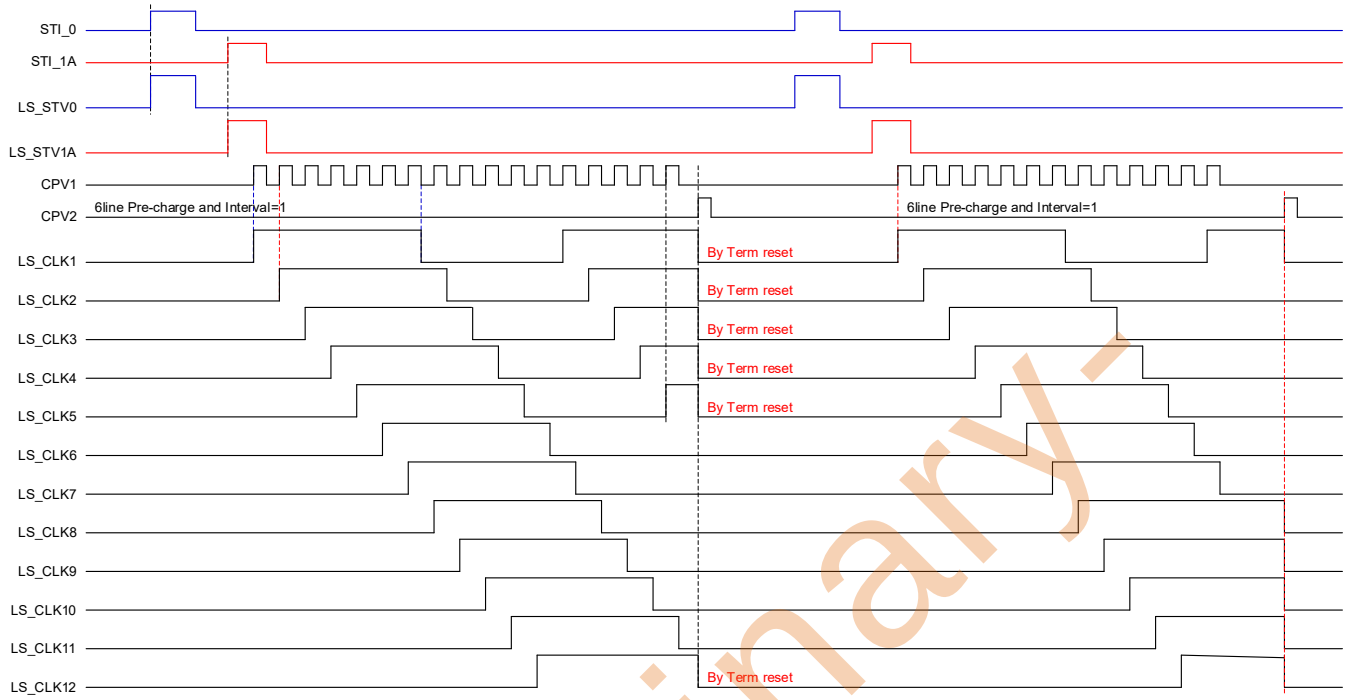
Type: 12-phase, 1line input mode and 4line pre-charge



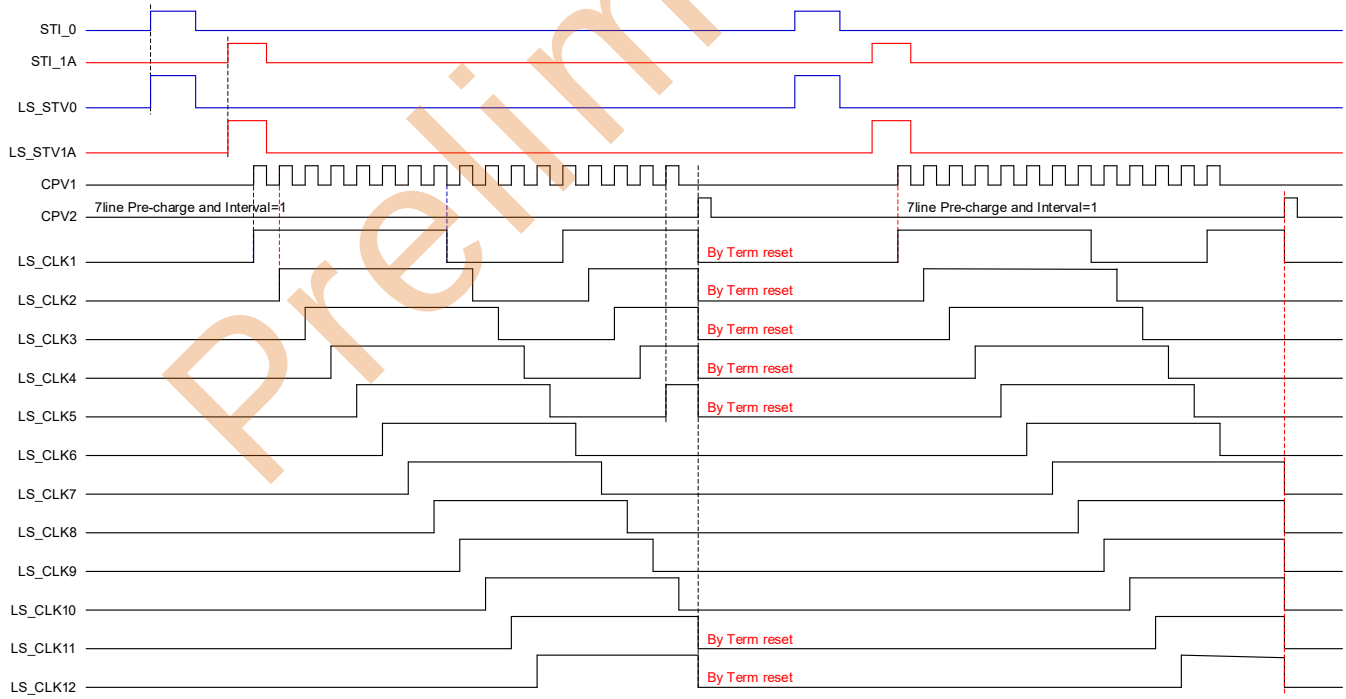
Type: 12-phase, 1line input mode and 5line pre-charge



Type: 12-phase, 1line input mode and 6line pre-charge

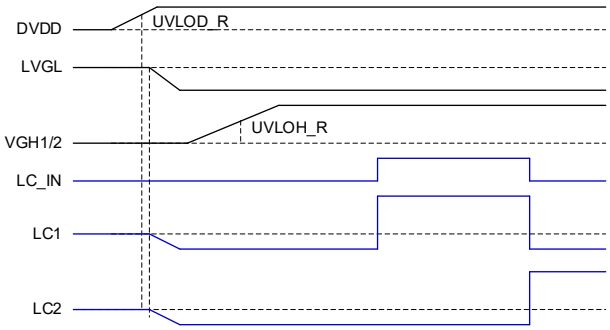


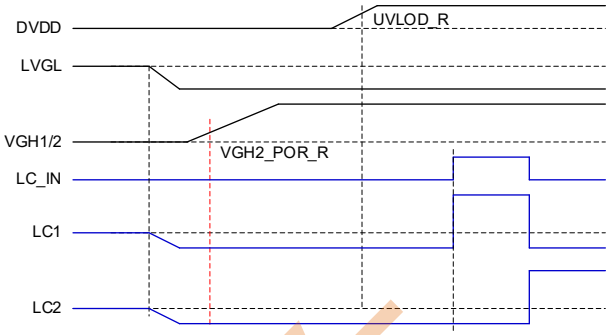
Type: 12-phase, 1line input mode and 7line pre-charge

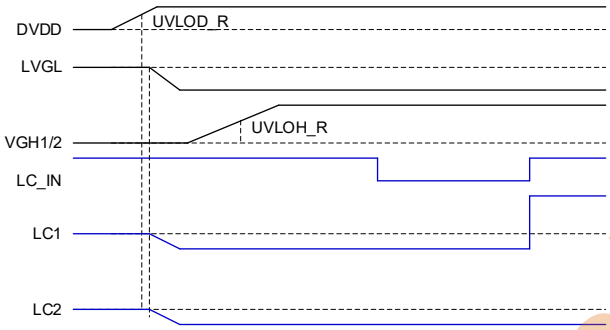


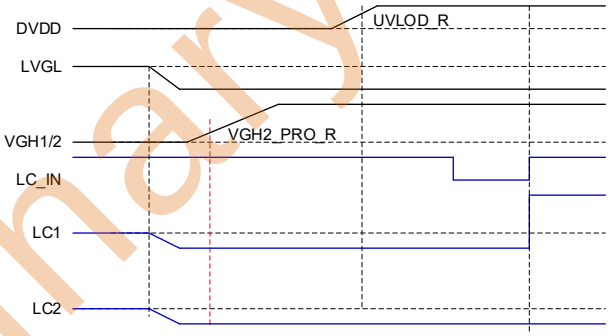
LC1 and LC2 output power on status control

Type1: LC1 and LC2 Both LVGL output

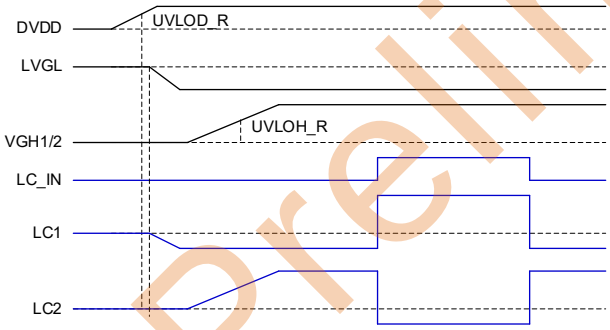


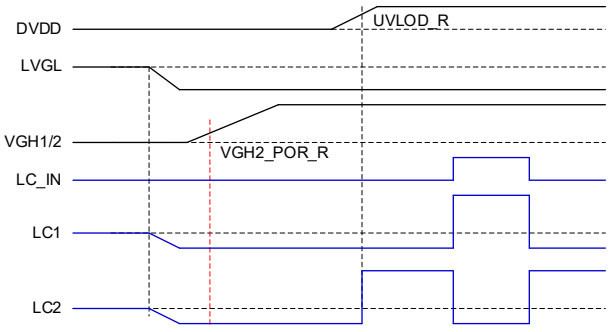


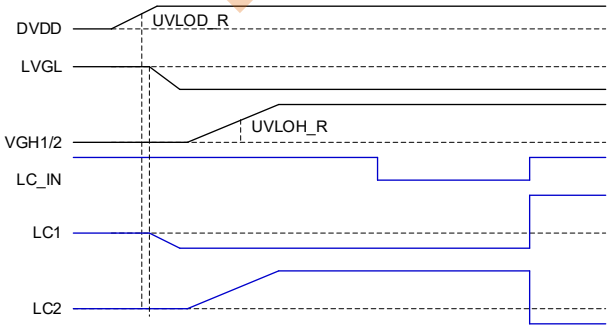


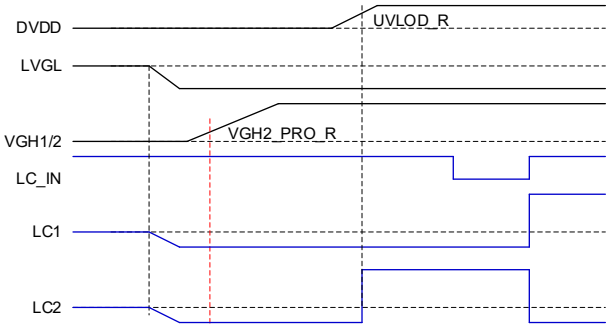


Type2: LC1 Follow LVGL and LC2 Follow VGH2

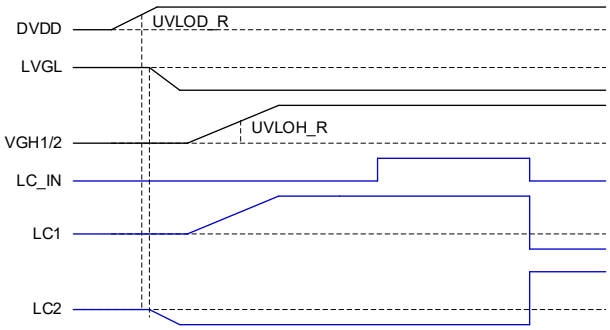


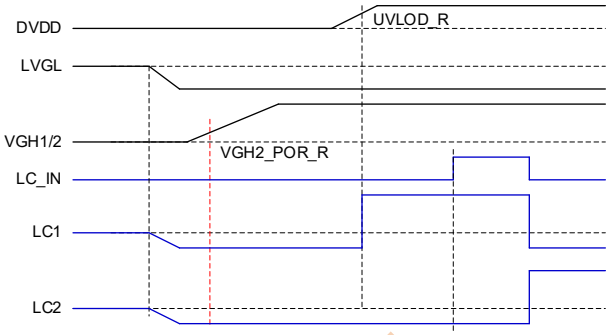


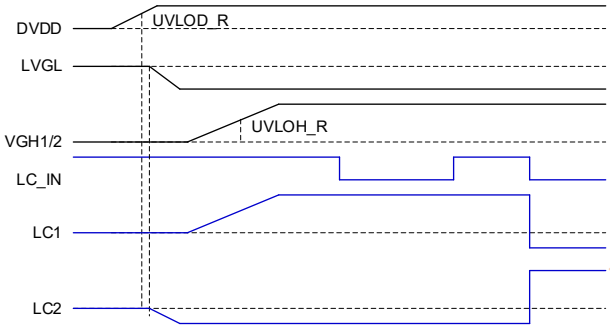


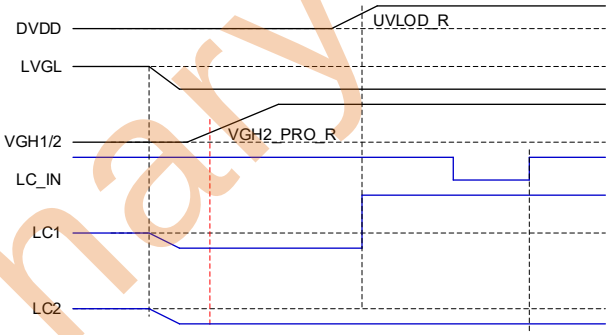


Type3: LC1 Follow VGH2 and LC2 Follow LVGL

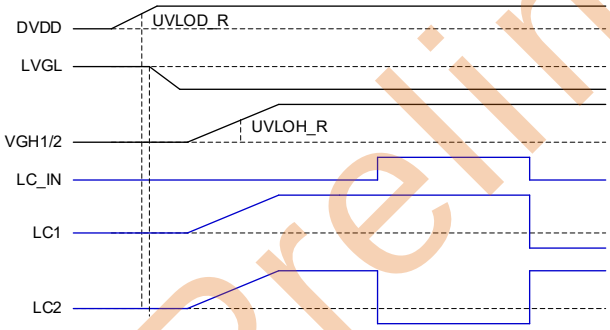


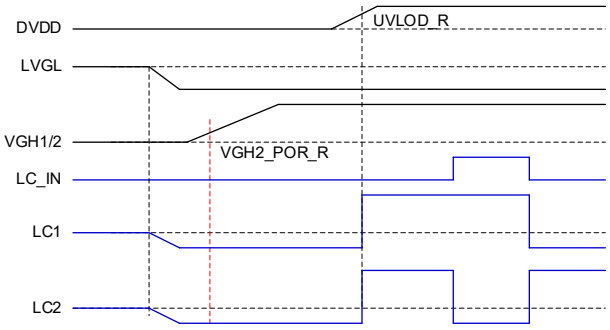


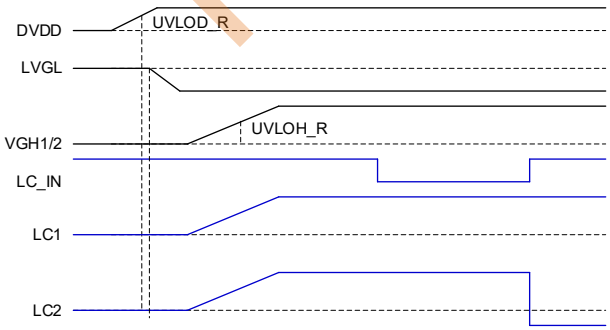


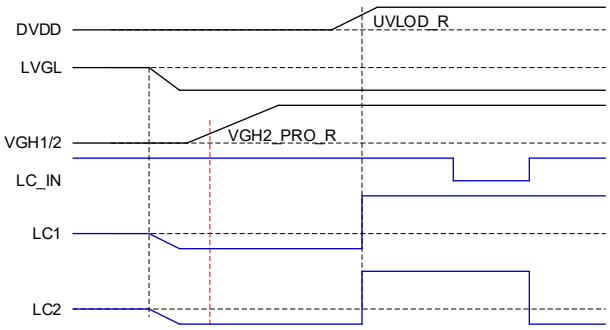


Type4: LC1 and LC2 Both Follow VGH2



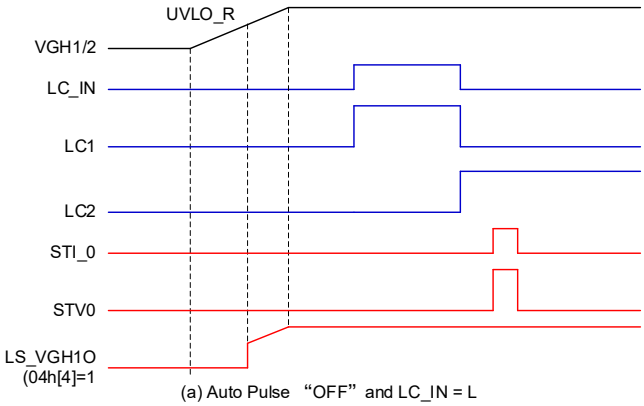




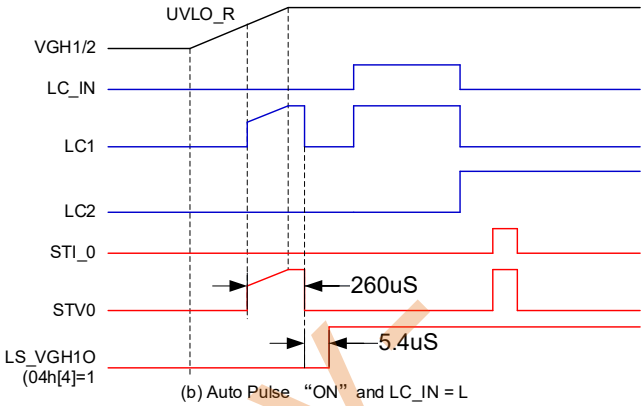


LC1 LC2 and STV0 output status with autopulse control

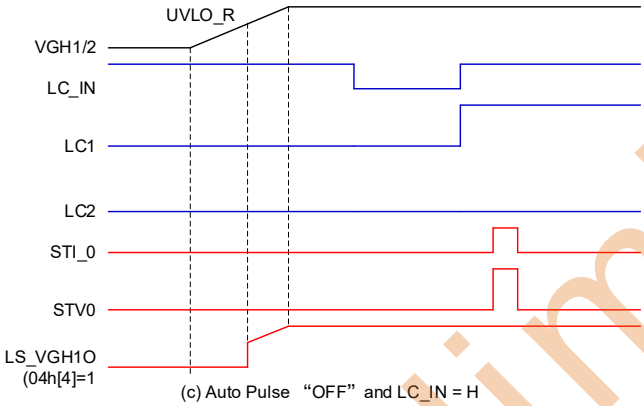
Type1: LC1 and LC2 Both LVGL output



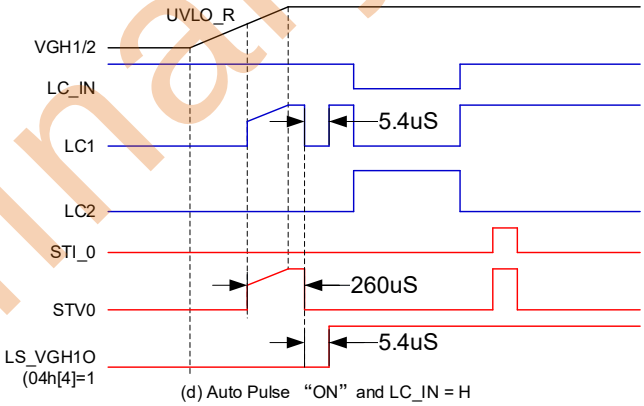
(a) Auto Pulse "OFF" and LC_IN = L



(b) Auto Pulse "ON" and LC_IN = L

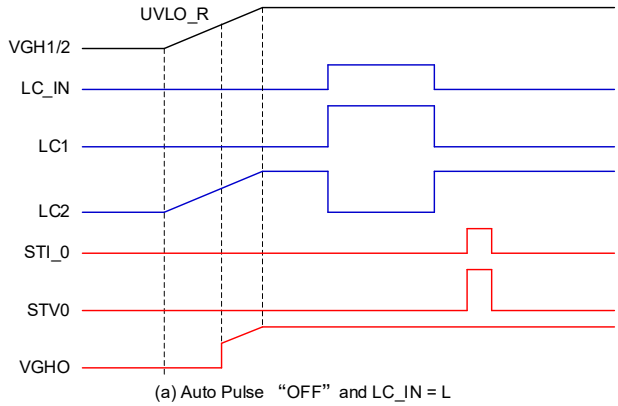


(c) Auto Pulse "OFF" and LC_IN = H

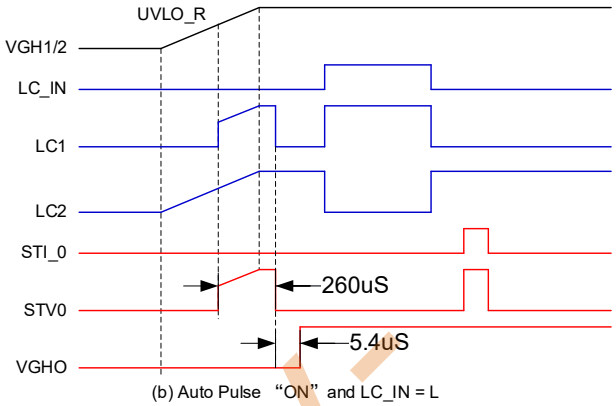


(d) Auto Pulse "ON" and LC_IN = H

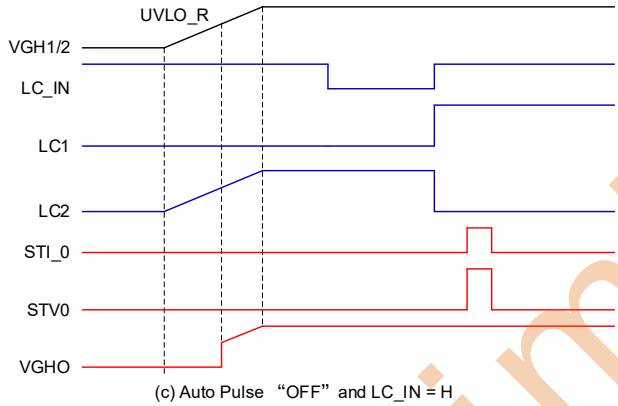
Type2: LC1 Follow LVGL and LC2 Follow VGH2



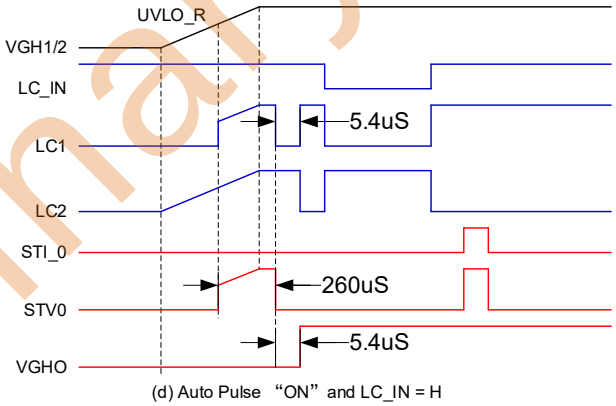
(a) Auto Pulse "OFF" and LC_IN = L



(b) Auto Pulse "ON" and LC_IN = L

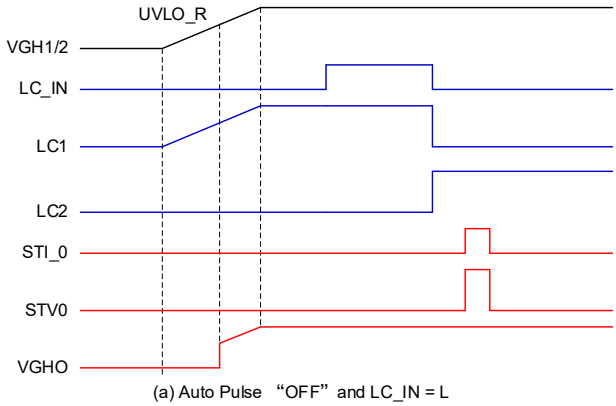


(c) Auto Pulse "OFF" and LC_IN = H

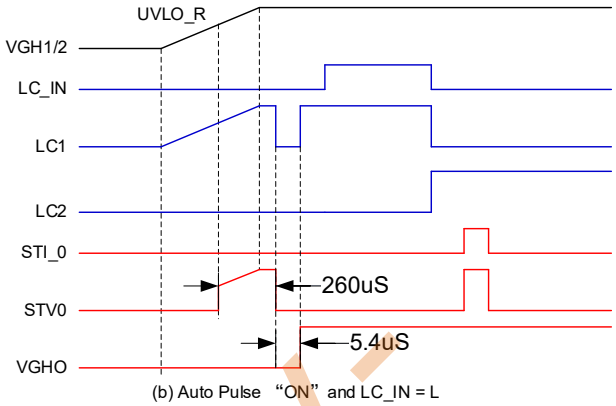


(d) Auto Pulse "ON" and LC_IN = H

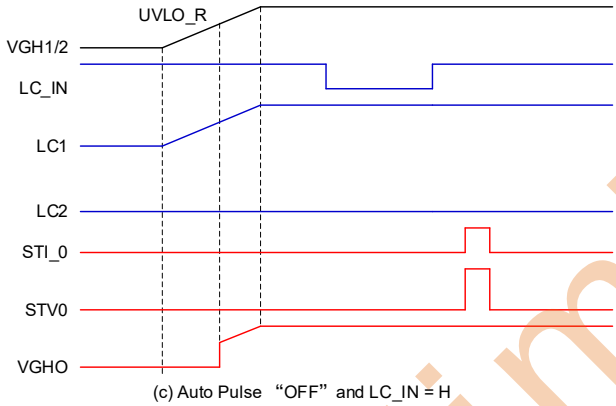
Type3: LC1 Follow VGH2 and LC2 Follow LVGL



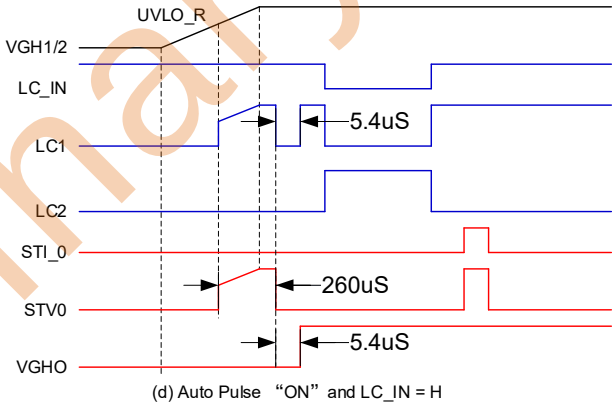
(a) Auto Pulse "OFF" and LC_IN = L



(b) Auto Pulse "ON" and LC_IN = L

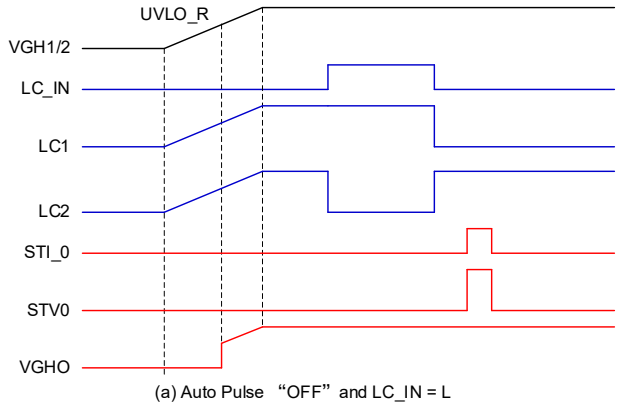


(c) Auto Pulse "OFF" and LC_IN = H

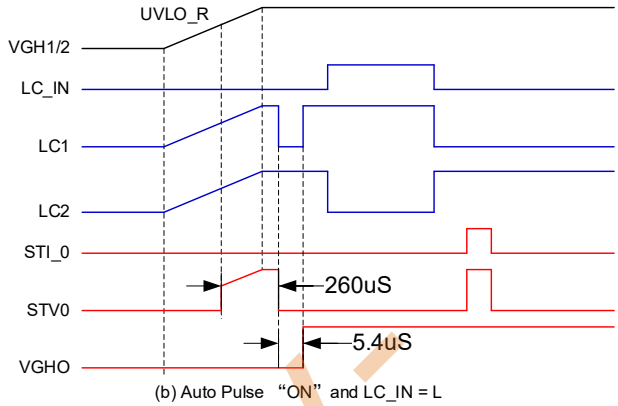


(d) Auto Pulse "ON" and LC_IN = H

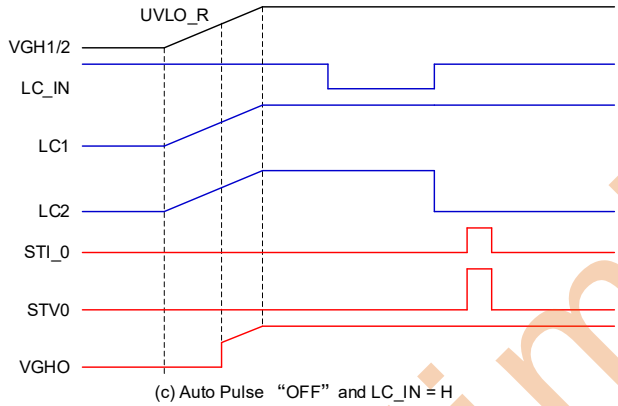
Type4: LC1 and LC2 Both Follow VGH2



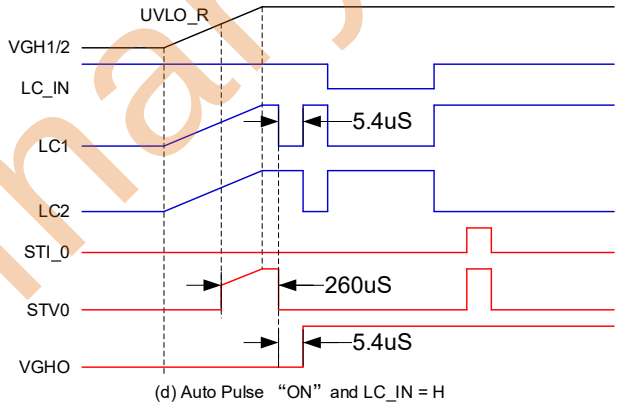
(a) Auto Pulse "OFF" and LC_IN = L



(b) Auto Pulse "ON" and LC_IN = L



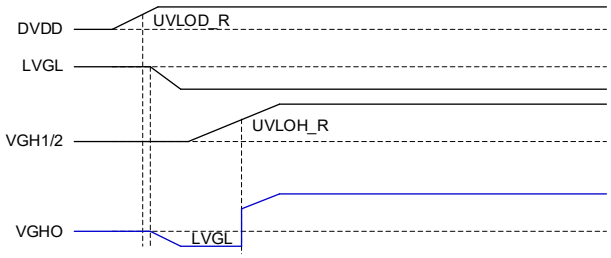
(c) Auto Pulse "OFF" and LC_IN = H



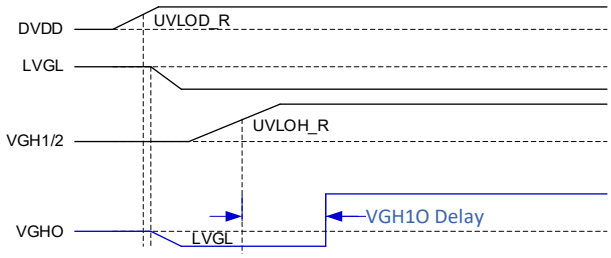
(d) Auto Pulse "ON" and LC_IN = H

VGH1O Power on Delay and Initial

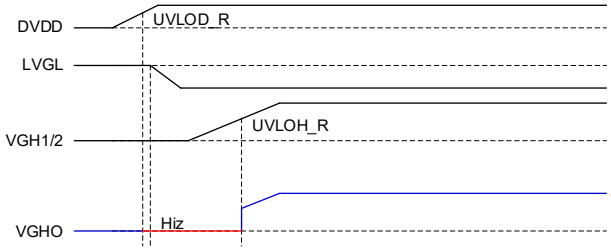
Type: Power on delay 0ms and initial follow LVGL



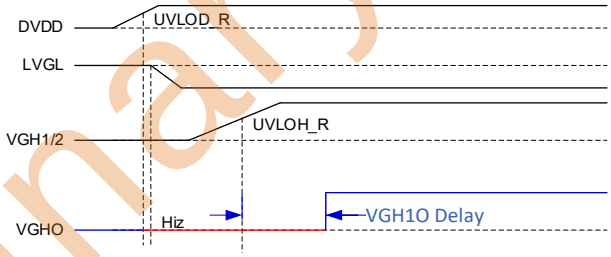
Type: Power on delay 150ms and initial follow LVGL



Type: Power on delay 0ms and initial is Hiz



Type: Power on delay 150ms and initial is Hiz



Protection

The LP6278 implies Over-Temperature Protection(OTP), Over-Current Protection(OCP), Short-Current Protection(SCP). The follow table shows the main behavior of each protection.
When OCP or SCP occurs and the chip is turned off, both DVDD and VGH2 must be powered down at the same time to release OCP/SCP fault
When the XON function is activated, the OCP and SCP functions are disabled

	Output	Recovery
OTP	Hi-Z	Tj decrease 20℃(Typ.)
	Hi-Z	DVDD<$DVDD_{UVLO\_F}$ & VGH2<$VGH2_{UVLOF}$
OCP	Hi-Z	DVDD<$DVDD_{UVLO\_F}$ & VGH2<$VGH2_{UVLOF}$
SCP	Hi-Z	DVDD<$DVDD_{UVLO\_F}$ & VGH2<$VGH2_{UVLOF}$

Over-Temperature Protection(OTP)

An Over-Temperature Protection (OTP) is equipped to prevent LP6278 from overheating due to the excessive power dissipation. The OTP will stop operating while junction temperature exceeds 150°C (Min.). All of output channel start operating while the decrease of junction temperature approximately 20°C (Typ.)

X All-on Output(XAO)

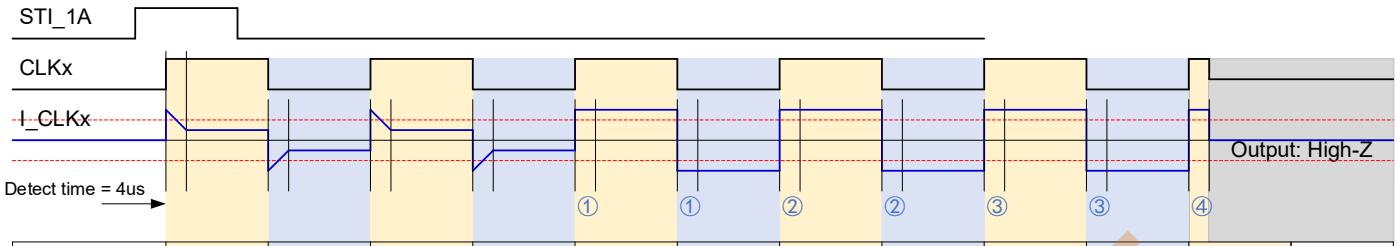
The LP6278 output channel has XAO function, which can detect the voltage sag of DIS_SENSE or DVDD and trigger X all-on. At this time, the state of the output channel is set by the temporary memory, and the state needs VGH2 to be less than VGH2_UVLOF before it is released.

Function	Function effective condition	Function Trigger condition	Output status after triggering	Recovery
XAO	DVDD>$DVDD_{UVLOR}$ (&DIS_SENSE>THR) & VGH1>$VGH1_{UVLOR}$ & First STI_1A rising	By Register set DIS_SENSE falling or DVDD falling	By Register setting	VGH2<$VGH2_{UVLOF}$

Over-Current Protection(OCP)

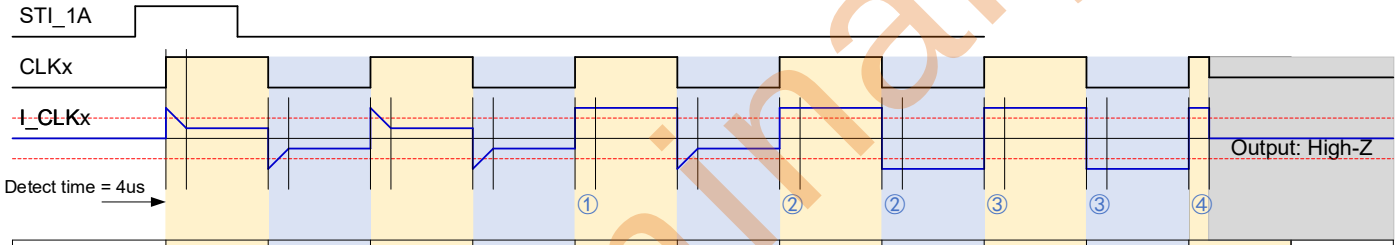
The LP6278 can detect output pins (STV0, STV1A, STV1B, CLK1 to 12, LC1, LC2, LS_VGL, LS_LVGL) short to each other short current. If the pin to pin short current over limit, the IC all outputs (STV0, STV1A, STV1B, CLK1 to 12, LC1, LC2, LS_VGL, LS_LVGL) will pull high impendence state. After DVDD<$DVDD_{UVLOF}$ and VGH2 <$VGH2_{UVLOF}$ falling, IC recovers again.

CLK OCP case1:



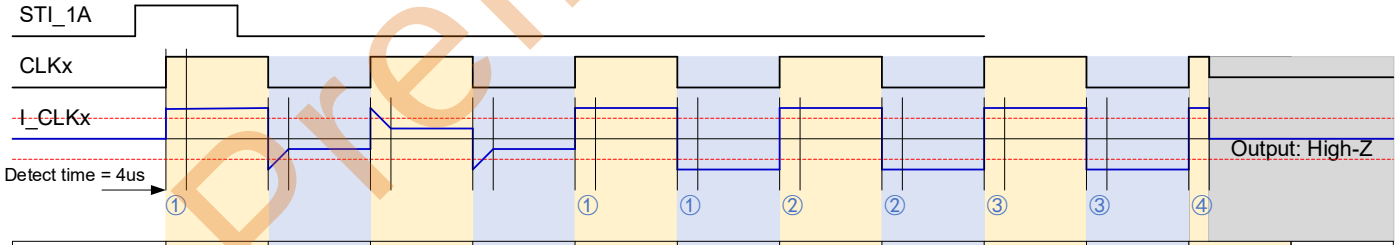
HS on / LS on	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	
OC judgement	PASS	PASS	PASS	PASS	Fail	Fail	Fail	Fail	Fail	Fail	Fail	
OCP_COUNT	Don't count	Don't count	Don't count	Don't count	1st	Keep 1st	2nd	Keep 2nd	3rd	Keep 3rd	4th	

CLK OCP case2:



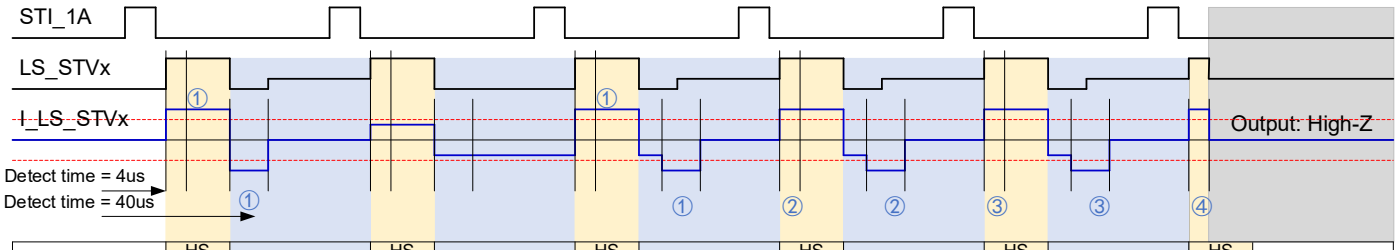
HS on / LS on	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	
OC judgement	PASS	PASS	PASS	PASS	Fail	Fail	Fail	Fail	Fail	Fail	Fail	
OCP_COUNT	Don't count	Don't count	Don't count	Don't count	1st	Keep 1st	2nd	Keep 2nd	3rd	Keep 3rd	4th	

CLK OCP case3:



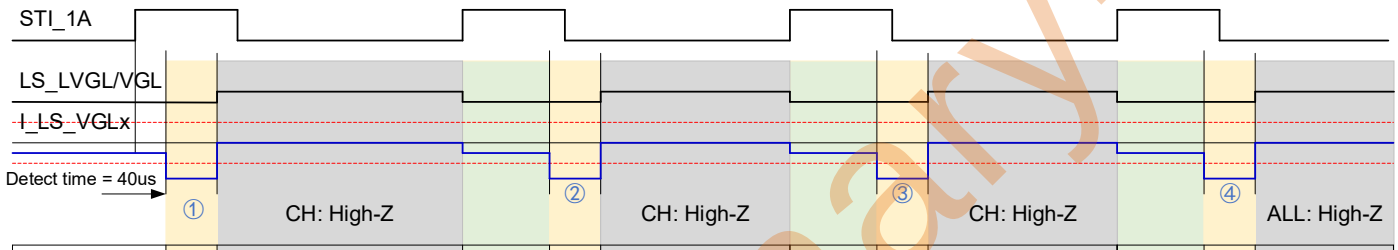
HS on / LS on	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	
OC judgement	Fail	PASS	PASS	PASS	Fail	Fail	Fail	Fail	Fail	Fail	Fail	
OCP_COUNT	1st	Keep 1st	Keep 1st	Reset	1st	Keep 1st	2nd	Keep 2nd	3rd	Keep 3rd	4th	

LS_STVx OCP case4:



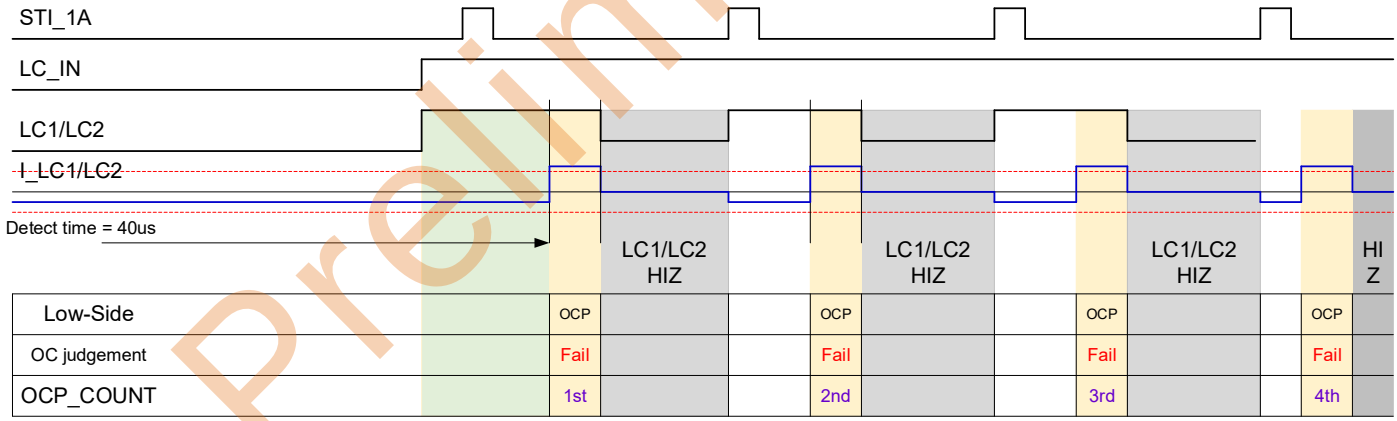
HS on / LS on	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	LS ON	HS ON	
OC judgement	Fail	PASS	PASS	PASS	Fail	Fail	Fail	Fail	Fail	Fail	Fail	
OCP_COUNT	Normal	Keep 1st	Keep 1st	Reset	1st	Keep 1st	2nd	Keep 2nd	3rd	Keep 3rd	4th	

LS_LVGL, LS_VGL OCP case5:



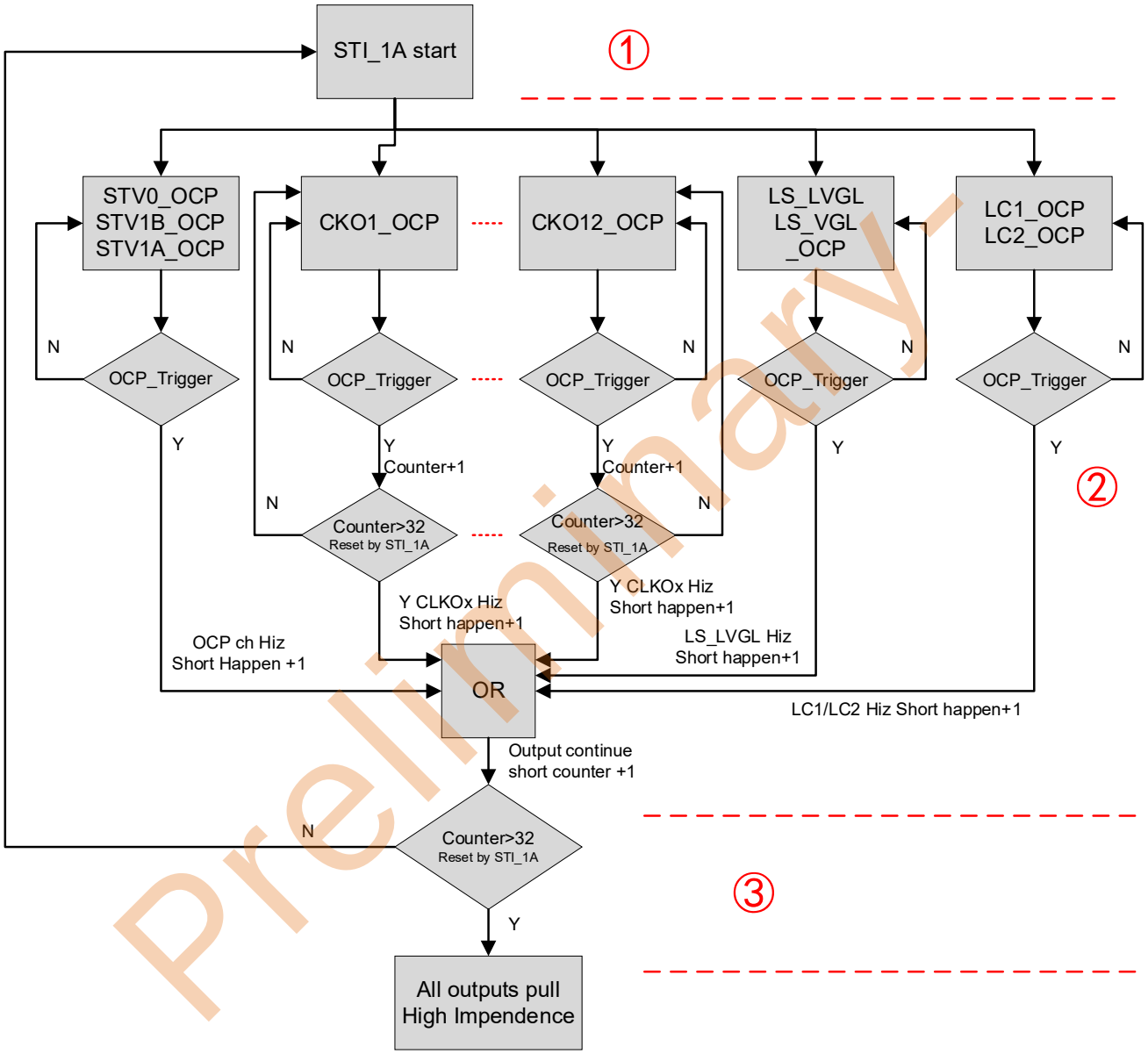
Low-Side	OCP			OCP			OCP			OCP		
OC judgement	Fail			Fail			Fail			Fail		
OCP_COUNT	1st			2nd			3rd			4th		

LC1, LC2 OCP case6:



Low-Side	OCP			OCP			OCP			OCP		
OC judgement	Fail			Fail			Fail			Fail		
OCP_COUNT	1st			2nd			3rd			4th		

The LP6278 can detect output pins (STV0, STV1A, STV1B, CLK1~CLK12, LC1~LC2, LS_LVGL,LS_VGL) short to each other short current. If the pin to pin short current over limit, the IC all outputs will pull high impendence state. After VIN_UVLO, IC recovers again. Please follow reference flow chart. If continue 32 times(By 0x01h[7:6] set) STI_1A have short occur, IC will pull all outputs to high impendence state. After VIN_UVLO and VGH2_UVLO, IC recovers again.
OCP Fucntion is below:



OCP detection behavior

OCP Disable	OCP Disable	OCP Start	OCP Stop	OCP Release
CLK1-CLK12	0x02h[5:3]=000	UVLO_DVDD_R & UVLO_VGH_R& DIS_SENSE_R	UVLO_DVDD_F or UVLO_VGH_F or DIS_SENSE_F	UVLO_DVDD_F & UVLO_VGH_F
STV0 STV1A STV1B	0x01h[5:3]=000	UVLO_DVDD_R & UVLO_VGH_R& DIS_SENSE_R	UVLO_DVDD_F & UVLO_VGH_F & DIS_SENSE_F	UVLO_DVDD_F & UVLO_VGH_F
LC1 LC2	0x01h[5:3]=000	UVLO_DVDD_R & UVLO_VGH_R& DIS_SENSE_R	UVLO_DVDD_F & UVLO_VGH_F & DIS_SENSE_F	UVLO_DVDD_F & UVLO_VGH_F
LS_LVGL LS_VGL	0x01h[5:3]=000	UVLO_DVDD_R & UVLO_VGH_R& DIS_SENSE_R	UVLO_DVDD_F & UVLO_VGH_F & DIS_SENSE_F	UVLO_DVDD_F & UVLO_VGH_F

SCP detection behavior

Channel	SCP Start	SCP Stop
CLK1-CLK12	UVLO_DVDD_R OR UVLO_VGH_R	UVLO_DVDD_F & UVLO_VGH_F
STV0 STV1A STV1B	UVLO_DVDD_R OR UVLO_VGH_R	UVLO_DVDD_F & UVLO_VGH2_F
LC1 LC2	UVLO_DVDD_R OR UVLO_VGH_R	UVLO_DVDD_F & UVLO_VGH_F
LS_LVGL LS_VGL	UVLO_DVDD_R OR UVLO_VGH_R	UVLO_DVDD_F & UVLO_VGH_F

Power on Condition

Power on LC1/LC2 requirement

Case	Analog Power Input			LC1/LC2 Output		Remark
	DVDD	VGH2	DIS_SENSE	LC1	LC2	
1	>UVLOR	>UVLOH	Don't care	LVGL (By REG.)	VGH2 (By REG.)	w/o LC_IN signal
				LC1=LC_IN LC2=LC1_B		w/i LC_IN signal
2	>UVLOR	<UVLOH	Don't care	LVGL (By REG.)	VGH2 (By REG.)	Register Table
3	<UVLOR	Don't care	Don't care	LVGL	LVGL	---

Power on logic table STV0, STV1A,STV1B

Case	Power			Input		Output	
	DVDD	VGH2	DIS_SENSE	STI_0	STI_1A/1B	STV0	STV1A/1B
1	>UVLOR	>UVLOH	>THR	Don't care	Don't care	Normal	Normal
2	>UVLOR	>UVLOH	<THR	Don't care	Don't care	LVGL	LVGL
3	>UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
4	<UVLOR	>UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
5	<UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL

Power on logic table STI_0 can not control CLKx

Case	Power			Input		Output	
	DVDD	VGH2	DIS_SENSE	STI_0	CPV1/CPV2	CLK1-12	STV0
1	>UVLOR	>UVLOH	>THR	Don't care	Don't care	Normal	Normal
2	>UVLOR	>UVLOH	<THR	Don't care	Don't care	LVGL	LVGL
3	>UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
4	<UVLOR	>UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
5	<UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL

Power on logic table STI_0 can control CLKx

Case	Power			Input		Output	
	DVDD	VGH2	DIS_SENSE	STI_0	CPV1/CPV2	CLK1-12	STV0
1	>UVLOR	>UVLOH	>THR	w/i	Don't care	Normal	Normal
2	>UVLOR	>UVLOH	>THR	w/o	Don't care	LVGL	Normal
3	>UVLOR	>UVLOH	<THR	Don't care	Don't care	LVGL	LVGL
4	>UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
5	<UVLOR	>UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
6	<UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL

Power on logic table STI_1A can not control CLKx

Case	Power			Input		Output	
	DVDD	VGH2	DIS_SENSE	STI_1A	CPV1/CPV2	CLK1-12	STV1A
1	>UVLOR	>UVLOH	>THR	Don't care	Don't care	Normal	Normal
2	>UVLOR	>UVLOH	<THR	Don't care	Don't care	LVGL	LVGL
3	>UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
4	<UVLOR	>UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
5	<UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL

Power on logic table STI_1A can control CLKx

Case	Power			Input		Output	
	DVDD	VGH2	DIS_SENSE	STI_1A	CPV1/CPV2	CLK1-12	STV1A
1	>UVLOR	>UVLOH	>THR	w/i	Don't care	Normal	Normal
2	>UVLOR	>UVLOH	>THR	w/o	Don't care	LVGL	Normal
3	>UVLOR	>UVLOH	<THR	Don't care	Don't care	LVGL	LVGL
4	>UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
5	<UVLOR	>UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL
6	<UVLOR	<UVLOH	Don't care	Don't care	Don't care	LVGL	LVGL

Power off logic table

Case	Analog Power Input			Output		Remark
	DVDD	VGH2	DIS_SENSE	LC1	LC2	
1	>UVLOD	>UVLOF	>THR	LVGL (By REG.)	VGH2 (By REG.)	w/o LC_IN signal Normal operate
				LC1=LC_IN LC2=LC1_B		w/i LC_IN signal Normal operate
2	>UVLOD	>UVLOF	<THR	By XON REG.	By XON REG.	By XON Follow set (STI_1A first rising happen)
				LC1=LC_IN LC2=LC1_B		(STI_1A first rising don't happen)
3	>UVLOD	<UVLOF	Don't care	LVGL	LVGL	
4	<UVLOD	>UVLOF	Don't care	By XON REG.	By XON REG.	By XON Follow set (STI_1A first rising happen)
				LVGL	LVGL	(STI_1A first rising don't happen)
5	<UVLOD	<UVLOF	Don't care	LVGL	LVGL	

Power off logic table

Case	Analog Power Input			Output		Remark
	DVDD	VGH2	DIS_SENSE	LS_LVGL	LS_VGL	
1	>UVLOD	>UVLOF	>THR	LVGL (By REG.)	VGL	
2	>UVLOD	>UVLOF	<THR	By XON REG.	By XON REG.	By XON Follow set (STI_1A first rising happen)
				LVGL/VGH1 0x04h[3] Reg.	VGL	(STI_1A first rising don't happen)
3	>UVLOD	<UVLOF	Don't care	LVGL	VGL	
4	<UVLOD	>UVLOF	Don't care	By XON REG.	By XON REG.	By XON Follow set (STI_1A first rising happen)
				LVGL	VGL	(STI_1A first rising don't happen)
5	<UVLOD	<UVLOF	Don't care	LVGL	VGL	

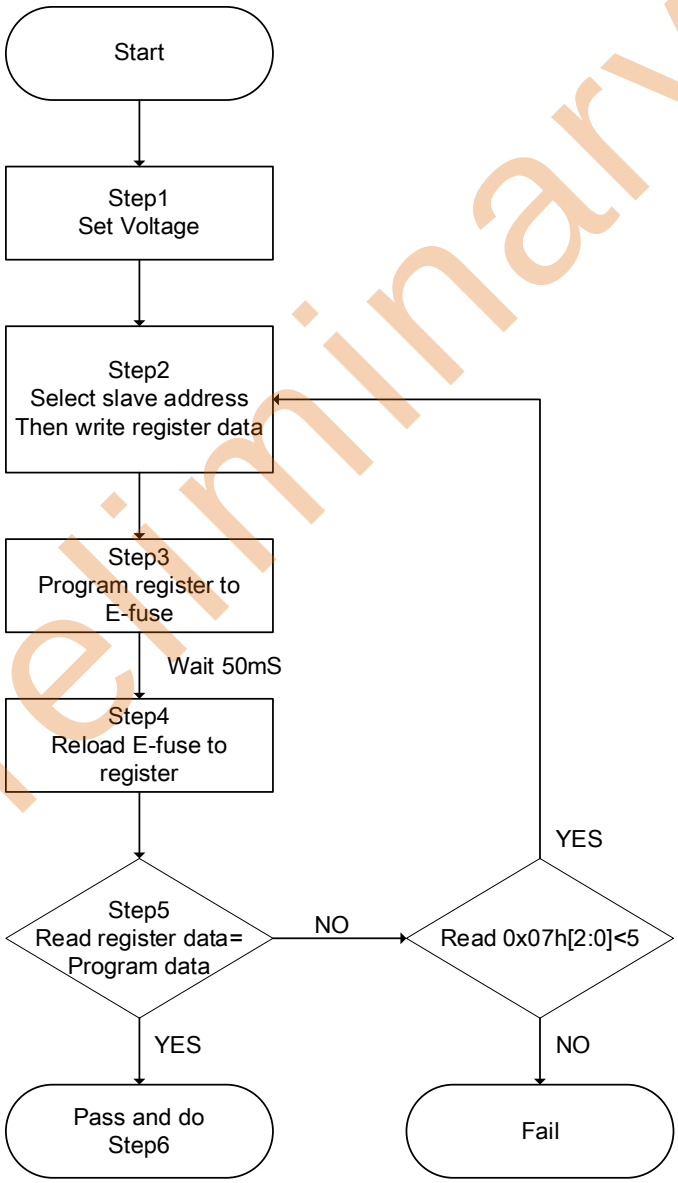
Case	Analog Power Input			Output		Remark
	DVDD	VGH2	DIS_SENSE	STV0	STV1A/1B	
1	>UVLOD	>UVLOF	>THR	Normal Operate	Normal Operate	
2	>UVLOD	>UVLOF	<THR	By XON REG.	By XON REG.	By XON Follow set (STI_1A first rising happen)
				LVGL	LVGL	(STI_1A first rising don't happen)
3	>UVLOD	<UVLOF	Don't care	LVGL	LVGL	
4	<UVLOD	>UVLOF	Don't care	By XON REG.	By XON REG.	By XON Follow set (STI_1A first rising happen)
				LVGL	LVGL	(STI_1A first rising don't happen)
5	<UVLOD	<UVLOF	Don't care	LVGL	LVGL	

Power off logic table

Case	Analog Power Input				Output	Remark
	DVDD	VGH2	DIS_SENSE	STI_0,STI_1A	CLK1-12	
1	>UVLOD	>UVLOF	>THR	w/o	LVGL	
	>UVLOD	>UVLOF	>THR	w/i	Normal Operate	
	>UVLOD	>UVLOF	<THR	w/o	LVGL	
	>UVLOD	>UVLOF	<THR	w/i	By XON REG.	By XON Follow set (STI_1A first rising happen)
3	>UVLOD	<UVLOF	Don't care	Don't care	LVGL	
4	<UVLOD	>UVLOF	Don't care	w/o	LVGL	
				w/i	By XON REG.	By XON Follow set (STI_1A first rising happen)
5	<UVLOD	<UVLOF	Don't care	LVGL	VGL	

E-fuse Program Flow:

- Step1: DVDD = 3.3V → LVGL = VGL = -6V → VGH = 20V.
- Step2: Select Slave Address: 0x50h/0x52h, then write register (0x00h~0x07h) data.
- Step3: Program register to E-fuse: 0xFFh = 0xA5.
- Step4: Reload E-fuse: 0xFFh = 0xA4.
- Step5: Check register(0x00h~0x07h) data with writing code :
  If register (0x00h~0x07h) data is the same with writing code --> successfully written
  If register (0x00h~0x07h) data isn't the same with writing code --> Repeat Step2~5
  (Note: IC can't program over 5 times)
- Step6: VGH = 0V → LVGL = VGL = 0V → DVDD = 0V.



Device Address Setting

PMIC Device Slave Address (By A0 PIN and 0x05h[2] set)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Write Address	Read Address
0	1	0	1	0	05h[2]=0 0	0 A0=L	R/W	0x50	0x51
0	1	0	1	0	05h[2]=0 0	1 A0=H/F	R/W	0x52	0x53
0	1	0	1	0	05h[2]=1 1	0 A0=L	R/W	0x54	0x55
0	1	0	1	0	05h[2]=1 1	1 A0=H/F	R/W	0x56	0x57

I2C Command Device address (Write_50h/Read_51h)

1. Single Byte Write Transaction

S	Slave Address (0x52h)	A	Reg. Address	A	Data for index register	A	P

2. Multi-Bye (Sequential) Write Transaction – From Registers X to Y

S	Slave Address (0x52h)	A	Reg. Address X	A	DATA(X)	A	DATA(X+1)	A	---

---	A	DATA(Y-1)	A	DATA(Y)	A	P

3. Write All DAC into MTP

S	Slave Address (0x52h)	A	Control Byte Address (0xFFh)	A	Control Byte Code (A5h)	A	P

4. Single Byte Read Transaction

S	Slave Address (0x52h)	A	Reg. Address X	SR	Slave Adress (0x53h)	A	Data read for X	NA	P

5. Multi-Byte (Sequential) Read Transaction - from register at index address X to index address Y

S	Slave Address (0x52h)	A	Index Address X	SR	Slave Adress (0x53h)	A	DATA(X)	A	DATA(X+1)	A	---

---	A	DATA(Y-1)	A	DATA(Y)	NA	P

6. Reset All data DAC from MTP to DAC

S	Slave Address (0x52h)	A	Control Byte Address (0xFFh)	A	Control Byte Code (A4h)	A	P

Register Map:

I2C Device Address: 0x50h/0x52h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x00h (**E1h**)	[7:6] CLKx output phase no.	CLKx_PH	6-phase, 8-phase 10-phase, 12-phase		11: 12phase
	[5:4] CLKx output slew rate	CLKx_SR	1000V/us, 700V/us 400V/us, 100V/us		10: 400V/us
	[3] CLCK11 and CLK12 select By CLK11_I/CLK12_I control		0: Don't by control 1: Can by control		0: Don't control
	[2] DIS_SENSE PIN Function Select		0: DIS_SENSE function 1: DLG control function		0: DIS_SENSE
	[1:0] Detect SENSE voltage	DIS_SENSE	00: Detect dvdd pin voltage 01-11:(2.3V, 0.8V, 2.5V)		01: 2.3V
0x01h (**28h**)	[7:6] Channel OCP detect count	CH_OCP_DC	4 times to 32 times		00: 4 times
	[5:3] Channel OCP level	CH_OCP	30mA to 160mA		101: 90mA
	[2] Channel OCP blanking time	CH_OCP_BT	2us or 4us		0: 2uS
	[1:0] CH output low side OCP detect time		CH: STV0/1A/1B,LS_VGL, LS_LVGL Low side MOS detect time, And LC1/LC2 low side and high side MOS detect time. 40us~160us		00: 40us
0x02h (**ADh**)	[7:6] CLKx OCP detect count	CLK_OCP_DC	4 times to 32 times		10: 16 times
	[5:3] CLKx OCP level	CLK_OCP	30mA to 160mA		101: 90mA
	[2:0] CLKx high/low side& STV0,STV1A,STV1B high side OCP detect time	CLK_OCP_DT	1us to 8us		101: 6us

I2C Device Address: 0x50h/0x52h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x03h (**F1h**)	[7] STV0 Power off XON Follow		0: LS_LVGL 1: VGH2		1: VGH2
	[6] STV1A/1B Power off XON Follow		0: LS_LVGL 1: VGH1		1: VGH1
	[5] CLKx, LC1/2 Power off XON Follow		0: LS_LVGL 1: CLKx=VGH1, LCx=VGH2		1: VGH1-CLK VGH2-LC1/2
	[4] LS_LVGL Power off XON Follow		0: LS_LVGL 1: VGH1		1: VGH1
	[3] Output Channel Power off XON state setting		0: Follow 0x03h[7:4] set 1: All Output Channel Hiz		0: By 0x03h[7:4]
	[2] Output Channel XON time-sharing control		0: Synchronous 1: Time-sharing		0: SYNC.
	[1] LS output enable control		0: Enable 1: Disable (All Channel Hiz)		0: Enable
	[0] VGH2 power on UVLO_R		0: 7V 1: 15V		1: 15V
0x04h (**C0**)	[7:6] LC1/2 power on status				11: Both VGH2
	[5] LC1/LC2 initial remove		0: LC_IN First rising 1: VGH_UVLO_R		0: LC_IN rising
	[4] Auto pulse function control				0: Disable
	[3] LS_LVGL Output status Option		0: Follow LS_LVGL 1: Follow VGH1		0: LS_LVGL
	[2] VGHO Initial state		0: Follow LVGL 1: Hiz		0: Follow LVGL
	[1:0] VGHO output delay time		0: Follow VGH_UVLO_R 0ms to 150ms		0: 0ms

I2C Device Address: 0x50h/0x52h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x05h (**28h**)	[7] Power on Blanking time		0: 0ms 1: 150ms		0: 0mS
	[6] STI_0 reset CLK setting	STI0_RST	0: Don't reset anything 1: STI0 rising reset CLK		0: Don't RST
	[5]STI_1A reset CLK setting	STI1A_RST	0: Don't reset anything 1: STI_1A rising reset		1: RST
	[4] CLK output enable control		0: Don't By STI_0 control 1: By STI_0 rising control CLK is low before 1st STI_0		0: Don't By STI_0
	[3] CLK output enable control		0: Don't By STI_1A control 1: By STI_1A rising control CLK low before 1st STI_1A		1: By STI_1A
	[2] Device address setting		Set Slave address bit2 0: Bit2=0 1: Bit2=1		0: Bit2=0
	[1] OTP_RE		OTP Recover 0: Hysteresis recovery 1: Latch, Power Re-start		0: HYS_RE
	[0] Dummy		Dummy		
0x06h (**00h**)	[7:6] Reserved				
	[5:4] CPV input control select		00: Rising and Falling 01: Only Rising 10: Only Falling 11: 1line tcon input (CPV1)		00: R and F
	[3:2] CLK output rotate mode		00: Normal 01: Mode1 10: Mode2 11: Inverted		00: Normal
	[1:0] DLG MODE SET		00: Adjacent MODE 01: Half way apart MODE 10: One apart MODE 11: Two apart MODE		00: Adjacent
0x07h (**00h**)	[7] CLK Interval select		Only when 0x06h[5:4]=11 0: No Interval between CLK 1: Interval between CLK		0: No Interval
	[6:4] CLK pre-charge select Just only @07h, bit[5:4] CPV input select = 11		Only when 0x06h[5:4]=11 000: No Pre-charge 001-111: 1line to 7line Pre-charge		000: No Pre-charge
	[3] Reserved				
	[2:0] E-fuse Write Times	Only Read	000~101: E-fuse write 1-5 times		000: User hasn't been written.

I2C Device Address: 0x50h/0x52h

Register Address	Parameter	Symbol	Range	Resolution	Default value
0x08h* (00h)	[7:0] DLG enable control Configurable online and effective at next STI_1A rising	DLG_EN	00h: Exit DLG output mode 01h: Enter DLG output mode		00h
0x10h* Read Only	[6] OTP fault status		OTP		0: OK
	[5] LS_VGL fault status		OCP and SCP		0: OK
	[4] LS_LVGL fault status		OCP and SCP		0: OK
	[3] LC1/LC2 fault status		OCP and SCP		0: OK
	[2] STV1A/1B fault status		OCP and SCP		0: OK
	[1] STV0 fault status		OCP and SCP		0: OK
	[0] CLK1-CLK12 fault status		OCP and SCP		0: OK
0xFFh*	[7:0] Control Byte	CTRL_BT	A5: Write All DAC into MTP A4: Reset from MTP to DAC		00h

Registers and DAC settings

CLKx and XAO voltage setting (0x00h) --- Default Code E1h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKx_PHASE_SEL		CLKx_SR		CLK11/12 _CTRL	DIS_SEN _SEL	DIS_SENSE_V	
1	1	0	0	0	0	0	1

Bit	Name	Description	
[7:6]	CLKx_PH_SEL	Code	CLKx output phase select
		00	6-Phase
		01	8-Phase
		10	10-Phase
		11	12-Phase
[5:4]	CLKx_SR	Code	CLKx output slew rate setting
		00	1000V/us
		01	700V/us
		10	400V/us
		11	100V/us
[3]	CLK11/12_CTRL	Code	CLK11/CLK12 by input signal control enable
		0	Don't by CLK11_I and CLK12_I control
		1	Can by CLK11_I and CLK12_I control (only 6/8/10 phase out)
[2]	DIS_SENSE_ PIN_SEL	Code	DIS_SENSE pin function select
		0	DIS_SENSE voltage detect function
		1	DLG enter and exit function (only 0x00h[1:0]=00)
[1:0]	DIS_SENSE_V	Code	DIS_SENSE detect voltage trigger XON function
		00	Detect DVDD pin voltage trigger XON function
		01	2.3V
		10	0.8V
		11	2.5V

Channel Setting (0x01h) --- Default Code 28h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CH_OCP_DC		CH_OCP_LEVEL			CH_OCP_BT	CH_LOCP_LEVEL	
0	0	1	0	1	0	0	0

Bit	Name	Description	
[7:6]	CH_OCP_DC	Code	Channel OCP detect count (CLKx is not included)
		00	4 times
		01	8 times
		10	16 times
		11	32 times
[5:3]	CH_OCP_LEVEL	Code	Channel OCP detect level (CLKx is not included)
		000	Disable OCP detect
		001	30mA
		010	40mA
		011	50mA
		100	70mA
		101	90mA
		110	120mA
		111	160mA
[2]	CH_OCP_BT	Code	All output channel OCP blanking time
		0	2uS
		1	4uS
[1:0]	CH_LOCP_DT	Code	Output Channel Low-side OCP detect time (CLK is not included) STV0,STV1A,STV1B only Low-side,LC1/LC2 low-side and high-side LS_LVGL and LS_VGL low-side
		00	40uS
		01	80uS
		10	120uS
		11	160uS

CLK Setting (0x02h) --- Default Code ADh

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKx_OCP_DC		CLKx_OCP_LEVEL			CLKx_OCP_DT		
1	0	1	0	1	1	0	1

Bit	Name	Description	
[7:6]	CLK_OCP_DC	Code	CLKx channel OCP detect count
		00	4 times
		01	8 times
		10	16 times
		11	32 times
[5:3]	CLKx_OCP_TH	Code	CLKx OCP detect level
		000	Disable OCP detect
		001	30mA
		010	40mA
		011	50mA
		100	70mA
		101	90mA
		110	120mA
		111	160mA
[2:0]	CLKx_OCP_DT	Code	CLKx OCP detect time
		000	1us
		001	2us
		010	3us
		011	4us
		100	5us
		101	6us
		110	7us
		111	8us

Power off Setting (0x03h) --- Default Code F1h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
STV0 _POFF	STV1A/1B _POFF	CLK,LC1/2 _POFF	LS_LVGL _POFF	CH_POFF	XON_TS	LS_EN	VGH2 _UVLO
1	1	1	1	0	0	0	1

Bit	Name	Description	
[7]	STV0_POFF	Code	STV0 trigger XON power off follow setting
		0	LVGL
		1	VGH2
[6]	STV1A/STV1B _POFF	Code	STV1A/STV1B trigger XON power off follow setting
		0	LVGL
		1	VGH1
[5]	CLKx/LC1/LC2 _POFF	Code	CLKx and LC1/LC2 trigger XON power off follow setting
		0	LVGL
		1	CLKx follow VGH1, LC1/LC2 follow VGH2
[4]	LS_LVGL_POFF	Code	LS_LVGL trigger XON power off follow setting
		0	LVGL
		1	VGH1
[3]	CH_POFF_SEL	Code	Output Channel trigger XON power off follow setting
		0	Follow 0x03h[7:4]
		1	All output channel Hi-Z
[2]	XON_TS	Code	Output channel trigger XON power off time-sharing control
		0	Synchronous
		1	Time-Sharing
[1]	LS_EN	Code	LS all output channel enable control
		0	Enable
		1	Disable (All output channel Hi-Z)
[0]	VGH2_UVLO_R	Code	VGH2 power on start voltage
		0	7.5V
		1	15V

Function Setting (0x04h) --- Default Code C0h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LC_PON_MODE		LC_INITIAL	AUP_EN	LS_LVGL _OPTION	VGHO _INITIAL	VGHO_DLY	
1	1	0	0	0	0	0	0

Bit	Name	Description	
[7:6]	LC_PON_MODE	Code	LC1/LC2 power on Initial state setting
		00	Both LVGL
		01	LC1 follow LVGL, LC2 follow VGH2
		10	LC1 follow VGH2, LC2 follow LVGL
		11	Both VGH2
[5]	LC_INITIAL	Code	LC1/LC2 power on initial remove condition
		0	LC_IN rising
		1	VGH_UVLO rising
[4]	AUP_EN	Code	Auto pulse control
		0	Disable auto pulse function
		1	Enable auto pulse function
[3]	LS_LVGL_OPTION	Code	LS_LVGL Output Status Control
		0	LS_LVGL Output LVGL
		1	LS_LVGL Output VGH1
[2]	VGHO_INITIAL	Code	VGHO output initial status
		0	Follow LVGL
		1	Hi-Z
[1:0]	VGHO_DLY	Code	VGHO output delay time
		00	0ms Follow VGH_UVLO_R
		01	50ms
		10	100ms
		11	150ms

Power off Setting (0x05h) --- Default Code 28h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PON_BT	STI0_RST	STI1A_RST	CLK_EN1	CLK_EN2	Slave_SEL	OTP_RE	Dummy
0	0	1	0	1	0	0	0

Bit	Name	Description	
[7]	PON_BT	Code	Power on blanking time
		0	0ms
		1	150ms
[6]	STI0_RST	Code	STI_0 reset CLK output control
		0	Don't reset CLK
		1	STI_0 rising pull low CLK and reset CLK
[5]	STI1A_RST	Code	STI_1A reset CLK output control
		0	Don't reset CLK
		1	STI_1A rising pull low CLK and reset CLK
[4]	CLK_EN1	Code	STI_0 first rising control CLK output setting
		0	Don't by STI_0 control
		1	By STI_0 rising control, CLK pull low before 1st STI_0
[3]	CLK_EN2	Code	STI_1A first rising control CLK output setting
		0	Don't by STI_1A control
		1	By STI_1A rising control, CLK pull low before 1st STI_1A
[2]	SLAVE_ADDR _SEL	Code	Set Slave address bit2
		0	Address bit2=0
		1	Address bit2=1
[1]	OTP_RE	Code	Over Temperature Protection recover condition setting
		0	Hysteresis Recovery - Temperature hysteresis 20℃ and Next STI_1A rising
		1	Latch Protection, Power Re-start - DVDD and VGH restart up
[0]	Dummy	Code	Dummy
		0	
		1	

CLK Control Setting (0x06h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Dummy	Dummy	CPV_CTRL		CLK_ROTATE_MODE		CLK_DLG_MODE	
0	0	0	0	0	0	0	0

Bit	Name	Description	
[7]	Dummy	Code	Dummy
		0	
		1	
[6]	Dummy	Code	Dummy
		0	
		1	
[5:4]	CPV_CTRL	Code	CPV1/CPV2 control CLK output setting
		00	Rising and Falling (CPV1 and CPV2)
		01	Only Rising (CPV1 and CPV2)
		10	Only Falling (CPV1 and CPV2)
		11	1line Tcon Input (Only CPV1, CPV2 is Terminal Function)
[3:2]	CLK_ROTATE_MODE	Code	CLK output sequence cycle setting
		00	Forward sequential output - Normal
		01	Forward sequential output from the second half
		10	Output in reverse order from the first half
		11	Reverse sequence output
[1:0]	DLG_MODE_SEL	Code	DLG output mode selection
		00	Adjacent MODE
		01	Half way apart MODE
		10	One apart MODE
		11	Two apart MODE

CLK Control Setting (0x07h) --- Default Code 00h

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLK_interval	CLK Pre-charge select			Reserved	E-fuse Write Times		
0	0	0	0	0	0	0	0

Bit	Name	Description	
[7]	CLK Interval select* Only 0x06h[5:4]=11	Code	CLK interval select
		0	No interval between CLK
		1	Interval between CLK
[6:4]	CLK pre-charge select * Only 0x06h[5:4]=11 1line Tcon Input (Only CPV1, CPV2 is Terminal Function)	Code	CLK pre-charge select
		000	No Pre-Charge
		001	1line Pre-Charge
		010	2line Pre-Charge
		011	3line Pre-Charge
		100	4line Pre-Charge
		101	5line Pre-Charge
		110	6line Pre-Charge
		111	7line Pre-Charge
[2:0] *- Only Read	E-fuse have been written 5 times. If Register Data=101. E-fuse can't be written andkeep 5th data.	Code	Record E-fuse Written times
		000	E-fuse don't write
		001	E-fuse write 1 time
		010	E-fuse write 2 time
		011	E-fuse write 3 time
		100	E-fuse write 4 time
		101	E-fuse write 5 time

DLG Control Setting (0x08h) --- Default Code 00h

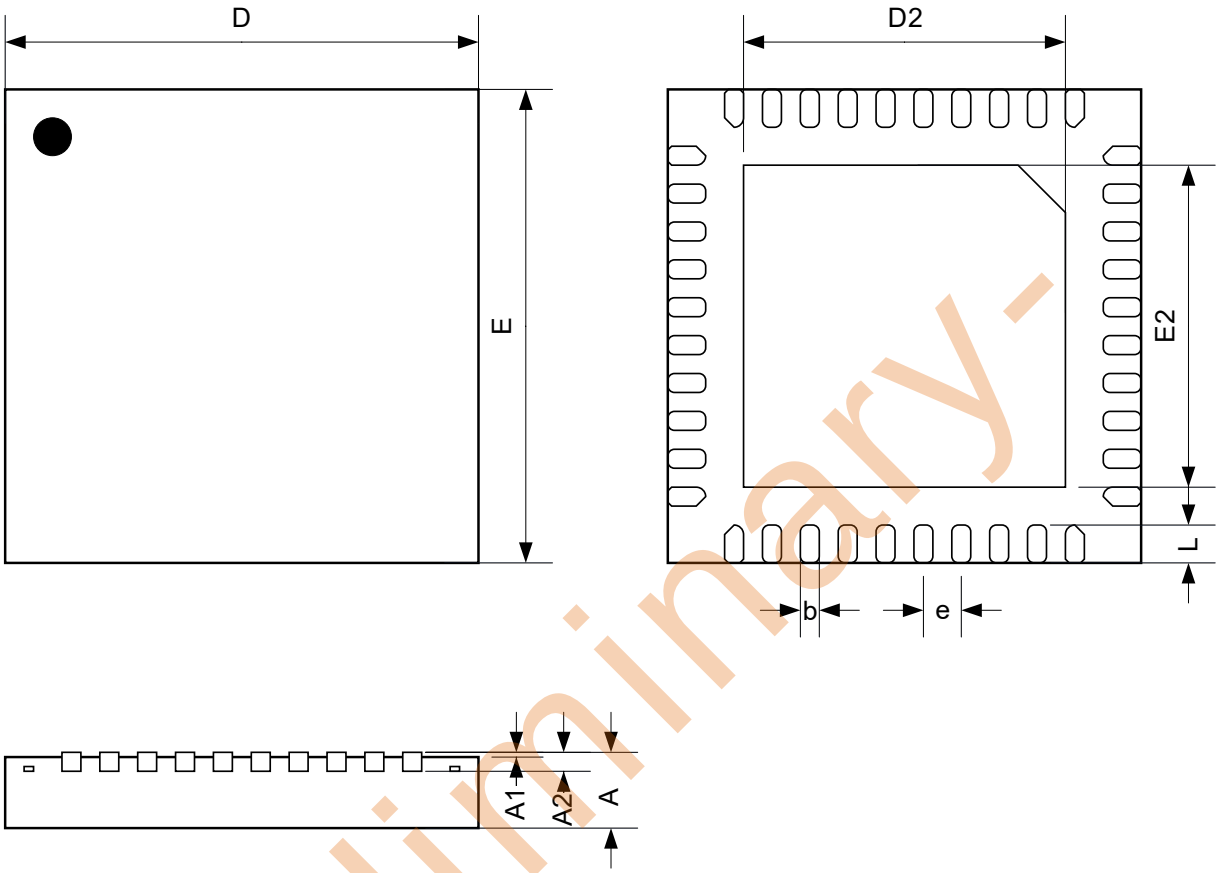
Bit	Name	Description	
[7:0]	DLG_EN	Code	DLG enter and exit control
		00h	DLG disable or Exit DLG mode
		01h	Enter DLG mode

Control Byte (0xFFh) --- Default Code 00h

Bit	Name	Description	
[7:0]	Control Byte	Code	Control Byte
		A5	Write All DAC into MTP
		A4	Reset from MTP to DAC

Packaging Information

QFN5X5-40



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	4.95	5.00	5.05	0.1949	0.1969	0.1988
E	4.95	5.00	5.05	0.1949	0.1969	0.1988
D1	3.30	3.40	3.50	0.1299	0.1339	0.1378
E1	3.30	3.40	3.50	0.1299	0.1339	0.1378
b	0.15	0.20	0.25	0.0059	0.0079	0.0098
e	0.40 BSC			0.0157 BSC		
L	0.30	0.40	0.45	0.0118	0.0157	0.0177