LP62702

Dual Output 200mA Power Supply for LCD Bias

Features

- Input voltage range: 2.7V to 5.5V
- Programmable output voltages
  - OUTP output voltage: 4V to 6.5V with 0.1V per step
  - OUTN output voltage: -6.5V to -4V with 0.1V per step
- OUTP output current up to 200mA
- OUTN output current up to 200mA
- 85% efficiency at VIN=4.4V, OUTP/OUTN = +/-5.5V, IOUTP=ION=150mA
- I2C Interface
  - Flexible Output Voltage Programming
  - Programmable Active Output Discharge
- Protections
  - Input under-voltage lockout (UVLO)
  - Boost cycle-by-cycle current-limit protection
  - Output over current protection
  - Output short circuit protection
  - Thermal shutdown protection
- Packaging
  - DFN3x3-12
  - RoHS compliant and halogen free
  - 100% lead (Pb) free

Applications

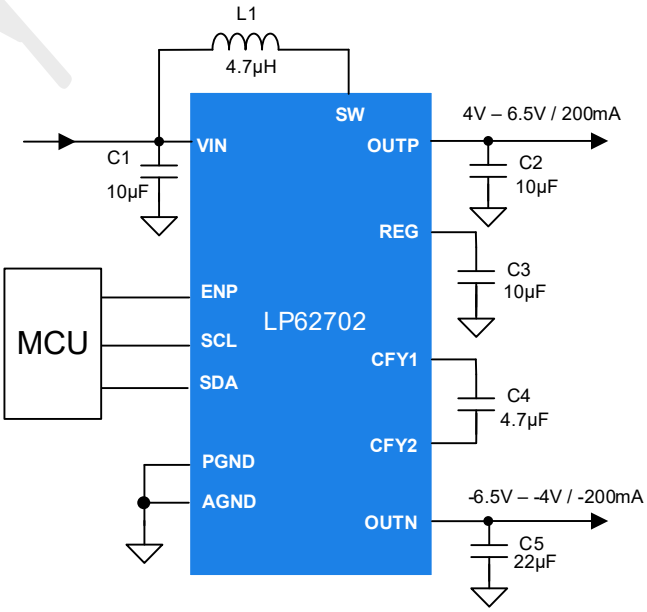
- TFT LCD Display
  - Smartphone, Tablet
  - Camera, GPS
  - Home Automation, Point-of-Sales

General Description

The LP62702 is designed to supply positive/negative driven applications. The device uses a single inductor scheme to provide up to 200mA currents for both positive and negative output. The integrated synchronous Boost converter provides a regulated voltage for a LDO and a charge pump. The LDO provides a regulated and programmable positive bias OUTP and the charge pump provides a regulated and programmable negative bias OUTN. The device offers low noise, small solution size, high efficiency and robust protections. The other features include under-voltage lockout (UVLO), internal soft-start, boost cycle-by-cycle current limit, output over current and short circuit protection as well as thermal shutdown. The LP62702 is available in a space saving DFN3x3 package.

Order Information

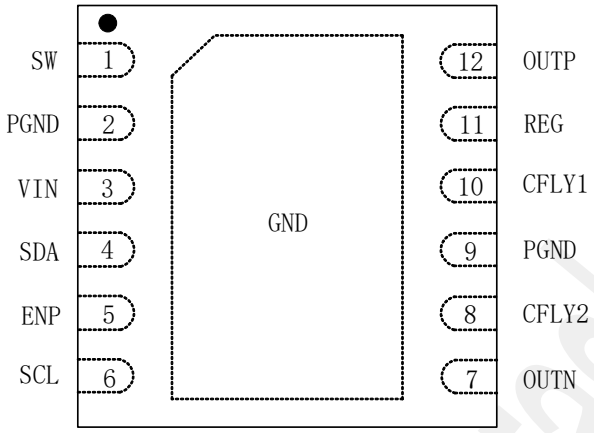
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Moisture Sensitivity Level	Shipping
LP62702HVF	LPS LP62702 YWX	DFN3x3	MSL3	5K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



DFN3x3-12 (Top View)

Pin Description

Pin #	Name	Description
1	SW	Switching node output. Connect a terminal of an external inductor to this switching node. Short and wide trace is required for SW connection.
2, 9	PGND	Power ground. Connect to thermal PAD on PCB top layer.
3	VIN	Supply voltage input. Connect a 10μF ceramic capacitor from this pin to PGND.
4	SDA	I2C interface data signal.
5	ENP	Enable input for OUTP and OUTN output.
6	SCL	I2C interface clock signal.
7	OUTN	Negative voltage output. Decouple this pin to PGND with a 10μF or higher ceramic capacitor as close to this pin as possible.
8	CFLY2	Negative input for the external flying capacitor. Connect a terminal of a 2.2μF or 4.7μF ceramic capacitor close to this pin.
10	CFLY1	Positive input for the external flying capacitor. Connect a terminal of a a 2.2μF or 4.7μF ceramic capacitor close to this pin.
11	REG	Boost converter regulated output. Decouple this pin to PGND with a 10μF or higher ceramic capacitor as close to this pin as possible.
12	OUTP	Positive voltage output. Decouple this pin to PGND with a 10μF or higher ceramic capacitor as close to this pin as possible.
13	Thermal PAD& GND	Analog ground. Thermal pad must be connected to PGND on PCB, better on top layer.

Absolute Maximum Ratings (Note)

VIN, SW, REG, OUTP, CFLY1, SDA, SCL Voltage to GND ---------- 0.3V to 7V
ENP Voltage to GND ---------- -0.3V to VIN+0.3V
OUTN, CFLY2 Voltage to GND ---------- -7V to 0.3V
Maximum Junction Temperature (Tj) ---------- 150℃
Storage Temperature Range ---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 85℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	2.7		5.5	V
I_{OUTP}	Positive Output Current	0		200(1)	mA
I_{OUTN}	Negative Output Current	0		200(1)	mA
V_{OUTP}	Positive Output Voltage	4.0	5.5	6.5	V
V_{OUTN}	Negative Output Voltage	-6.5	-5.5	-4.0	V
T_J	Operating Junction Temperature Range (TJ)	-40		125	℃
T_A	Ambient Temperature Range	-40		85	℃
L	Boost Inductance(2)	1.54	2.2	5.64	μH
C_{IN}	Input Capacitance (2) (3)	4	10	30	μF
C_{REG}	Boost Output Capacitance(2) (3)	4	10	30	μF
C_{FLY}	Flying capacitance(2) (3)	1.4	4.7	5.64	μF
C_{OUTP}	Output Capacitance(2) (3)	4	10	32	μF
C_{OUTN}	Output Capacitance(2) (3)	4	10	32	μF

Notes:
(1) Higher transient output current is allowed with higher output voltage drop.
(2) The values recommended in the table are effective inductance and capacitance.
(3) X7R or X5R 10V (or 16V) voltage rating capacitors are recommended

Electrical Characteristics

(The specifications are at V_{IN}=3.7V, OUTP=5.5V, OUTN=-5.5V and T_J = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Range		2.7		5.5	V
I_{SHDN}	Input Supply Current	VENP =0			1	μA
I_Q	Input Supply Current	Boost switching, V_{IN}=3.7V,OUTP=-OUTN=5.5V		0.8		mA
V_{IN_UVLO}	Under Voltage Lockout of V_{IN}	V_{IN} Rising		2.48		V
$V_{IN\_UVLO\_HYS}$	V_{UVLO} Hysteresis	V_{IN} Falling		230		mV
BOOST CONVERTER						
F_{SW}	Switching Frequency		1.0	1.2	1.4	MHz
I_{LIM}	Switch Valley Current Limit	V_{REG}> V_{IN}		1.32		A
D_{MAX}	Maximum Duty Cycle			90		%
R_{DSON_HS}	High-side MOSFET On-resistance			0.32		Ω
R_{DSON_LS}	Low-side MOSFET On-resistance			0.12		Ω
V_{SCP_VREG}	Hiccup Threshold	Percentage of V_{REG} regulation, V_{REG} falling		66		%
V_{SS_BOOST}	Soft-start Threshold from Linear to Switching	(V_{IN} – V_{REG}), V_{REG} rising		350		mV
$V_{SS\_\_HYS}$	Soft-start Threshold from Linear to Switching Hysteresis	(V_{IN} – V_{REG}), V_{REG} falling		250		mV
I_{SS_BOOST}	Soft Start Current in Linear Mode	V_{REG} < V_{IN} – 0.35V		220		mA
$T_{SS\_MAX\_BOOST}$	Maximum Soft-start Time			2		ms
T_{SCP_HICCUP}	SCP Hiccup Deglitch Time	Waiting time before entry into hiccup mode		16		us
T_{HICCUP}	Waiting Time Prior to Hiccup Retry			20		ms

Electrical Characteristics (Continued)

(The specifications are at VIN=3.7V, OUTP=5.5V, OUTN=-5.5V and TJ = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POSITIVE OUTPUT VOLTAGE LDO						
OUTP	Positive Output Voltage Range	21 steps, each step, 100mV	4.0		6.5	V
$OUTP_{\_ACC}$	Positive Output Voltage Accuracy	VOUT=4.0V-6.2V, IOUTP=10mA	-1.5		+1.5	%
$IOUTP_{\_C}$	Positive Output Current Capability		200			mA
VREG_LINE	Line Regulation	VIN=2.7V~4.5V,IOUTP=80mA, VOUT=5.5V		1		%
V_{HRV_LDO}	Headroom Voltage			400		mV
V_{HRV_LDO}	Headroom Voltage			200		mV
V_{REG_LOAD}	Load Regulation	OUTP=5.5V, IOUTP=0mA to150mA		0.5		%
R_{DIS_P}	OUTP Discharge Resistance			70		Ω
R_{PD_ENP}	ENP Pull-Down Resistor			200		kΩ
I_{LIM_LDO}	Output Current Limit	OUTP > 40% of regulated voltage		325		mA
I_{SCP_LDO}	Output Short Circuit (SCP) Current	OUTP < 40% of regulated voltage		150		mA
V_{SCP_LDO}	Short Circuit Protection Threshold	Percentage of OUTP hiccup threshold		40		%
T_{SS_LDO}	LDO Startup Ramp-up Time	C_{OP}=10uF		1.2		ms
$T_{SS\_MAX\_LDO}$	LDO Maximum Soft-start Time			3.0		ms

Electrical Characteristics (Continued)

(The specifications are at V_{IN}=3.7V, OUTP=5.5V, OUTN=-5.5V and T_J = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
NEGATIVE OUTPUT VOLTAGE CHARGE PUMP						
F_{CP}	Negative Charge Pump Switching Frequency		1.0	1.2	1.4	MHz
OUTN	Negative Output Voltage Range	21 steps, 100mV per step	-6.2		-4.0	V
$OUTN_{\_ACC}$	Output Voltage Accuracy	OUTN=-6.2V to -4V, IOUTP=10mA	-1.5		+1.5	%
I_{ON_C}	Negative Output Current Capability	Current flowing into OUTN	220			mA
V_{HRV_CP}	Headroom Voltage	OUTN=-5.5V, V_{HRV_CP} = V_{REG} - 5.5V REG03[7]=0		400		mV
V_{HRV_CP}	Headroom Voltage	OUTN=-5.5V, V_{HRV_CP} = V_{REG} - 5.5V REG03[7]=1		200		mV
$OUTN_{\_LINE}$	Line Regulation	V_{IN}=2.7V~4.5V, I_{ON}= 150mA		1		%
$OUTN_{\_LOAD}$	Load Regulation	I_{ON}=-200mA to -10mA		2		%
R_{DIS_N}	OUTN Discharge Resistance			30		Ω
$I_{LIM\_M4\_SCP}$	Internal Current Limit			210		mA
$T_{SS\_CP\_MAX}$	Maximum Soft-start Time			8	15	ms
$I_{LIM\_M1\_SS}$	Internal Current Limit	Soft-start		160		mA
V_{SCP_CP}	Short Circuit Detection	Percentage of OUTN, entry into hiccup mode		90		%

Electrical Characteristics (Continued)

(The specifications are at V_{IN}=3.7V, OUTP=5.5V, OUTN=-5.5V and T_J = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN PROTECTION						
T_{SHUT}	Thermal Shutdown	Temperature Rising		140		℃
T_{SHUT_HYST}	Thermal Shutdown Hysteresis	Temperature Falling		20		℃
LOGIC I/O						
$V_{ENP(H)}$	Input High Threshold Level		1.2			V
$V_{ENP(L)}$	Input Low Threshold Level				0.4	V

Electrical Characteristics (Continued)

(The specifications are at V_{IN}=3.7V, OUTP=5.5V, OUTN=-5.5V and T_J = 25°C for typical values unless otherwise noted.)

Symbol	Parameter	Condition	Min	Typ	Max	Units
I2C COMPATIBLE TIMING SPECIFICATIONS						
f_{SCL}	SCL clock frequency	Standard Mode			100	kHz
		Fast Mode			400	kHz
t_{LOW}	Low period of the SCL clock	Standard Mode	4.7			us
		Fast Mode	1.3			us
t_{HIGH}	High period of the SCL clock	Standard Mode	4.0			us
		Fast Mode	0.6			us
t_{BUF}	Bus free time between a STOP and START condition	Standard Mode	4.7			us
		Fast Mode	1.3			us
$t_{HD, SDA}$	Hold time for a repeated START condition	Standard Mode	4.0			us
		Fast Mode	0.6			us
$t_{SU, DAT}$	Data setup time	Standard Mode	0.25			us
		Fast Mode	0.1			us
$t_{HD, DAT}$	Data hold time	Standard Mode	0.05		3.45	us
		Fast Mode	0.05		0.9	us
t_{RDA}	Rise time of SDA signal	Standard Mode	20+0.1C_B		1000	ns
		Fast Mode	20+0.1C_B		300	ns
t_{FDA}	Fall time of SDA signal	Standard Mode	20+0.1C_B		300	ns
		Fast Mode	20+0.1C_B		300	ns
$t_{SU,STO}$	Setup time for STOP condition	Standard Mode	4.0		-	
		Fast Mode	0.6		-	
C_B	Capacitive load for SCL and SDA		-	-	0.2	nF

Typical Characteristics

(L1=2.2μH, C_1, C2, C3= 10 μF, C4= 4.7μF, C5=22μF and T_J = 25°C unless otherwise noted; the schematic is as shown in Figure 8)

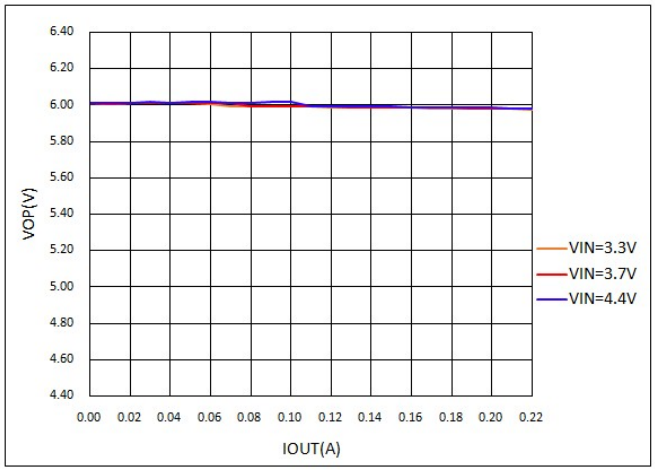


Figure 1. Positive Output Voltage OUTP vs Load
（VOUTP=-VOUTN=6V, IOUTP=-ION=0-220mA）

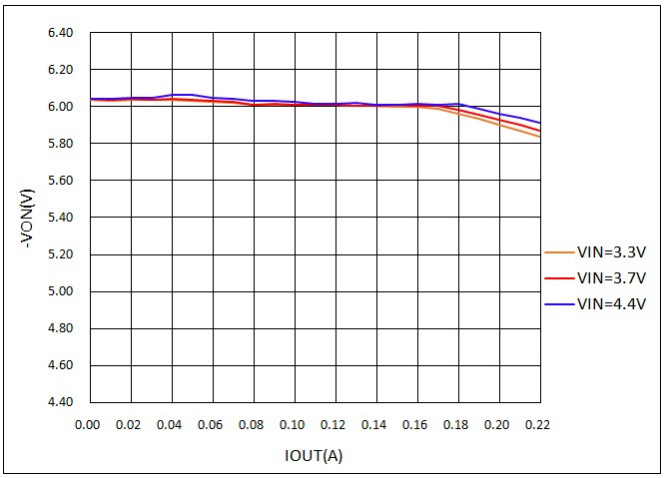


Figure 2. Negative Output Voltage OUTN vs Load
（VOUTP=-VOUTN=6V, IOUTP=-IOUTN=0-220mA）

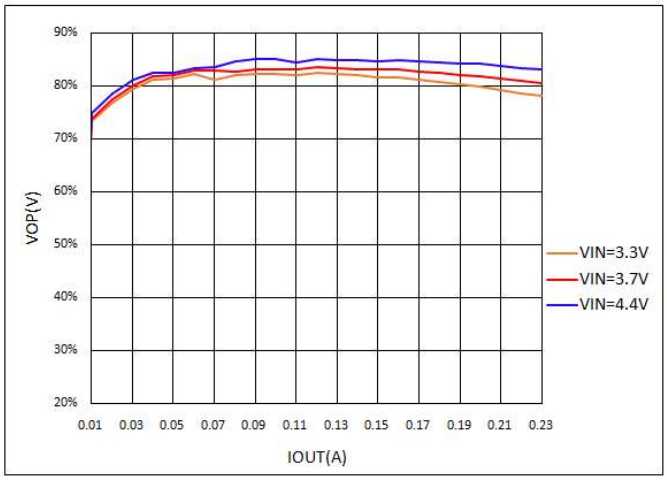
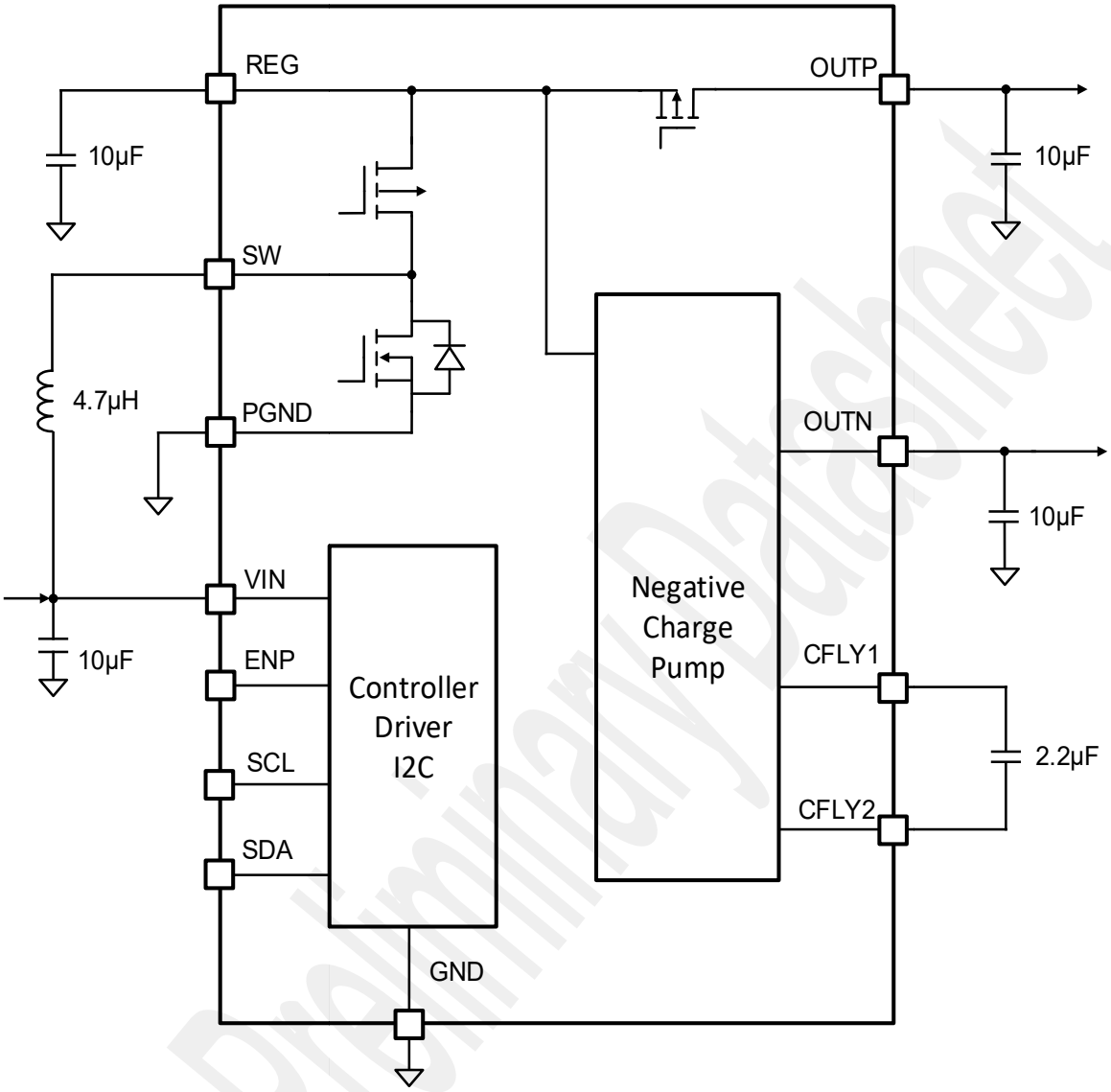


Figure 3. Efficiency vs. Load
（VOUTP=-VOUTN=6V, IOUTP=-IOUTN=0-230mA）

Functional Block Diagram



Detailed Description

Overview

The LP62702 supports input voltage range from 2.7 V to 5.5 V and operates with a single inductor scheme to provide a high-efficiency small-size solution. The synchronous boost converter generates a positive voltage that is regulated down by an integrated LDO that provides a positive supply rail (OUTP). The negative supply rail (OUTN) is generated by an integrated negative charge pump (NCP) driven from the boost converter output. The output current capability for both positive rail and negative rail is 200mA. The device allows a 100% asymmetry of the output currents.

Under Voltage Lockout (UVLO)

The LP62702 integrates an under-voltage lockout block (UVLO) that enables the device once the voltage on the VIN pin exceeds the UVLO threshold. The device will not start and no output voltages will be generated as long as the enable pins ENP is not pulled HIGH. The device, as well as all converters (boost converter, LDO, NCP), will be disabled as soon as the VIN voltage falls below the UVLO threshold.

Power Sequencing

The LDO and the negative charge pump (NCP) can be enabled / disabled by external enable signals. The ENP pin is the enable control input for both OUTP and OUTN. There is about 12ms delay from OUTP startup to OUTN startup.

Soft Startup

Boost converter starts in linear mode with output current limited to I_{SS_BOOST}. Within maximum boost startup time $T_{SS\_MAX\_BOOST}$, if the boost output voltage V_{REG} ramps above the threshold V_{SS_BOOST}, the boost converter soft-start is complete and the system enables LDO or NCP sequentially. If $T_{SS\_MAX\_BOOST}$ expires and V_{REG} has not reached the threshold V_{SS_BOOST}, the boost converter turns off and restarts in T_{HICCUP}.

LDO starts with output current limited to I_{SCP_LDO}. Within maximum LDO startup time $T_{SS\_MAX\_LDO}$, if the LDO output voltage V_{OUTP} ramps above the threshold V_{SCP_LDO}, the LDO current limit is increased to I_{LIM_LDO}. If the LDO output voltage V_{OUTP} fails to ramp up above the threshold V_{SCP_LDO}, a short circuit is assumed and the system (boost, LDO and NCP) shut off and restarts in T_{HICCUP}.

NCP starts with internal MOSFET current limited to $I_{LIM\_M4\_SCP}$ and $I_{LIM\_M1\_SS.}$ Within maximum LDO startup time $T_{SS\_CP\_MAX}$, if the NCP output voltage OUTN ramps above V_{SCP_CP}, the soft-start is complete. If the NCP output voltage OUTN fails to ramp up above the threshold V_{SCP_CP}, a short circuit is assumed and the system (boost, LDO and NCP) shut off and restarts in T_{HICCUP}.

Boost Converter

The LP62702 integrates a PWM synchronous boost converter operating with valley current mode control. The inductor current is cycle-by-cycle limited. The boost switching frequency is 1.2MHz (typ.). The device is designed for high efficiency over wide output current range.

OUTP and OUTN Discharge

If V_{IN} falls below UVLO threshold or both ENP pin is pulled low, all regulators are turned off and OUTP and OUTN will be actively discharged to GND.

Protections

The LP62702 device integrates protection circuits including boost cycle by cycle current limit protection, boost short circuit, LDO over current limit and short circuit protections, charge pump negative output short circuit protection as well as thermal shutdown protection.

Boost Short Circuit

During operation, if the boost output is shorted to ground, V_{REG} voltage falls below V_{SCP_VREG}, the LP62702 device enters into hiccup mode. The boost converter turns off and restarts in $T_{HICCUP.}$

OUTP Over Current and Short Circuit

During operation, if OUTP output current is limited to I_{LIM_LDO}. If the output is over loaded or shorted to ground, the LDO output is over the current limit, OUTP falls below the voltage threshold V_{SCP_LDO} and the hiccup mode is triggered. The regulators (boost, LDO and NCP) shut off and restart in T_{HICCUP}. The system keeps in hiccup until the faults are cleared. During restart-up, the output current is limited $I_{SCP\_LDO.}$ Under the protection of hiccup, the LDO can start into short circuit and recover from short circuit.

OUTN Short Circuit

If the OUTN output is shorted to ground, the NCP output voltage falls below the voltage threshold V_{SCP_CP} and the hiccup mode is triggered. The regulators (boost, LDO and NCP) shut off and restart in T_{HICCUP}. The system keeps in hiccup until the faults are cleared. During restart-up, the output current is internally limited by NCP. Under the protection of hiccup, the NCP can start into short circuit and recover from short circuit.

Thermal Shutdown Protection

The LP62702 device enters over temperature protection if its junction temperature exceeds T_{SHUT}. During over temperature protection the device is shut down. Once the junction temperature falls below the hysteresis threshold, the device restarts.

I2C Interface Specification

The LP62702 can easily modify parameters by I2C bus. I2C is a two-wire serial interface that consists of a clock line (SCL) and a data line (SDA) with pull-up structures. The LP62702 works as a slave mode with a slave address 0x3E. The data transfer protocol follow I2C-Bus Specification's standard mode (100kbps) and fast mode (400kbps).

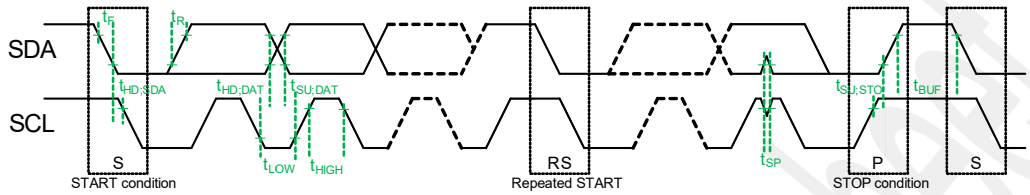


Figure 4. START and STOP Conditions

Write Data to Register

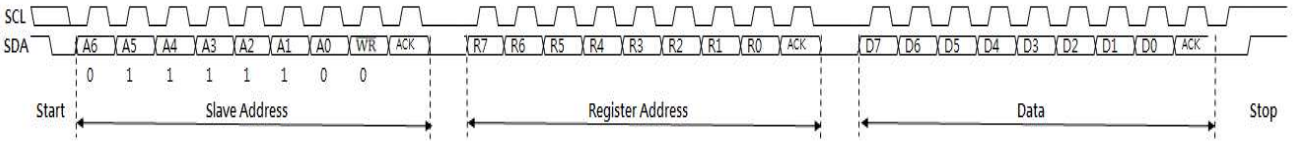


Figure 5. Write Single Byte Data to Register

Read Data from Register

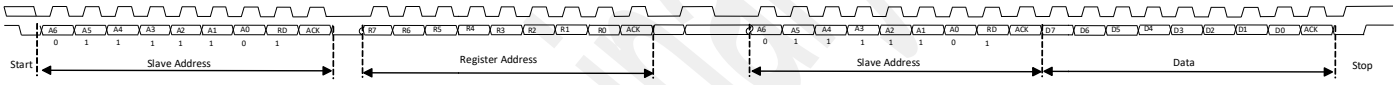


Figure 6. Read Single Byte Data from Register

Register Map

Address	Description	Default	D7	D6	D5	D4	D3	D2	D1	D0
00H	OUTP Voltage	0x0F	--		--	OUTP [4:0]				
01H	OUTN Voltage	0x0F	--		--	OUTN [4:0]				
03H	Discharge Resistor Enable	0x03	MODE	--	--	--	--	--	DIS_ OUTP	DIS_ OUTN
FFH	Control Register	0x00	WR	--	--	--	--	--	--	--

OUTP Voltage Setting (REG 00H)

OUTP Voltage							
	Default Value: 0x0F (OUTP =5.5V)						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	OUTP[4]	OUTP [3]	OUTP [2]	OUTP [1]	OUTP [0]

OUTP [4:0]			
Register	Volt (V)	Register	Volt (V)
00000	4.00	10000	5.60
00001	4.10	10001	5.70
00010	4.20	10010	5.80
00011	4.30	10011	5.90
00100	4.40	10100	6.00
00101	4.50	10101	6.10
00110	4.60	10110	6.20
00111	4.70	10111	6.30(Default)
01000	4.80	11000	6.40
01001	4.90	11001	6.50
01010	5.00	11010	6.50
01011	5.10	11011	6.50
01100	5.20	11100	6.50
01101	5.30	11101	6.50
01110	5.40	11110	6.50
01111	5.50	11111	6.50

OUTN Voltage Setting (REG 01H)

OUTN Voltage							
	Default Value: 0x0FH (OUTN =-5.5V)						
D7	D6	D5	D4	D3	D2	D1	D0
R	R	R	R/W	R/W	R/W	R/W	R/W
0	0	0	OUTN[4]	OUTN [3]	OUTN [2]	OUTN [1]	OUTN [0]

OUTN[4:0]			
Register	Volt (V)	Register	Volt (V)
00000	-4.00	10000	-5.60
00001	-4.10	10001	-5.70
00010	-4.20	10010	-5.80
00011	-4.30	10011	-5.90
00100	-4.40	10100	-6.00
00101	-4.50	10101	-6.10
00110	-4.60	10110	-6.20
00111	-4.70	10111	-6.30(Default)
01000	-4.80	11000	-6.40
01001	-4.90	11001	-6.50
01010	-5.00	11010	-6.50
01011	-5.10	11011	-6.50
01100	-5.20	11100	-6.50
01101	-5.30	11101	-6.50
01110	-5.40	11110	-6.50
01111	-5.50	11111	-6.50

Discharge Resistor Enable Setting (REG 03H)

Discharged Resistor Enable/Disable							
	Default Value : DIS_VO(Register)=0x03H						
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R/W	R/W
Mode Selection 0: 200mA (Default) 1: 100mA	0	0	0	0	0	DIS_OUTP	DIS_OUTN

DIS_OUTP		DIS_OUTN	
Register	DIS_OUTP	Register	DISP_OUTN
0	Disable	0	Disable
1	Enable	1	Enable

Control Register Setting (REG FFH)

Control Register							
	Write : Control (Register) = 0x80H, Read : Control(Register)=0x00H						
D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R
W_EPROM	0	0	0	0	0	0	0

Write to burn fuse:

1. Loading efuse values to the registers (14x8 bits)
2. Write 0x80H to burn efuse for maximum 3 times

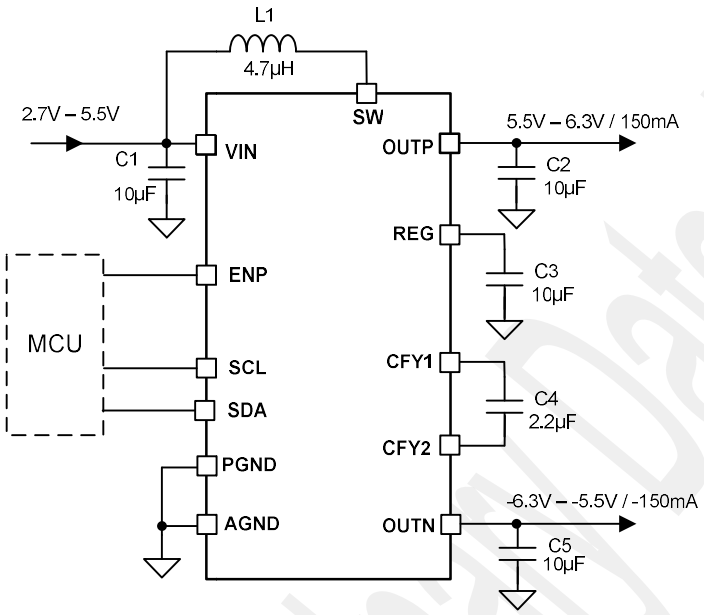
W_EPROM	
Register	Bit Description
0	Disable any registers data write into the EPROM
1	Enable all register's data to write into the EPROM

Application and Implementation

Application Information

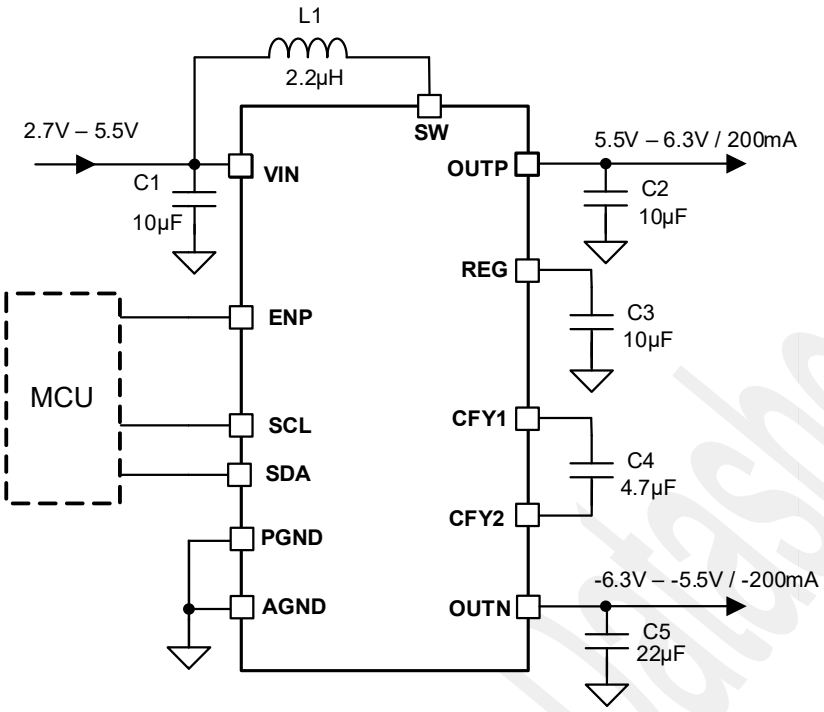
The device can be used for any applications that require positive and negative supplies, ranging from ±4V to ±6.2V and current up to 200mA. The positive and negative output voltages are independently programmable by I2C interface and their sequencing is also independently programmable by external signals at ENP pin.

Application Schematic



Designator	Values	Part Number(s)	Manufacturer	Package Size	Specifications
C1, C2, C3, C5	10 µF ±10%	GRM188R61C106KAALD	Murata	0603	16V Ceramic, X5R
C4	2.2 µF ±10%	GRM188Z71C225KE43D	Murata	0603	16V Ceramic, X7R
L1	4.7 µH ±20%	TFM252012ALVA4R7MTAA	TDK	2.5x2.0x1.2	Isat=2.2A, DCR=180mΩ

Figure 7: Typical Applications (150mA)



Designator	Values	Part Number(s)	Manufacturer	Package Size (mm)	Specifications
C1, C2, C3, C5	10 µF ±10%	GRM188R61C106KAALD	Murata	0603	16V Ceramic, X5R
C4	4.7 µF ±10%	GRM188R61C475KAAJD	Murata	0603	16V Ceramic, X7R
C5	22 µF ±20%	GRM188R61A226ME15D	Murata	0603	10V Ceramic, X5R
L1	2.2 µH ±20%	TFM252012ALVA2R2MTAA	TDK	2.5x2.0x1.2	Isat=3.3A, DCR=75mΩ

Figure 8: Typical Applications (200mA)

Application and Implementation (Continued)

Components Selection

Boost Input Capacitor Selection

10μF or higher values of low ESR ceramic capacitors are recommended at input VIN pin. A minimum effective capacitance of 4μF is required at VIN pin. Considering capacitance de-rating with higher temperature and DC bias voltages, X7R, and 10V or 16V voltage rating are recommended.

Boost Inductor Selection

A 4.7μH or 2.2μH inductor is recommended as shown in the table of Recommended Operating Conditions. In general, lower inductor DCR and larger inductor size support higher boost conversion efficiency.

Boost Output Capacitor Selection

10μF or higher values of low ESR ceramic capacitors are recommended as shown in the table of Recommended Operating Conditions. A minimum effective capacitance of 4μF is required. Higher capacitor values and higher voltage ratings can be used to improve load transient response.

LDO Output Capacitor Selection

10μF or higher values of low ESR ceramic capacitors are recommended as shown in the table of Recommended Operating Conditions. A minimum effective capacitance of 4μF is required. Higher capacitor values and higher voltage ratings can be used to improve load transient response.

Charge Pump Output Capacitor Selection

10μF, 22μF or higher values of low ESR ceramic capacitors are recommended as shown in the table of Recommended Operating Conditions. A minimum effective capacitance of 4μF is required. Higher capacitor values and higher voltage ratings can be used to improve load transient response.

Flying Capacitor Selection

A 2.2μF or 4.7uF low ESR ceramic capacitor is recommended as shown in the table of Recommended Operating Conditions. Flying capacitor values directly impact the OUTN output voltage accuracy and load transient response. A minimum effective capacitance of 1.4μF is required at a DC bias of OUTN + 0.3V. For proper operation, the flying capacitor effective value must be lower than the boost effective output capacitance. X7R and 16V voltage rating are recommended

Application and Implementation (Continued)

Application Curves

(Schematic as shown in Figure 8)

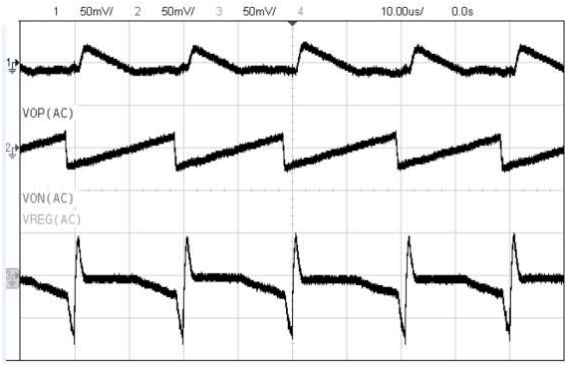


Figure 9. Output voltage ripples
(Load current from OUTP to OUTN: 10mA)

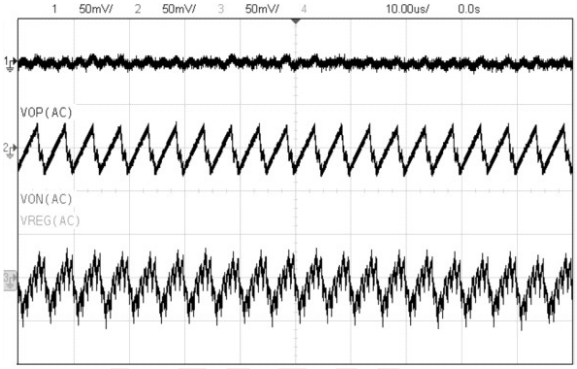


Figure 10. Output voltage ripples
(Load current from OUTP to OUTN: 80mA)

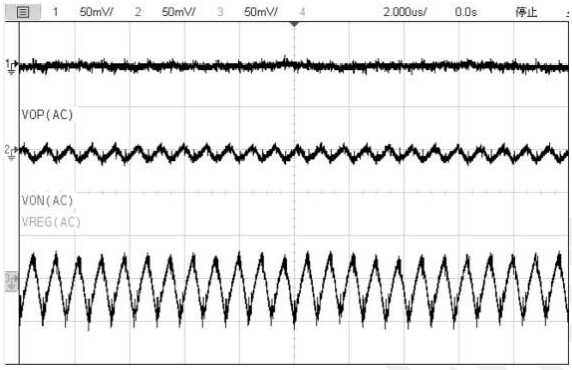


Figure 11. Output voltage ripples
(Load current from OUTP to OUTN: 150mA)

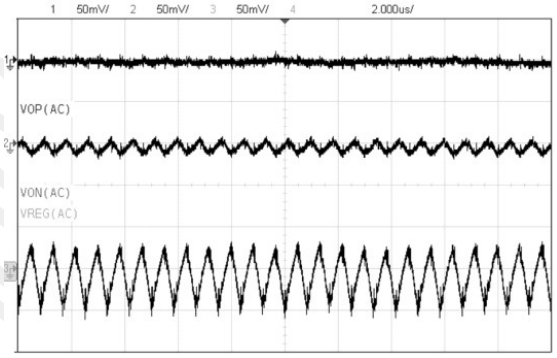


Figure 12. Output voltage ripples
(Load current from OUTP to OUTN: 200mA)

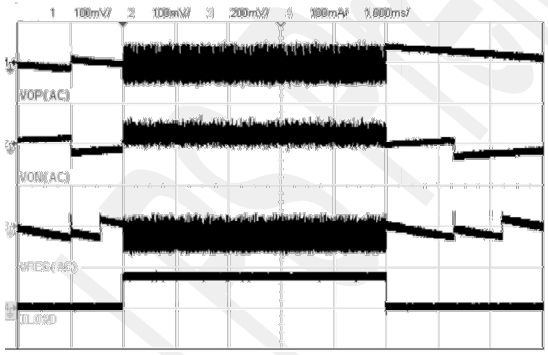


Figure 13. Load transient response
(Load from OUTP to OUTN: 0mA-80mA-0mA)

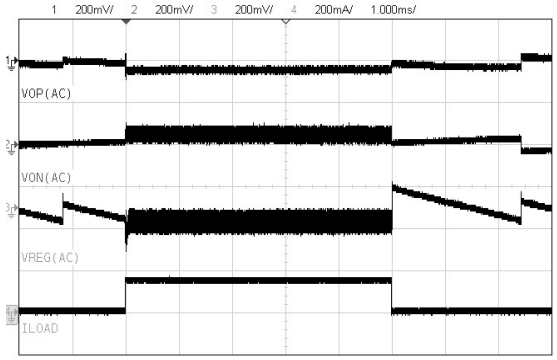


Figure 14. Load transient response
(Load from OUTP to OUTN: 0mA-150mA-0mA)

Application Curves (Continued)

(Schematic as shown in Figure 8)

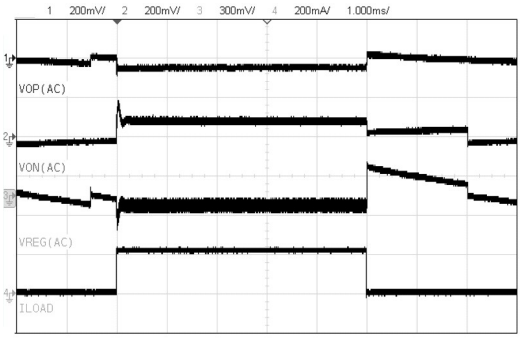


Figure 15. Load transient response
(Load from OUTP to OUTN: 0mA-200mA-0mA)

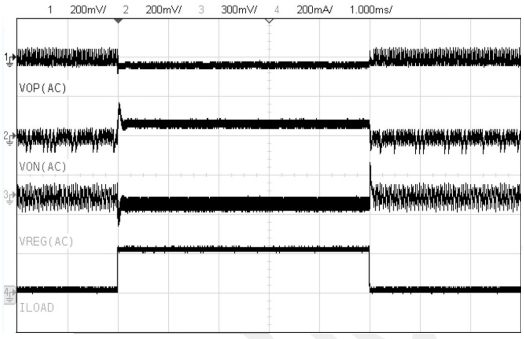


Figure 16. Load transient response
(Load from OUTP to OUTN: 10mA-200mA-10mA)

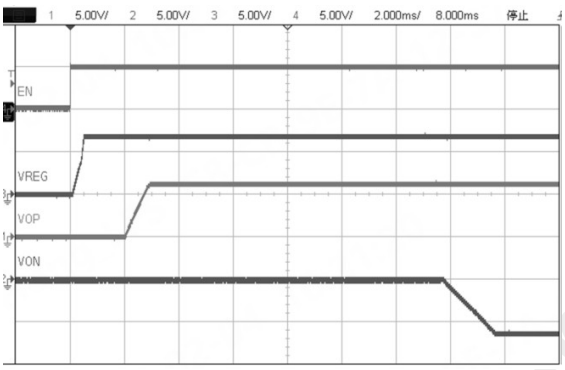


Figure 17. OUTP and OUTN power-up by EN

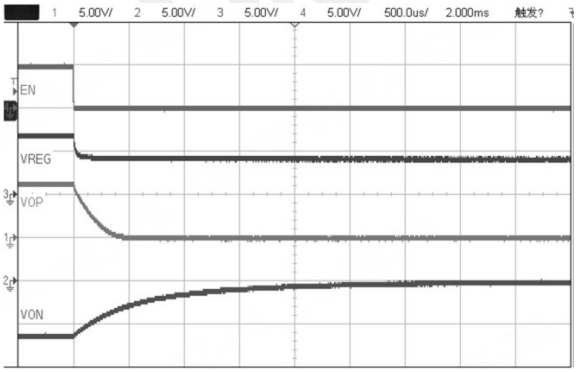


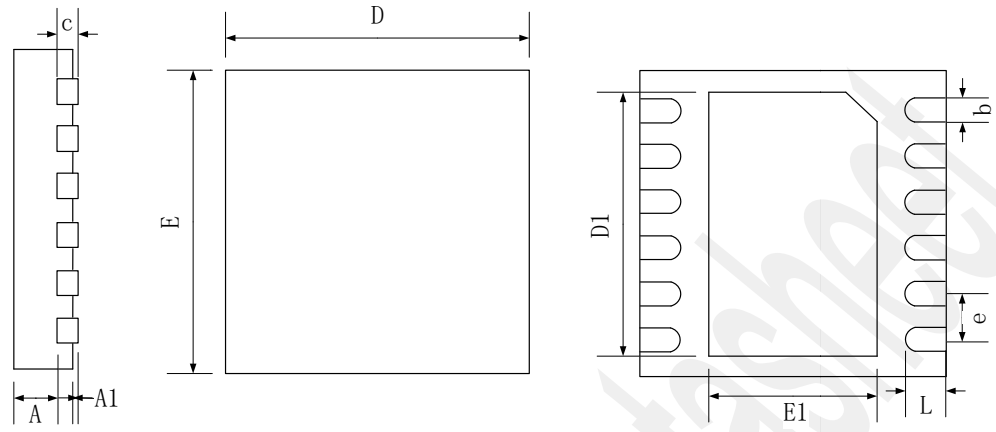
Figure 18. OUTP and OUTN power-down by EN

PCB Layout Guideline

Appropriate PCB layout is important in the power supply design. Good PCB layout minimizes EMI and allows very good output voltage regulation. The PCB layout guidelines are recommended as below:

- Decouple VIN, REG, OUTP and OUTN pins to PGND on the top layer and place decoupling capacitors as close to the pins as possible. Always avoid vias if possible because they have high inductance and resistance. If vias are necessary, always use more than one in parallel to decrease parasitics especially for power traces.
- Connect AGND and PGND ground together with at least one uninterrupted ground plane, which include power ground and analog ground.
- Place the flying capacitor as close as possible to the CFY1 and CFY2 pins and connect flying capacitors to the IC pins with short trace.
- Minimize trace length of SW node if possible to help reduce EMI emissions and noise that may couple into other portions of the converter.

Package Information

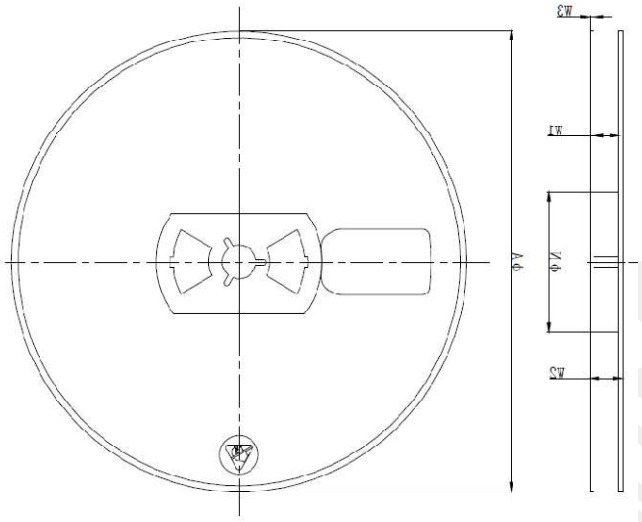


SIDE VIEW　　TOP VIEW　　BOTTOM VIEW

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.18	0.23	0.28
C		0.203 REF	
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
e		0.45 BSC	
L	0.30	0.40	0.50

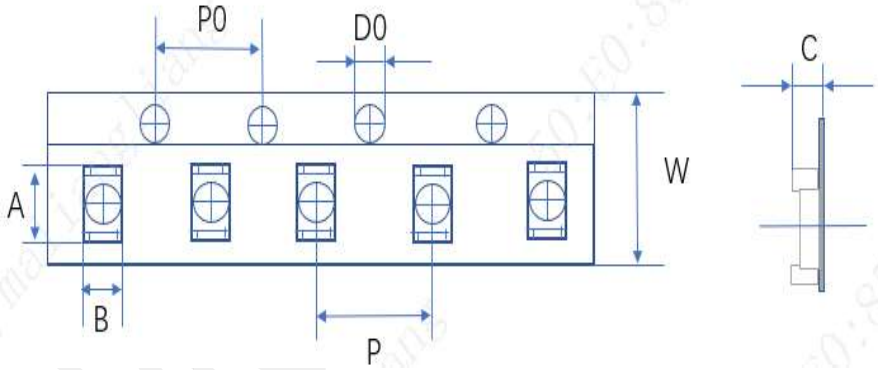
Carrier information

REEL DIMENSIONS（Unit: mm）



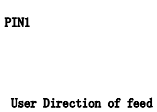
ΦA	W2
180±4	11.7±2

TAPE DIMENSIONS



口袋宽度A		口袋长度B		编带孔中心间距P0		IC中心间距P		孔径D0		编带宽度W		编带厚度C	
Size(mm)	Tolerance	Size(mm)	Tolerance	Size(mm)	Tolerance	Size(mm)	Tolerance	Size(mm)	Tolerance	Size(mm)	Tolerance	Size(mm)	Tolerance
1.29	±0.1	2.09	±0.1	4	±0.2	4	±0.2	1.5	±0.2	8	±0.6	0.96	±0.06

PIN1 AND TAPE FEEDING DIRECTION



Revision History

Revision	Date	Change Description
Rev 0.1	02/10/2023	Initial Release
Rev 0.21	10/18/2023	Initial Release - Revision
Rev 0.6	03/03/2024	Update power-up and power-down waveforms in Application Curves
Rev 0.7	03/06/2024	Update Package Information
Rev 0.8	05/21/2024	Update Top Marking
Rev 0.9	07/16/2025	Update I2C data read example figure