LP7820B

30V, MCU Integrated, 1A Switch Mode TWS Solution

Features

- Input over-voltage protected up to 30V
- MCU
  - 8-bit 8051 core
  - Compliance with MCS-51 instruction set
  - DPTRs
  - Support 16MHz high-speed oscillator and 10kHz low-speed oscillator
  - Up to 32K byte Flash
  - Programmable 8K/6K/4K/2K/0K byte LDROM
  - Up to 1K RAM
  - Support 2 independent UART channels
  - Support 2 16-bit counter/timer
  - Integrated 12-bit, 8-channel ADC
- Charge management
  - Programmable charge current up to 1A
  - 93% charge efficiency at 0.5A from 5V input
  - Programmable floating voltage with 0.35% accuracy
  - Programmable trickle charge and termination current with minimum 10mA termination current
- Automatic re-charge and thermal foldback
- Power path management
- Boost converter with up to 0.6A output
- Two independent load switches with up to 250mA output for each channel
- Earphone insertion and removal detection
- Bi-directional communication with earphones
- NTC management (JIETA Compliance)
- HALL detection
- Rich protections: UVLO, OVP, SCP
- 4mm X 4mm QFN-28 package
- RoHS Compliant and 100% Lead (Pb) Free

Applications

- TWS
- Wireless Microphone
- Smart Glasses
- Electrical Tool
- Solar-cell charger

General Description

The LP7820B is a fully integrated TWS charging case solution with MCU, charger, boost and load switches. The LP7820B has built-in an 8-bit MCU core with up to 32K-byte flash and 1K-byte RAM. A low on-resistance BUS-FET is integrated to manage the input power from the VIN pin. A bidirectional buck or boost converter is integrated to manage charging and discharging of the battery. The buck charger supports up to 1A charging current with up to 95% efficiency. The ultra-low quiescent current boost converter consumes less than 2μA quiescent current and supports up to 0.6A output current. Two independent load switches feature earphone insert detection, removal detection and provide power from the PMID pin to the VOL pin and VOR pin with ultra-low voltage drop. An NTC circuit is offered to manage the temperature range that charging or discharging is allowed. The LP7820B offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the VIN input and the battery to meet the system loading needs.

Multiple features are offered for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), etc. When powered by a battery, LP7820B can operate with only 8μA current.

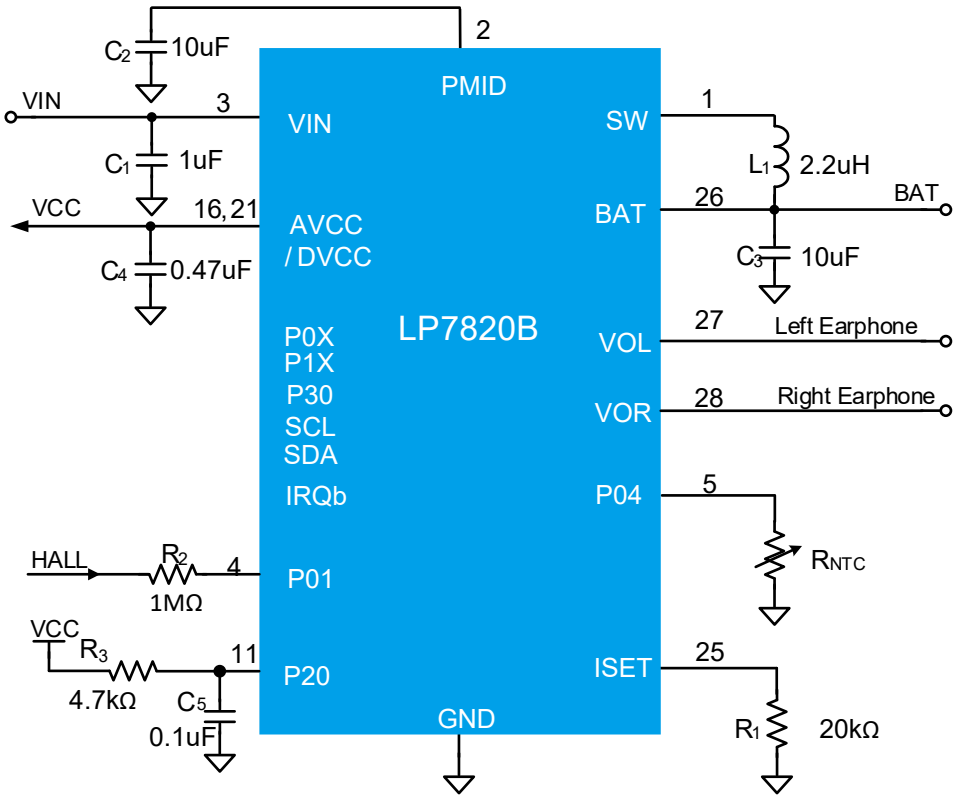
The whole System is in a 28-pin 4 X 4 QFN package.

Order Information

LP7820B □□ □

- F：Green/Pb-Free
- Package Type
  - QV : QFN

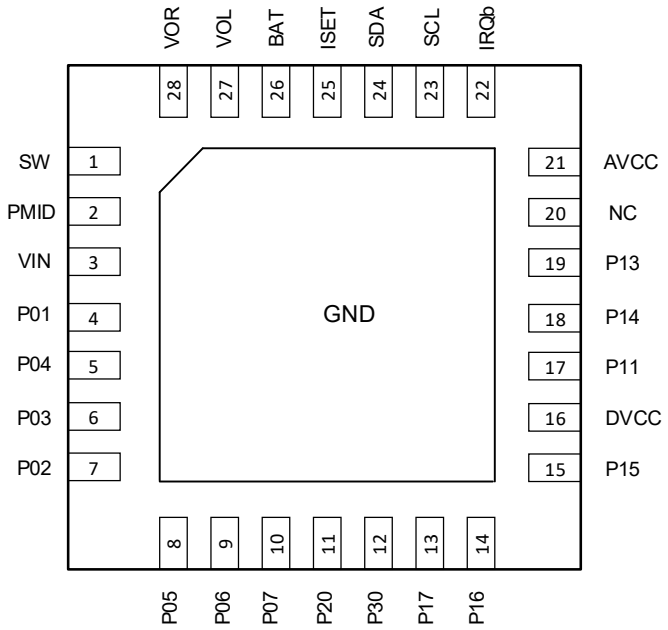
Typical Application Circuit



Device Information

Part Number	Top Marking	Package	Shipping	MSL
LP7820BQVF	LPS LP7820B YWX	28-pin 4 X 4 QFN	3K/REEL	LEVEL 3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. MSL: Moisture Sensitivity Level according to JEDEC Standard.				

Pin Diagram



LP7820B Pinout

Pin Description

Pin #	Name	Description
1	SW	Switch node of the boost converter/ buck charger.
2	PMID	Power input for the buck charger and power output for the load switches. A 10uF or higher ceramic capacitor is required between this pin and the GND pins.
3	VIN	Input voltage that is connected to the positive input of the USB port. 30V maximum voltage rating. A 1uF or higher value input decoupling capacitor must be connected to this pin and the GND pins. An additional 100nF capacitor should be placed between this pin and GND to decouple noise.
4	P01	GPIO. This pin is reserved for HALL detection
5	P04	GPIO. This pin is reserved for NTC detection. Connect a NTC resistor with beta=3950, 10kΩ typical resistance. AIN5: ADC input channel 5
6	P03	GPIO PWM5: PWM output channel 5 IC5: Timer capture channel 5 AIN6: ADC input channel 6
7	P02	GPIO TCK input RXD_1: UART Data input
8	P05	GPIO PWM2: PWM output channel 2 IC6: Timer capture channel 6 T0: Timer 0
9	P06	GPIO TXD_0: UART0 Data output AIN3: ADC input channel 3 PWM4: PWM output channel 4

10	P07	GPIO RXD_0: UART0 Data input AIN2: ADC input channel 2 PWM0: PWM output channel 0
11	P20	RSTB. Reset pin
12	P30	GPIO INT0: Interrupt 0 input XIN: External clock input if ECLK mode AIN1: ADC input channel 1
13	P17	GPIO INT0: Interrupt 2 input AIN0: ADC input channel 0
14	P16	GPIO TMS TXD_1: UART_1 Data output
15	P15	GPIO PWM5: PWM output channel 5 IC7: Timer capture channel 7 CS: SPI slave select pin
16	DVCC	Digital power supply. Connect this pin with AVCC pin.
17	P11	GPIO PWM1: PWM output channel 1 IC1: Timer capture channel 1 AIN7: ADC input channel 7 CLO: System clock output
18	P14	GPIO SDA: I2C data pin PWM1: PWM output channel 1
19	P13	GPIO SCL: I2C clock pin
20	NC	No connection.
21	AVCC	LDO output pin. This pin is also the analog power supply. A 0.47uF capacitor must be connected to this pin and the GND pin.
22	IRQb	This pin is reserved as KEY input detection A 100nF capacitor should be placed between this pin and GND to decouple noise. Open drain configuration and need level pull-up resistor.
23	SCL	This pin is reserved as clock line of the I2C bus (SCL). Open drain configuration and need 10kΩ level pull-up resistor.
24	SDA	This pin is reserved as data line of the I2C bus (SDA). Open drain configuration and need 10kΩ level pull-up resistor.
25	ISET	This pin set the charging current. Don't leave this pin open.
26	BAT	Battery voltage sense pin of the buck charger. A 10uF or higher value decoupling capacitor must be connected to this pin and the GND pins.
27	VOL	Left earphone power output pin.
28	VOR	Right earphone power output pin.
Thermal PAD	PGND	Power Ground pin. This is also the thermal dissipation PAD. Connect to ground plane.

Absolute Maximum Ratings (Note 1)

VIN to GND ---------- -0.3V to 30V
All other pins to GND ---------- -0.3V to 6.3V
SW to GND (5ns transient) ---------- -1V to 8V
Junction Temperature (T_J) ---------- -40°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec)---------- 260℃

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 55℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	4.1		5.7	V
I_{IN}	Input current			2	A
T_A	Ambient temperature range	-40		85	°C
C_{IN}	Input decoupling capacitor, 25V rating or higher		1		μF
C_{pmid}	System capacitor, 10V rating or higher		10		μF
C_{bat}	Battery capacitor, 10V rating or higher		10		μF

Electrical Characteristics

(The specifications are at $V_{UVLO\_IN} < V_{IN} < V_{OVP\_IN}$, V_{BAT} =3.6V, T_A = -40°C to +85°C and T_A = 25°C for typical values unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{UVLO_IN}	VIN UVLO	V_{IN} falling	3.55	3.7	3.85	V
	Hysteresis			150		mV
V_{OVP_IN}	VIN OVP threshold	V_{IN} rising, 5.85V option	5.7	5.85	6.0	V
	Hysteresis			150		mV
I_{q_IN}	Input quiescent current	V_{IN} =5.0V, V_{BAT} =4.3V, ENCHG=1		200		μA
R_{DSON_IN}	BUS-FET on- resistance	V_{IN} =5.0V		0.3		Ω
T_{ss}	Soft-start time of BUS-FET			150		μs
BATTERY SECTION						
V_{BAT_POR}	BAT Power-on-reset	V_{BAT} rising			2.6	V
	Hysteresis			180		mV
I_{BAT}	Quiescent current from BAT	Discharge mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=01, EN_BST=1, MCU PD mode not include NTC bias current		32		μA
		Standby mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=01, EN_BST=1,MCU PD mode		14		μA
		Standby mode, V_{IN} =0V, V_{BAT} =4.5V, PUP[1:0]=00, EN_BST=0,MCU PD mode		12		μA
		Charge mode, V_{IN} =5V, V_{BAT} =4.5V, EN_CHG=1		3		μA
CHARGE MANAGEMENT						
V_{TRI}	Trickle charge voltage threshold	V_{BAT} rising, V_{TRI}=3.0V option	2.95	3.0	3.05	V
	Hysteresis			100		mV
I_{TRI}	Trickle charge current	R_{ISET}=10K, I_{CC} =1000mA, 10%I_{CC}	90	100	110	mA
		R_{ISET}=10K, I_{CC} =1000mA, 2%I_{CC}	18	20	22	mA
I_{CC}	CC current	25°C, 1000mA R_{ISET}=10K, ICCR[2:0]=000	-5		+5	%
		From -10°C to 85°C, 1000mA R_{ISET}=10K, ICCR[2:0]=000	-10		+10	%
		25°C, 500mA R_{ISET}=10K, ICCR[2:0]=100	-5		+5	%
		25°C, 125mA R_{ISET}=10K, ICCR[2:0]=111	-10		+10	%
V_{CV}	CV voltage	25°C, V_{CV}=4.2V	-0.35		0.35	%
		From -10°C to 85°C, V_{CV}=4.2V	-0.6		0.6	%
		25°C, V_{CV}=4.35V	-0.35		0.35	%
		25°C, V_{CV}=4.4V	-0.35		0.35	%
V_{RECHG}	Re-charge threshold	V_{BAT} falling, Reference to CV voltage		-150		mV
t_{drechg}	Recharge deglitch time[Note 2]			30		ms

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{TERM}	Charge termination current	I_{CC} =1000mA, 12%I_{CC}	110	120	130	mA
		I_{CC} =1000mA, 3%I_{CC}	27	30	33	mA
t_{dterm}	termination deglitch time[Note 2]			30		ms
T_{therm}	Thermal foldback threshold[Note 2]		100	120	140	℃
f_{SW1}	Buck switching frequency	V_{IN} =5.0V,V_{BAT} =3.6V, I_{CC}=800mA		1.1		MHz
R_{DSON_HS}	HS-FET on resistance	V_{BAT} =3.6V, V_{PMID}=5.1V		0.24		Ω
R_{DSON_LS}	LS-FET on resistance	V_{BAT} =3.6V, V_{PMID}=5.1V		0.12		Ω
I_{BUCK_LIM}	Buck HS-FET peak current limit			1.8		A
BOOST CONVERTER						
V_{PMID}	Boost output voltage accuracy	5.1V option	5.03	5.1	5.15	V
I_{BST_LIM}	Boost LS-FET peak current limit			2.2		A
I_{BYP_LIM}	Boost HS-FET bypass mode current limit	V_{BAT}=4.2V, V_{PMID}=3.5V	0.6	0.8		A
f_{SW2}	Boost switching frequency	V_{BAT}=3.6V, V_{PMID}=5.1V, 500mA		1.3		MHz
V_{BAT_UV}	Battery UVLO	V_{BAT} falling, 3.3V option	3.25	3.3	3.35	V
	Hysteresis	V_{BAT} rising		0.2		V
t_{d_BATUV}	BAT_UV deglitch time[Note 2]			30		us
NTC MANAGEMENT						
I_{NTC}	NTC bias current	-10℃/0℃/10℃/15℃, (R_{NTC}=10K)	19.2	20	20.8	uA
		45℃/60℃, (R_{NTC}=10K)	96	100	104	uA
T_{-10}	-10℃ threshold	V_{NTC} rising	1.07	1.1	1.13	V
	Hysteresis			1		V
T_0	0℃ threshold	V_{NTC} rising	0.63	0.65	0.67	V
	Hysteresis			0.6		V
T_{10}	10℃ threshold	V_{NTC} rising	0.385	0.4	0.42	V
	Hysteresis			0.37		V
T_{15}	15℃ threshold	V_{NTC} rising	0.3	0.31	0.32	V
	Hysteresis			0.28		V
T_{45}	45℃ threshold	V_{NTC} falling	0.43	0.44	0.45	V
	Hysteresis			0.47		V
T_{60}	60℃ threshold	V_{NTC} falling	0.24	0.25	0.26	V
	Hysteresis			0.28		V
ULTRA-LOW QUIESCNET CURRENT LDO						
V_{CC}	LDO output voltage accuracy	V_{BAT} =3.6V, VCC[1:0]=00, 5mA load	2.69	2.72	2.75	V
I_{VCC}	LDO output current capability	V_{BAT} =3.6V, VCC[1:0]=00, 5% VCC drop		100		mA
LOAD SWITCH (VOL, VOR)						
I_{PUP}	Load insert detection current	PUP[1:0]=10, 7μA pull up current, V_{BAT} =3.6V	6	6.5	7	uA

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{INSERT}	Load insert detection threshold	V_{BAT} =3.6V, V_{PMID} =5.1V, reference to PMID voltage		-0.7		V
t_{dins}	Load insert deglitch time[Note 2]			30		ms
R_{on_EAR}	$R_{ds,on}$ of VOL/R	V_{PMID}=5.1V		650		mΩ
I_{LS_LIM}	Load switch current limit	25℃, EICC=200mA	190	200	210	mA
		25℃, EICC=20mA	18	20	22	mA
I_{LS_LL}	Load switch light load current threshold	EEOC=4mA	3.5	4	5	mA
		EEOC=16mA	14	16	18	mA
t_{dLL}	Load switch light load deglitch time[Note 2]			30		ms
V_{clamp}	VOL/R output clamp	4.6V option	4.55	4.6	4.65	V
GPIO						
V_{IH}	Logic Input High	Smitter trigger	0.7V_{CC}			V
V_{IH1}	Logic Input High	TTL	0.2V_{CC}+0.9			V
V_{IL}	Logic Input Low	Smitter trigger			0.3V_{CC}	V
V_{IL1}	Logic Input Low	TTL			0.2V_{CC}-0.1	V
V_{OL}	Output Low				0.4	V
V_{OH}	Output High	VCC>=2.7V	2.4			V
		VCC=1.8V	1.4			V
R_{up}	Pull Up resistor			60		kΩ
R_{down}	Pull Down resistor			60		kΩ
I_{leak}	Leakage current			1		uA
Oscillator						
F_{HIRC}	16MHz			±1		%
F_{LIRC}	10kHz			±10		%
ADC						
I_{AVDD}	ADC current consumption			500		μA
V_{AIN}	ADC input range		0		VCC	V
N_R	Resolution			12		bit
DNL				4		LSB
INL				±3		LSB
OE	Offset error			±2		LSB
TUE	Full scale error			8		LSB
F_C	Transfer rate			200		ksps
T_{ADCEN}	ADC startup time			15		uS
C_{IN}	ADC input capacitance			3.6		pF

Note 2: Not production tested. Guaranteed by design.

Typical Characteristics

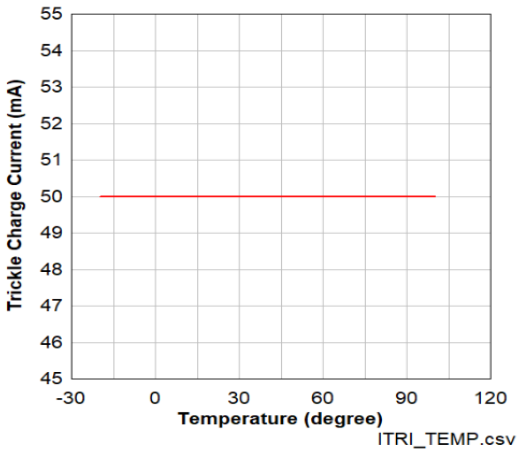


Figure 1. I_{TRI} vs. Ambient Temperature. V_{BAT}=2.5V, 50mA

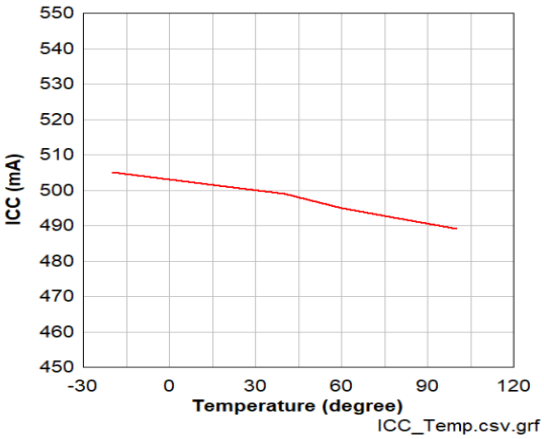


Figure 2. I_{CC} vs. Ambient Temperature. V_{BAT}=3.6V I_{CC}=500mA

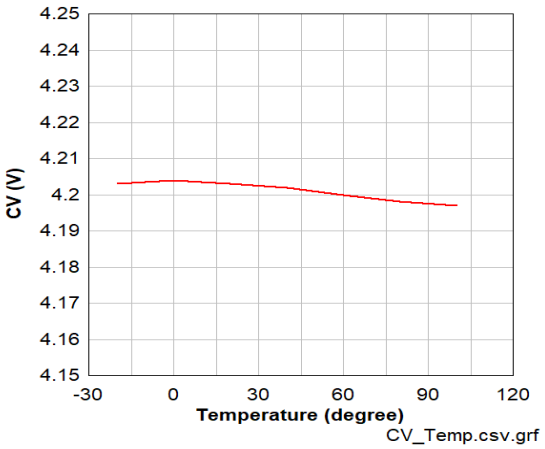


Figure 3. V_{CV} vs. Ambient Temperature. CV=4.2V

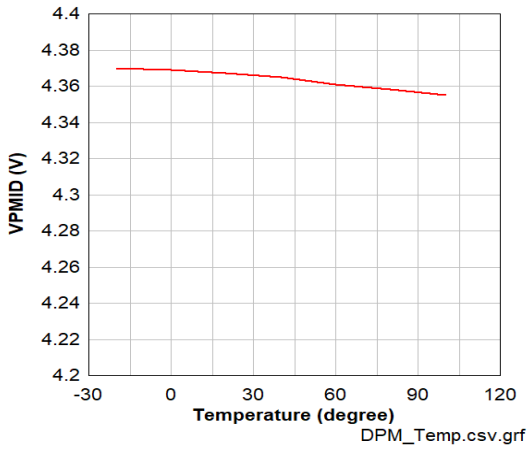


Figure 4. V_{DPM} vs. Ambient Temperature.

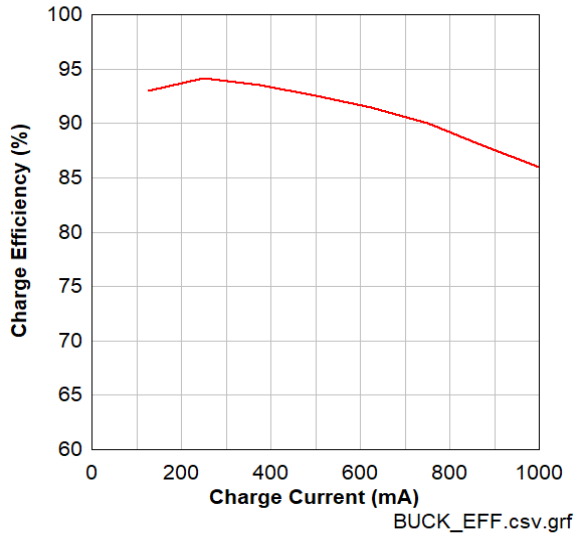


Figure 5. Charger Efficiency. V_{BAT}=3.8V, 2.2μH

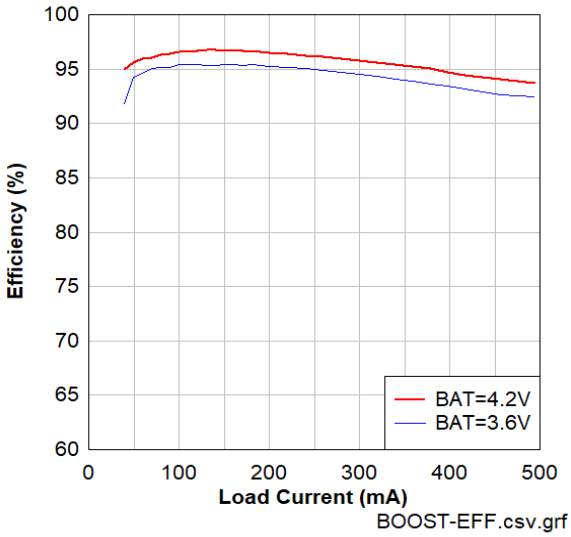


Figure 6. Boost Efficiency. V_{PMID}=4.5V, 2.2μH

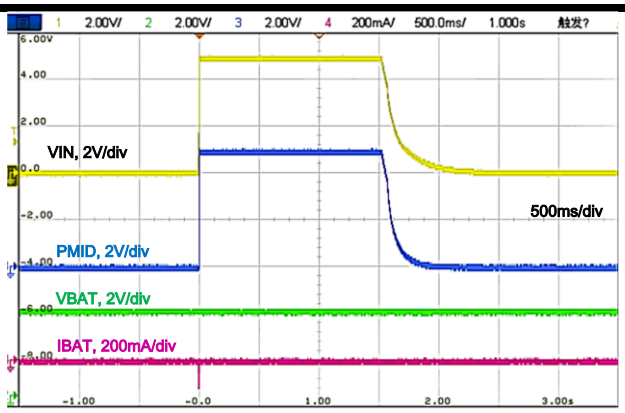


Figure 7. VIN plugged in and unplugged with V_{BAT}=3.6V (EN_BST=EN_CHG=0)

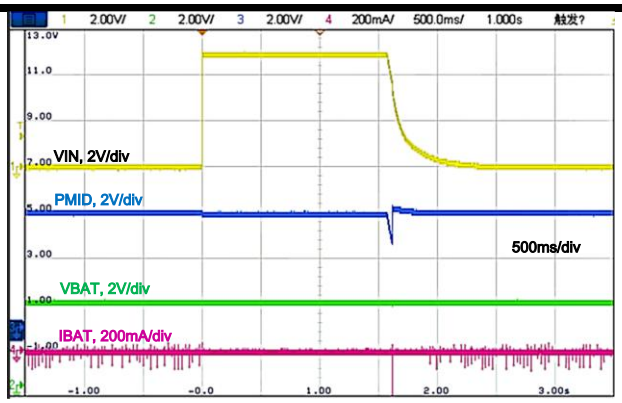


Figure8. VIN plugged in and unplugged with V_{BAT}=3.6V (EN_BST=1, EN_CHG=0)

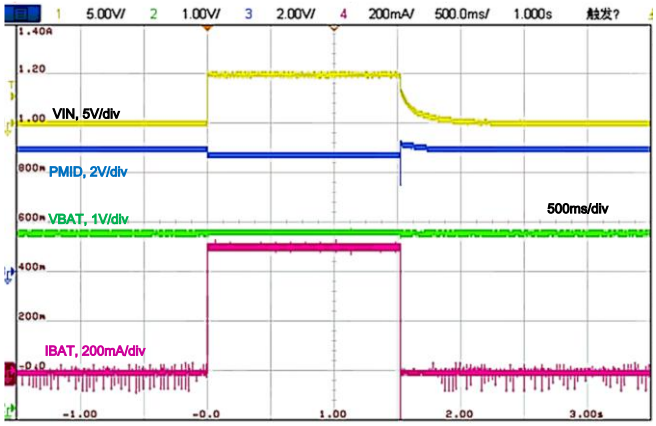


Figure9. VIN plugged in and unplugged with ICC=500mA, V_{BAT}=3.6V(EN_BST=EN_CHG=1)

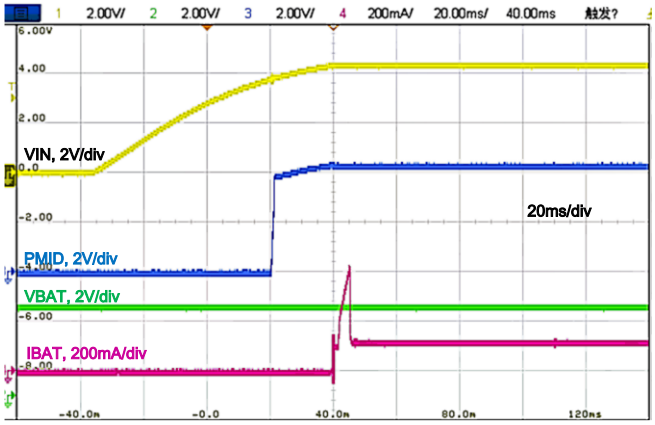


Figure 10. VIN plugged in and unplugged with VIN DPM, ICC=500mA, V_{BAT}=3.6V

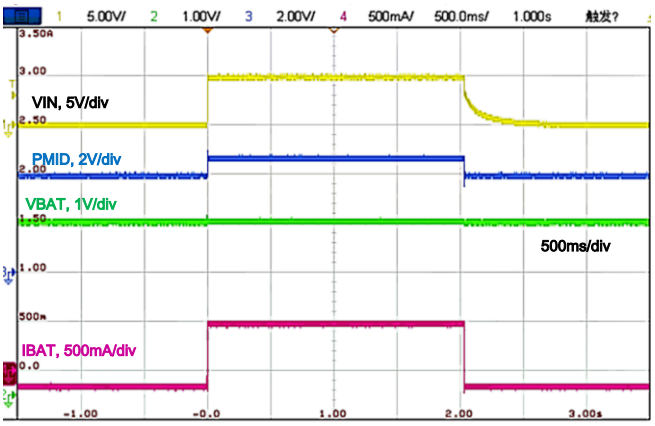


Figure 11. VIN powerup with ICC=500mA, VOL sinks 150mA, V_{BAT}=3.6V

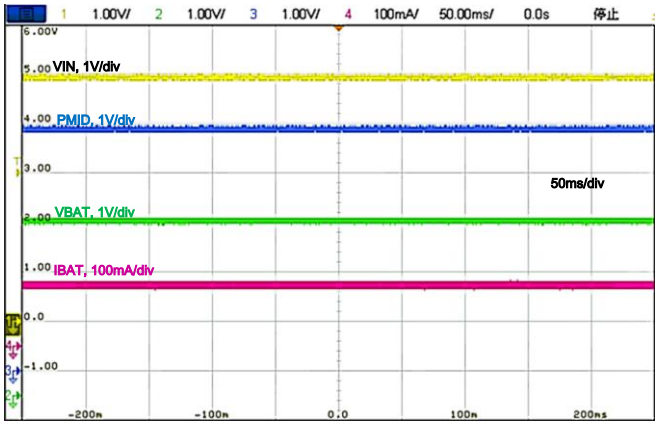


Figure 12. Switch charge, ICC=125mA, V_{BAT}=3.6V

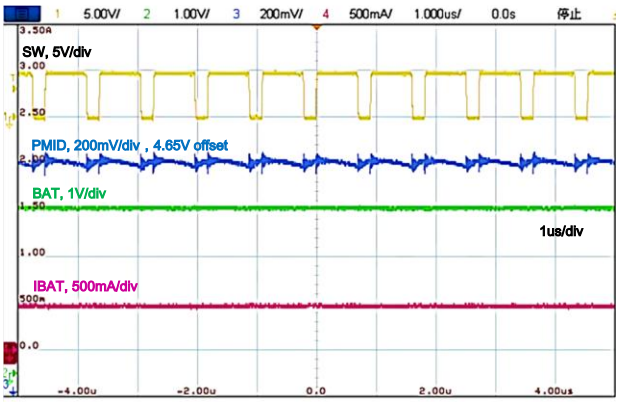


Figure13. Switch charge, ICC=500mA, V_{BAT}=3.8V

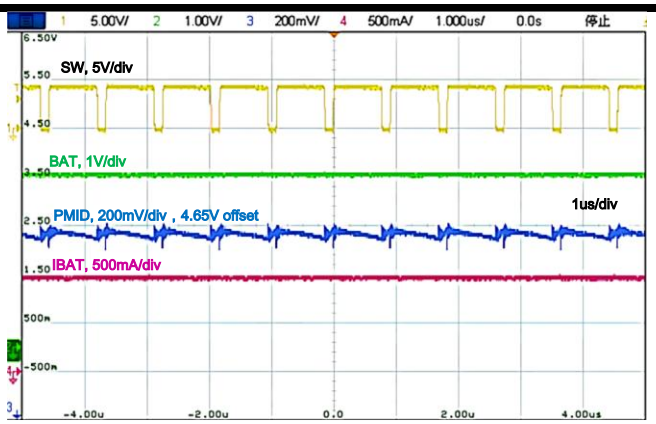


Figure14. Switch charge, ICC=1A, V_{BAT}=3.8V

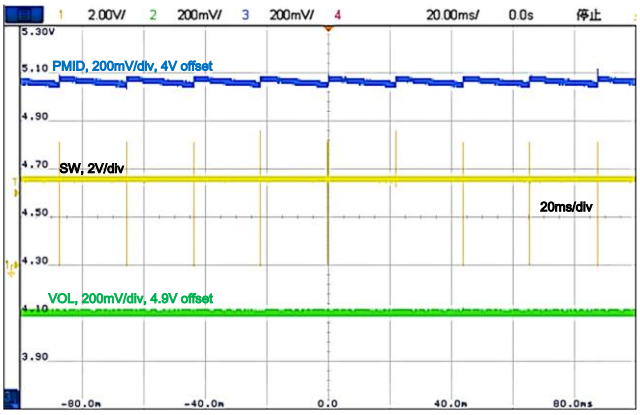


Figure15. BOOST operation, 10mA,
V_{BAT}=3.6V, V_{PMID}=4.6V

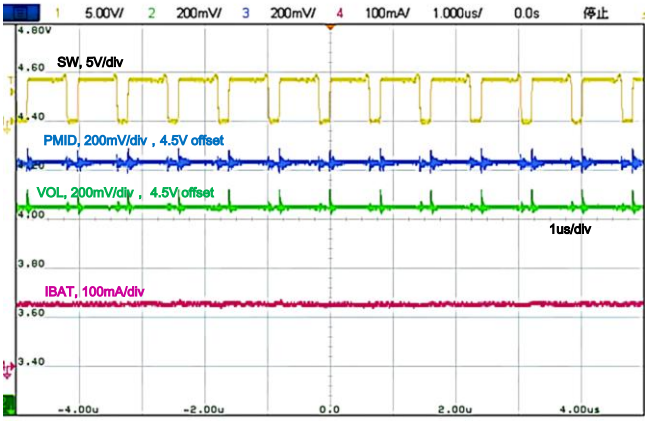


Figure16. BOOST operation, EICC=100mA load,
V_{BAT}=3.6V, V_{PMID}=4.6V

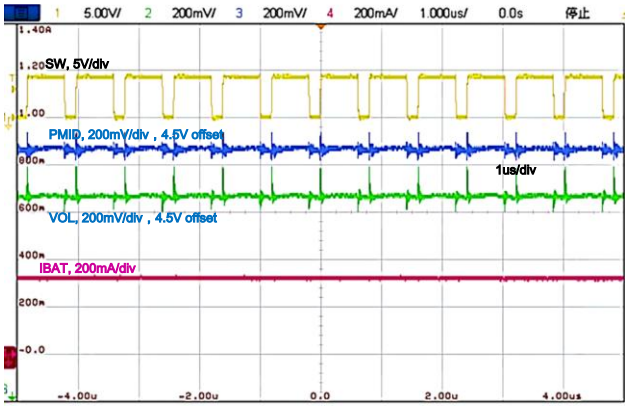


Figure17. BOOST operation, EICC=250mA load,
V_{BAT}=3.6V, V_{PMID}=4.6V

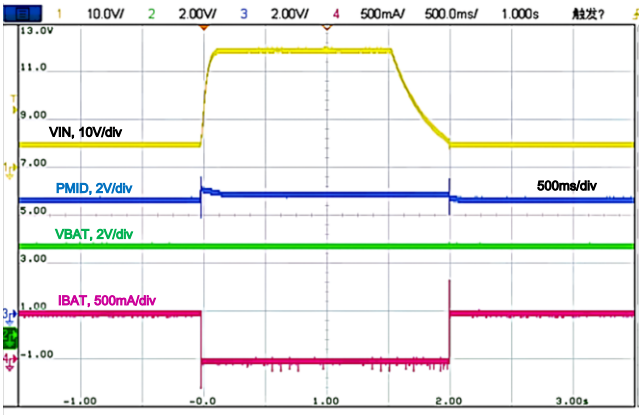
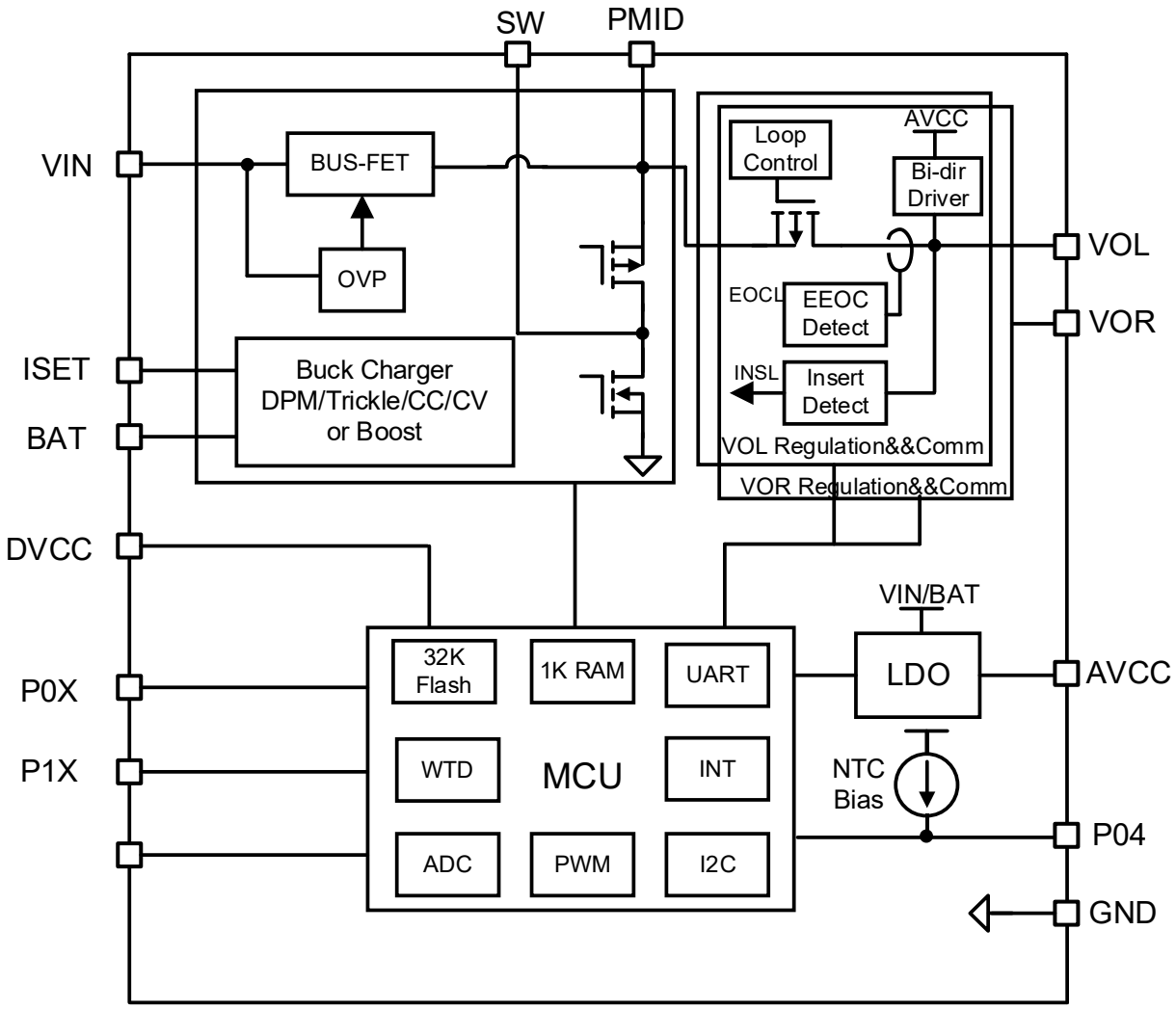


Figure18. Input OVP and Release

Functional Block Diagram



Detailed Description

Overview

The LP7820B is a fully integrated TWS charging case solution with MCU, charger, boost and load switches. The LP7820B has built-in an 8-bit MCU core with up to 32K-byte flash and 1K-byte RAM. A low on-resistance BUS-FET is integrated to manage the input power from the VIN pin. A bidirectional buck or boost converter is integrated to manage charging and discharging of the battery. The buck charger supports up to 1A charging current with up to 95% efficiency. The ultra-low quiescent current boost converter consumes less than 2μA quiescent current and supports up to 0.6A output current. Two independent load switches feature earphone insert detection, removal detection and provide power from the PMID pin to the VOL pin and VOR pin with ultra-low voltage drop. An NTC circuit is offered to manage the temperature range that charging or discharging is allowed. The LP7820B offers power path management that allows the system to be powered up with a fully-discharged battery. It can dynamically manage the power from the VIN input and the battery to meet the system loading needs.

Multiple features are offered for the safe operation of the system, including input voltage OVP (over voltage protection), UVLO (under voltage lockout), OTP (over temperature protection), SCP (short circuit protection), etc. When powered by a battery, LP7820B can operate with only 8μA current.

Power-on Reset (POR)

The LP7820B performs a POR when either the VIN input voltage or the BAT pin voltage is higher than the $V_{BAT\ POR}$ rising threshold. All registers will be set to default values when performing the POR. Refer to the Register Map section for more register information.

Input Section

The input section contains the BUS-FET and its control circuitry to realize UVLO, OVP and RCP (Reverse current protection).

UVLO and OVP

The input section control circuit monitors the VIN-pin voltage to determine when to turn on or off the BUS-FET. The LP7820B detects an over-voltage event when the input voltage is higher than OVP threshold and turns off the BUS-FET immediately. The LP7820B detects an under voltage (UV) event when the input voltage is lower than V_{UVLO_IN} falling threshold. The LP7820B turns off the BUS-FET immediately as well.

VIN Power Good (PGD)

When it is between the UVLO and the OVP threshold, the input voltage is in a power-good (PGD) range. The BUS-FET is turned on slowly and the PGD bit of the Status Register 0 is set after a 30ms deglitch time. If the VIN voltage falls off the PGD range, the BUS-FET is turned off.

Reverser Current Protection

If the BUS-FET is reversely biased, i.e. the VIN-pin voltage is only 200mV higher than the BAT-pin voltage, the BUS-FET is turned off immediately and the reverse current is fully blocked. The RCP comparator has a typical 50mV hysteresis.

Charge Management

The LP7820B will charge the battery through the BUCK charger when the PMID-pin voltage is 150mV higher than the battery voltage. The charger operates with three charging modes, i.e., trickle, CC, and CV modes. During trickle charge mode, the LP7820B is a linear charger to achieve high low-current accuracy. The LP7820B automatically enters switch mode when LP7820B exits the trickle charge mode and enters the CC mode. The LP7820B enters linear mode again when the battery is close to be fully charged. A typical charging cycle is shown in Figure 19. The charging currents and CV are programmable by I^2C. The EN_CHG bit of Control Register 3 can enable the charger. The following describes the details of the charging operation.

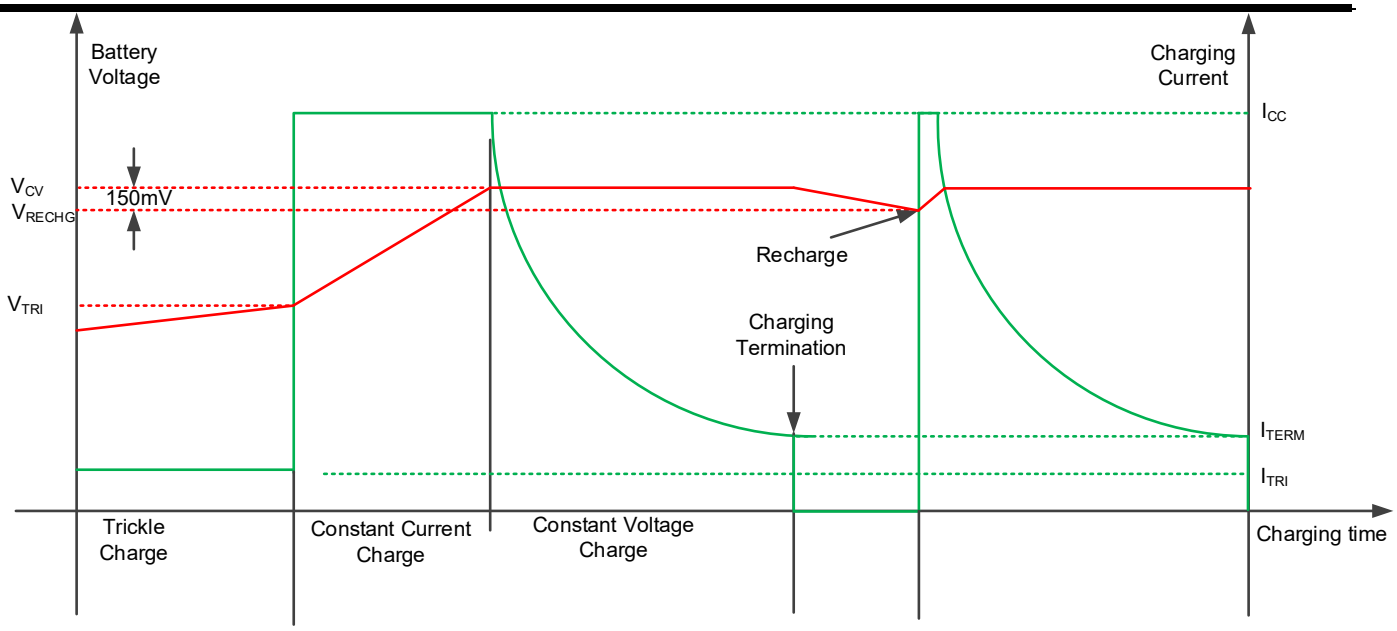


Figure19. 5V normal charging profile

Start of a Charge Cycle

The charger can be in a charge cycle when all the conditions below are valid,

- PGD = 1
- EN_CHG = 1
- The NTC-pin voltage is in the range of T_0 and T_{45} given in the Electrical Characteristics table.

A new charge cycle will start when the last of the above conditions change from invalid to valid. For example, when the NTC-pin voltage and the PGD are valid when the EN-CHG bit is set.
The CHG[1:0] bits of the Status Register0 is set to 00 before a charge cycle.

Trickle Mode

The charger enters the trickle mode at the beginning of a charge cycle if the battery voltage is below the trickle-charge voltage threshold (V_{TRI}) that is programmable via the VTRI bit of the Control Register 0. The default value is 3.0V. The trickle-charge current is programmable with the R_{ISET} resistance and the ITRI[1:0] bits of the Control Register 0. The LP7820B is a linear mode charger when the battery voltage is below the V_{TRI}.
The CHG[1:0] bits of the Status Register0 is set to 01 in trickle mode.

CC Mode

The LP7820B starts the CC mode when the battery voltage is higher than the trickle threshold but lower than the CV threshold. The charging current is determined by the resistor connected at ISET pin and the ICCR[2:0] bits of the Control Register 1. The CC current is calculated with the equation below:

$$ICC = ICCR[2:0] * \frac{10000}{R_{ISET}} \ (A)$$

For example, the CC current is 400mA if the R_{ISET} is 25kΩ and ICCR[2:0]=000. The CC current is programmable from 10~1000mA and the LP7820B works in switch mode all the time when in CC mode. The default charging current is 100% the current set by the R_{ISET}.
The CHG[1:0] bits of the Status Register0 is set to 01 in CC and CV mode.
Please be noted: The CC current should always 2.5 times higher than the termination current. Please follow the **table 1** to configure the ICCR[1:0] and ITER[1:0] registers.

Table 1 ICCR and ITERM Combination

ITERM Ratio / ICC Ratio	ITERM [1:0] =00, 3%	ITERM [1:0] =01, 6%	ITERM [1:0] =10, 8%	ITERM [1:0] =11, 12%
ICCR [2:0] =111, 12.5%	YES	NO	NO	NO
ICCR [2:0] =110, 25%	YES	YES	YES	NO
ICCR [2:0] =101, 37.5%	YES	YES	YES	YES
ICCR [2:0] =100, 50%	YES	YES	YES	YES
ICCR [2:0] =011, 62.5%	YES	YES	YES	YES
ICCR [2:0] =010, 75%	YES	YES	YES	YES
ICCR [2:0] =001, 87.5%	YES	YES	YES	YES
ICCR [2:0] =000, 100%	YES	YES	YES	YES

CV Mode

The LP7820B starts the CV mode when the battery voltage reaches the CV threshold. The charging current decreases gradually until the charging termination is triggered in this mode. The CV voltage is programmable via the CV[2:0] bits of the Control Register 0. The default value is 4.2V.

Charge Cycle Termination

When the BAT voltage is higher than the recharge voltage and the charging current drops to the termination current threshold, which is programmable with the R_{ISET} resistance and the ITERM[1:0] bits of the Control Register 0. the charging termination is triggered. The charging is terminated immediately and the CHG[1:0] bits of the Status Register0 is set to 11. Please be noted the termination current should be adjusted according to table 1.
Termination is disable in VIN DPM and thermal regulation.

Recharge

A re-charge cycle will start when the battery voltage falls 150mV below the CV voltage while the VIN voltage is still present after a typical 30ms deglitch time. The LP7820B works in switch mode again at the beginning of recharge cycle.

Charge Current Thermal Foldback

When the die temperature reaches 120 °C, the charging current decreases to prevent further temperature rise.

NTC Management

An NTC resistor with typical 10kΩ resistance, 1% accuracy and a beta of 3950 is recommended for LP7820B. The NTC resistor is enabled by the DISNTC bit with its default value of 0. The internal NTC detection circuitry is disabled when DISNTC bit is set to 1 to reduce the quiescent current.
Four temperature detecting thresholds are provided when charging, i.e., T_0, T_{10}, T_{15}, and T_{45}. An NTC interrupt pulse will be sent when the temperature is crossing these thresholds. The charging is terminated when the temperature range is out of T_0 - T_{45}.
The NTC [2:0] bits are used to indicate the temperature range in the Status Register 0. The MCU can change the charging parameters or disable the charging operation by using the control registers.
The NTC[2:0] will be set to 100 when DISNTC is set to 1.

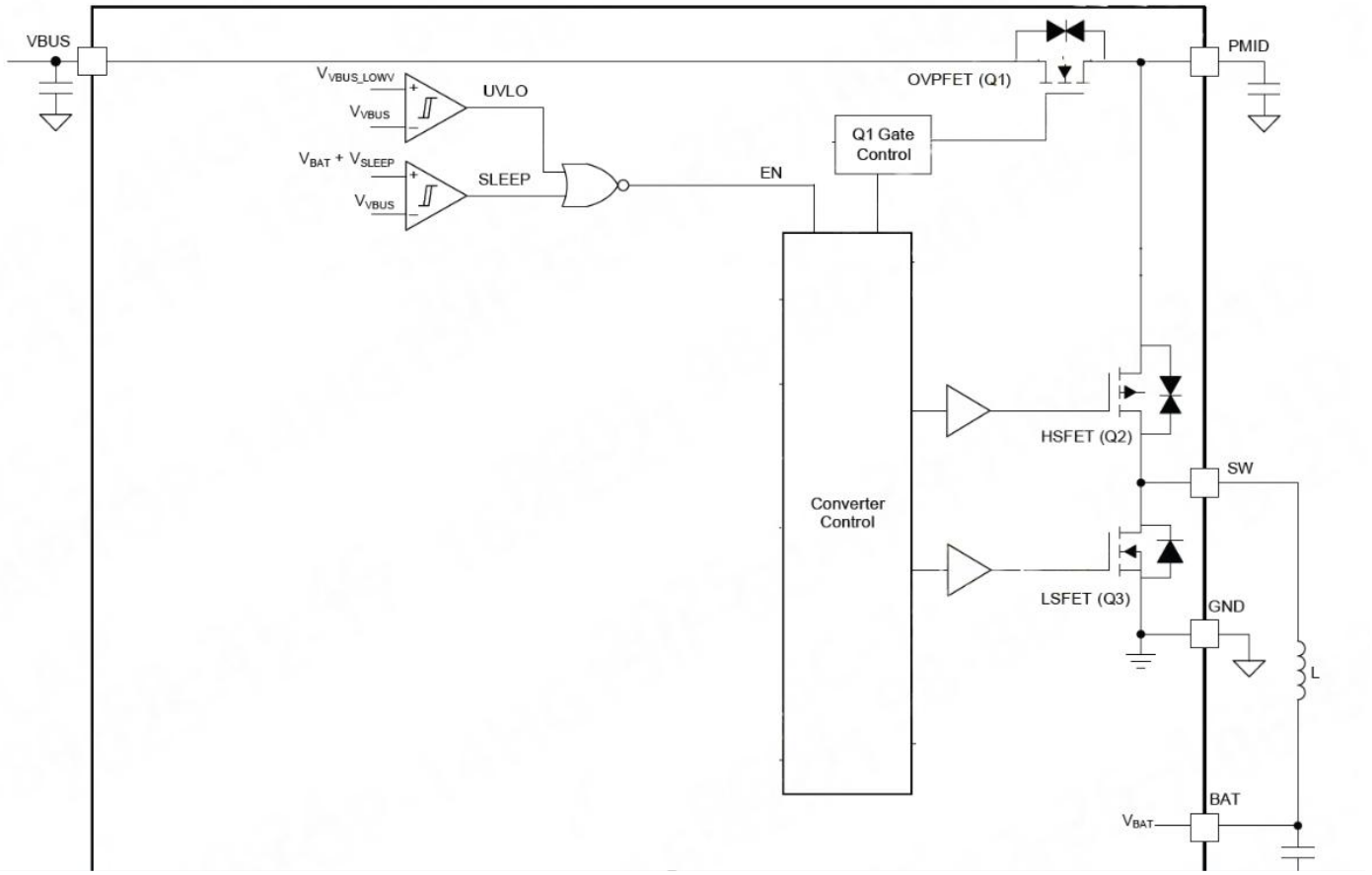
ENCHG Bit

ENCHG bit can enable the charger. When ENCHG is set to 0, the charging cycle is terminated immediately. When ENCHG is set to 1 from 0, a new charging cycle starts again. The default value of ENCHG bit is 0.

ISET Abnormal Detection

The LP7820B performs a ISET detection if a valid power source is present at VIN pin and the ENCHG is set to 1 at the same time. The charging function will not be enabled and the ISET_Abn bit is set to 1 when the ISET pin is short to ground or floating.
If the ISET short or floating when charging, the ISET_Abn bit will not be set at the register table and the charge function will not be forced off.

VSLEEP function



The primary function of VSLEEP is to enable battery charging from VBUS only when the VBUS voltage exceeds the VBAT voltage by at least 200mV. Otherwise, VBUS is prevented from charging the battery.

Power Path Management

The LP7820B integrates the power path management function. The PMID pin can be powered from the input voltage, the battery under different scenarios.

Dynamic Power Management

The voltage at the VIN pin and currents through the BUS-FET is monitored continuously when the LP7820B is powered. The minimum VIN-pin voltage is set by the DPM[1:0] bits of the Control Register 6. When the VIN-pin voltage drops (due to load switches' loading) to the voltage set by the DPM[1:0] bits , the charging current is reduced to prevent the VIN-pin voltage from dropping further. The battery will start providing current if the VIN drops to the V_{UVLO_IN} falling threshold, in which case the HS-FET and LS-FET are controlled as a boost converter.

Boost converter

When the input power is removed, the HS-FET and LS-FET are controlled as a boost converter with up to 0.6A output current capability. The quiescent current of the boost converter is only 2μA from the battery when there is no load sink by the load switches.

The boost is always-on once ENBST is set to 1 until the BAT pin voltage falls below BSTUV threshold.

Boost Converter Operation

The boost regulator has two operation modes. It operates in the voltage step-up mode when the PMID voltage is required to be higher than the battery voltage. It operates in a by-pass mode when the PMID voltage is required to be lower or equal to the battery voltage. The maximum output voltage of the boost converter is programmable by the VBST[2:0] bits of the Control Register 2. The range is between 3.6V- 5.1V with minimum 50mV/STEP.

PFM and FPWM Operation

The boost regulator improves the efficiency by reducing the switching frequency when the load decreases, this is called

the PFM mode.

The LP7820B supports another operation mode, which is FPWM by setting the FPWM register at Control Register 6. In FPWM mode, the switching frequency is kept at 1.3MHz even with no load. In this way, the output ripple is greatly reduced. The quiescent current increase 3~4mA in FPWM and the MCU can disable the FPWM when no earphone is in charge mode (both the ENVOL and ENVOL are set to 0).

Boost Under-voltage Protection

The boost converter is turned off after a typical 200-ms deglitch time when the BAT pin voltage falls below the boost under-voltage protection threshold, which is programmable by the BSTUV[1:0] bits of the Control Register 2. The range is between 3.0V- 3.5V with minimum 100mV/STEP.

The boost converter recovers to operation when the BAT pin rises 200mV above the battery under-voltage protection threshold.

Current Limit

The current flow the HS-FET of the boost regulator is limited to 2.2A when the PMID is overloaded. The current is even reduced to 0.8A when the PMID is short to ground.

ENBST Bit

The boost converter can be enabled by the ENBST bit of the Control Register 3. When ENBST is set to 0, the earphone charge is terminated immediately. The default value of ENBST bit is 0.

Earphone Control

The LP7820B offers two independent control circuits to detect the earphone insert, earphone charge, and earphone light load detection. The earphone charge circuit is achieved by two 600mΩ on-resistance power FETs to provide power for the earphones. Both the load switches are powered by the PMID and the current limit is programmable from 20mA to 250mA with minimum 5mA/step by the EICC[4:0] bits of the Control Register 1.

Earphone insert and removal

The LP7820B supports earphone insert and removal detection. Both the VOL and VOR are pulled to the PMID or BAT with a weak current source, which is programmable by the PUP[1:0] bits of the Control Register 2. The VOL and VOR are pulled at the same voltage level of PMID or BAT when there is nothing connected to the VOL and VOR. When the VOL/R pin is pulled 0.7-V lower than the maximum voltage of PMID and BAT pin because of the earphone insert, the INSL or the INSR bit is set to 1 and an interrupt is sent and the MCU can enable the load switches, i.e., the ENVOL and ENVOR bits to power the earphones.

Earphone charge

The load switches support constant current source function by configuring the EICC[4:0] bits of the Control Register 1.

When work with LP4080H or LP4081, the voltage drop between the PMID and VOL is only 200mV and the system efficiency is improved compared with the traditional 5.1V constant output at the PMID pin. This is the low-voltage dropout mode. The maximum current for the each peripheral device connected at VOL and VOR is 250mA in this mode.

Earphone voltage clamp

The LP7820B integrates two independent clamp control circuits to clamp the maximum output voltage of VOL and VOR by setting the VEAR[1:0] register at Control Register 6 to protect the bluetooth SoC.

The clamp circuit is disabled when the VEAR[1:0] is set to 00, which is the default value.

Earphone light load current detection

When the charge current at each load switch is reduced to less than the earphone light load current threshold which is set by the register EEOC[1:0] bits of the Control Register 4, the EOCL bit or EOCR bit is set to 1 and the interrupt is sent to MCU and the MCU can decide whether to cutoff the power to the earphones. When the earphone is removed from the VOL or the VOR pin, the VOL or the VOR voltage recovers to the level same as the PMID voltage, the INSL bit or the INSR is set to 0 and no interrupt is sent to the MCU this time.

Load switch SCP

The LP7820B integrates short circuit protection as well. The SCPL bit and the SCPR bit of the Status Register 1 is set to 1 and the interrupt is sent to the MCU when any one pin voltage falls below 0.7V. The MCU can take actions

accordingly. The current limit is fixed at 150mA when VOL or VOR is below 0.7V.

NTC Management

Two temperature detecting thresholds are provided when the battery is discharging, i.e., T_{-10} and T_{60}. An NTC interrupt pulse will be sent when the temperature is crossing these thresholds. The load switches are terminated when the temperature range is out of T_{-10} - T_{60} by default.
The VOL and VOR are terminated when the temperature range is out of T_0 – T_{45}. If the JEITA bit from Control Register 4 is set to 1.

Ultra-low quiescent current LDO (AVCC)

The LP7820B integrates an ultra-low quiescent current linear regulator that is powered by either the VIN or the BAT pin. This output is to power the internal MCU core, the NTC circuit, the internal logic circuit, and the communication circuit. This LDO can also be used to power peripheral devices, such as LCD panel or digital tube. A 0.1~0.47μF external ceramic capacitor is required. The LDO output voltage is programmable by the VCC[1:0] bits of the Control Register 5 from 1.8V to 3.3V.

Thermal Shutdown

When the internal junction temperature of LP7820B exceeds the thermal shutdown threshold of 150 °C, the LP7820B disables all the power paths. The LP7820B will not reset the registers and recovers to the default setting after the junction temperature falls to the 130 °C.

MCU Instruction Set and Registers

Please contact LPS sales for more information.

Application Information

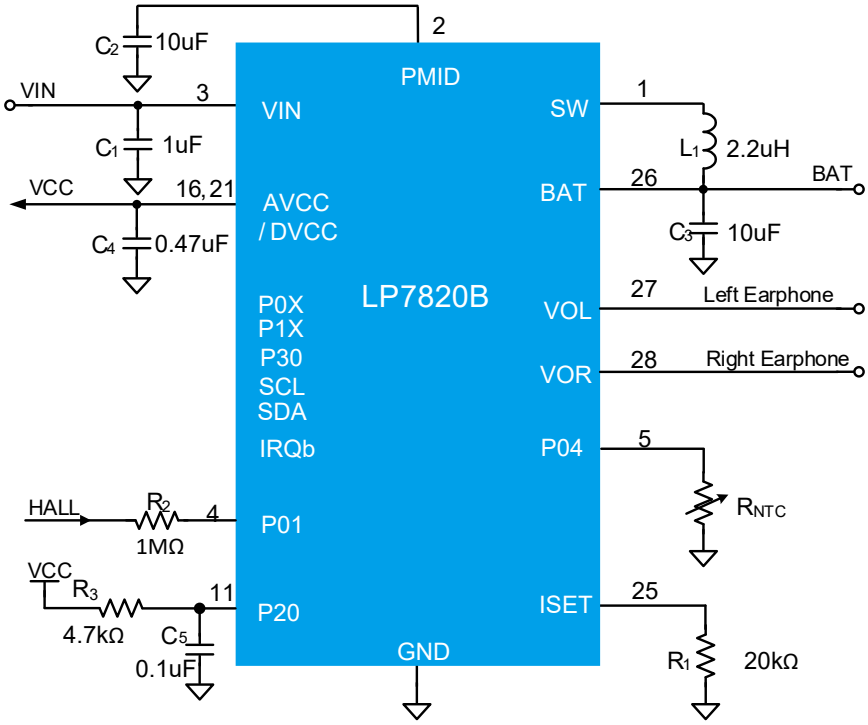


Figure 20. Typical Application Schematic

When powering up in default mode, the battery CV voltage of LP7820B is 4.2V, the termination current is 12% ICC and the trickle charge current is 10%ICC. The maximum output voltage of boost converter is 4.6V and the battery discharge undervoltage protection threshold is 3.3V. All these values can be changed by writing the registers.

Inductor and Capacitor Selection

For best input and output filtering, at least one X5R ceramic capacitor should be placed at each of the VIN, BAT and PMID pin to the GND pin. The VIN capacitor C_1 should be 25V rating with minimum 1μF capacitance. The BAT capacitor C_3 should be at least 6.3V rating with minimum 10μF capacitance. The PMID capacitor C_2 should be at least 6.3V rating with minimum 10μF capacitance. The VCC capacitor C_4 should be at least 6.3V rating with typical 0.1μF capacitance. The LP7820B is optimized to work between 1μH and 2.2μH inductance.

NTC Circuit Design

The P04 pin is used as the NTC detection. Two control methods are supported: 1) Standard JEITA temperature range control; 2) customized temperature range control by internal ADC sampling.

For the first method, as all the trigger point thresholds of the internal NTC comparators are well design with a certain type of NTC resistor, a 10-kΩ NTC resistor with 1% accuracy and with a beta of 3950 is recommended. All the trigger point thresholds can be found in the electrical characteristics table. The default NTC threshold indicates the temperature of -10℃, 0℃, 10℃, 15℃, 45℃, 60℃.

For the second method, the internal JEITA NTC detection function should be disabled by setting DIS_NTC bit to 1. The P04 can be configured as an ADC input. The ADC supports 12-bit resolution with 200ksps sample rate.

HALL Design

The P01 pin is used as the hall input detection.

KEY Design

The P00 pin is used as the KEY input detection.

PCB Layout Guidelines

Please follow the rules when designing the PCB layout.

1. The high frequency filtering capacitor C_2 should be placed with the highest priority and as close to the PMID pin and the GND pin (the GND is also the thermal PAD). 0603 size capacitors are recommended. The critical path loop circumference formed by the capacitor and the pins should less than 200 mils to minimize the parasitic inductance. (For example, the enclosed circumference via the C_2, the PMID pin and the thermal PAD should be controlled to less than 200 mils. This the most critical path, marked with yellow line.)
2. The C_1 is recommended to serve as the bulk capacitor and an 1Ω resistor is recommended to be in series with C_1 to absorb the input spike when the USB is plugged in. The C_1 should be placed to the VIN pin and the ground plane with less than 300mil loop circumference.
3. The VIN, BAT, VOL, VOR and the GND power paths should be wide and short to improve the system efficiency. As a recommendation, the trace path should be at least 40 mils to deliver 1A current with 1oz copper thickness.
4. The thermal pad which is also the power ground of the device, should be connected to the ground plane to help dissipating the power from the silicon.

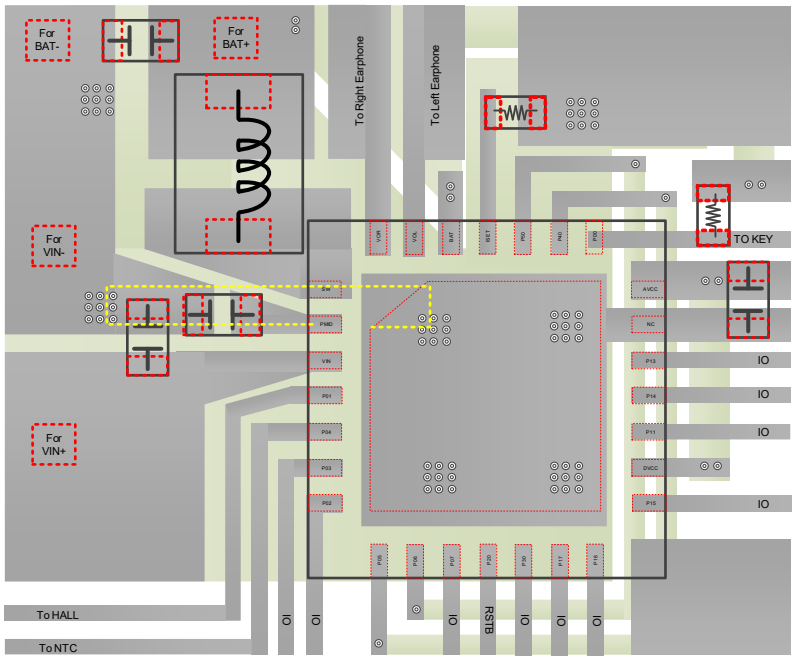
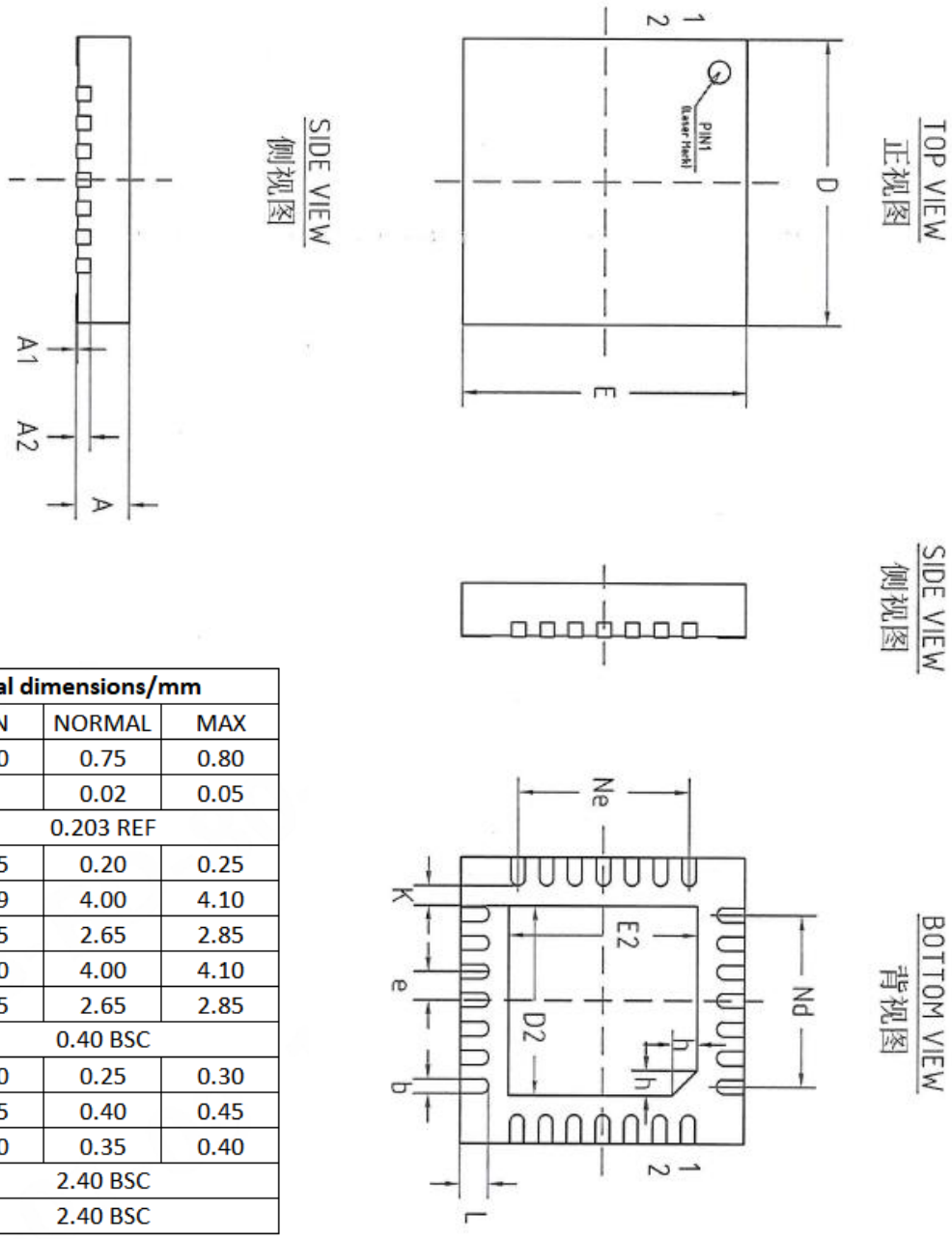


Figure 21. PCB Example (TOP View)

Packaging Information



Mechanical dimensions/mm			
SYMBOL	MIN	NORMAL	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2		0.203 REF	
b	0.15	0.20	0.25
D	0.39	4.00	4.10
D2	2.35	2.65	2.85
E	3.90	4.00	4.10
E2	2.35	2.65	2.85
e		0.40 BSC	
K	0.20	0.25	0.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
Ne		2.40 BSC	
Nd		2.40 BSC	