

### Features

- Wide input voltage range: 4V – 30V
- Output voltage range:  $V_{ref} - 13.2V$
- High efficiency operation
  - Integrated a 70-mΩ LS-MOSFET and a 105-mΩ HS-MOSFET
  - 91.5% efficiency at 2A load from 12V to 5V conversion
- Automatic PFM mode at light load
- $\pm 1\%$   $V_{ref}$  accuracy
- 500-kHz switching frequency
- COT control scheme with fast load transient response
- Hiccup protection
- Integrated UVLO, OVP, OCP, SCP, and OTP protections
- 1.6mm X 2.9mm SOT23-6 package
- RoHS Compliant and 100% Lead (Pb) Free

### Applications

- Industrial PC
- Network/digital video recorder (NVR/DVR)
- TV and TV box
- 12V and 24V Industrial bus applications

### General Description

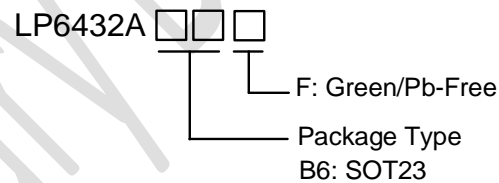
The LP6432A is a synchronous buck converter supporting up to 2A output current. The LP6432A employs an adaptive constant-on-time (COT) control scheme to achieve fast load transient response. The external components are minimized, requiring only one inductor, two resistors, and two capacitors.

The LP6432A supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

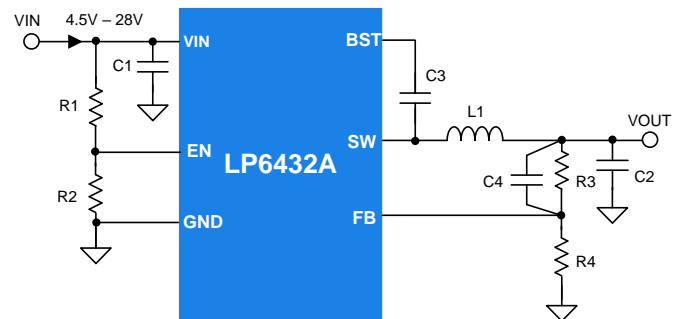
The LP6432A integrates PFM (Pulse Frequency Modulation) operation, which helps maintain the system efficiency at light load. The LP6432A also integrates multiple protection functions, i.e., over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), output over-voltage protection (OVP), and short circuit protection (SCP).

The LP6432A is available in a small 6-pin 1.6mmX2.9mm SOT23-6 package.

### Order Information



### Typical Application Circuit





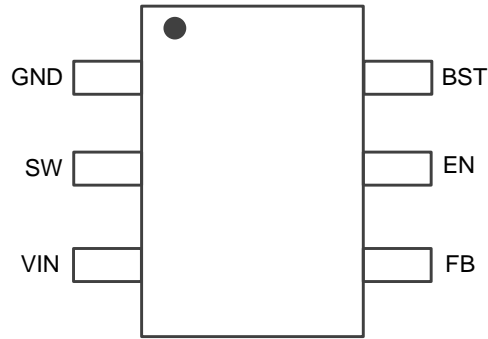
## Device Information

| Part Number   | Top Marking | Fsw    | PFM/FPWM | MSL     | Shipping |
|---|-------------|--------|----------|---------|----------|
| LP6432AB6F  |             | 500kHz | PFM      | LEVEL 3 | 3K/REEL  |
| Marking indication: Y: Year code. W: Week code. X: Batch numbers.<br>MSL: Moisture Sensitivity Level according to JEDEC Standard. |             |        |          |         |          |

LPS preliminary Datasheet



## Pin Diagram



SOT23-6  
(Top View)

LP6432A Pinout

## Pin Description

| Pin # | Name | Description   |
|-------|------|---|
| 1     | GND  | Power ground of the IC.   |
| 2     | SW   | The switching node of the converter.  |
| 3     | VIN  | IC power supply input.  |
| 4     | FB   | Feedback pin. Use a resistor divider to set the desired output voltage.   |
| 5     | EN   | Enable input. This pin can be used to control the system power sequence as well.  |
| 6     | BST  | Bootstrap pin. Power supply for high-side MOSFET gate driver. A 0.1- $\mu$ F capacitor must be connected between this pin and SW pin. |



## Absolute Maximum Ratings <sup>(Note)</sup>

|  |       |                |
|--|-------|----------------|
| VIN, SW to GND                                   | ----- | -0.3V to 32V   |
| SW to GND (5ns transient)                        | ----- | -3V to 34V     |
| EN to GND  | ----- | -0.3V to 30V   |
| FB to GND  | ----- | -0.3V to 6.5V  |
| BST to SW  | ----- | -0.3V to 5.5V  |
| BST to GND (EN=Low)                              | ----- | -0.3V to 34V   |
| BST to GND (EN=High)                             | ----- | -0.3V to 38V   |
| Junction Temperature Range (T <sub>J</sub> )     | ----- | -40°C to 150°C |
| Maximum Soldering Temperature (at leads, 10 sec) | ----- | 260°C          |

**Note:** Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ESD Ratings

|                            |       |      |
|----------------------------|-------|------|
| HBM (Human Body Model)     | ----- | 2kV  |
| CDM (Charged-device Model) | ----- | 500V |

## Thermal Information

|  |       |         |
|--|-------|---------|
| θ <sub>JA</sub> (Junction-to-Ambient Thermal Resistance) | ----- | 140°C/W |
|--|-------|---------|

## Recommended Operating Conditions

| SYMBOL           | PARAMETER  | MIN              | TYP | MAX  | UNIT |
|------------------|--|------------------|-----|------|------|
| VIN              | Input voltage                                    | 4                |     | 30   | V    |
| VOUT             | Output voltage                                   | V <sub>ref</sub> |     | 13.2 | V    |
| L                | Inductor   | 0.7              |     | 13   | μH   |
| T <sub>A</sub>   | Ambient temperature range                        | -40              |     | 85   | °C   |
| C <sub>IN</sub>  | Input decoupling capacitor, 25V rating or higher | 4.7              |     | 100  | μF   |
| C <sub>OUT</sub> | Output capacitor, 10V rating or higher           | 10               |     | 100  | μF   |



## Electrical Characteristics

(The specifications are measured under conditions  $V_{IN} = 12V$ ,  $T_A = 25^\circ C$ , unless otherwise specified.)

| SYMBOL           | PARAMETER                             | TEST CONDITIONS                       | MIN   | TYP  | MAX   | UNIT       |
|------------------|---------------------------------------|---------------------------------------|-------|------|-------|------------|
| INPUT SECTION    |                                       |                                       |       |      |       |            |
| $V_{ULVO\_R}$    | Input voltage under lockout threshold | $V_{IN}$ rising threshold             |       | 3.65 | 3.8   | V          |
| $V_{ULVO\_H}$    | UVLO hysteresis                       | $V_{IN}$ falling threshold            |       | 0.15 |       | V          |
| $I_{q\_VIN}$     | Input quiescent current               | No switching, $EN=3V$ , $FB=1.0V$     |       | 400  |       | $\mu A$    |
| $I_{SD}$         | Shutdown current                      | $EN=0V$ , $V_{IN} = 12V$              |       | 1.5  |       | $\mu A$    |
| BUCK CONVERTER   |                                       |                                       |       |      |       |            |
| $I_{LIM}$        | Low-side valley current limit         | $T_A=25^\circ C$                      | 2.0   | 3.0  | 4.0   | A          |
| $V_{ref}$        | Reference voltage                     | $T_A=25^\circ C$ ,                    | 0.594 | 0.6  | 0.606 | V          |
| $R_{dson\_HS}$   | High-side FET on resistance           | $V_{IN}=12V$                          |       | 105  |       | m $\Omega$ |
| $R_{dson\_LS}$   | Low-side FET on resistance            | $V_{IN}=12V$                          |       | 70   |       | m $\Omega$ |
| $f_{sw}$         | Switching frequency                   |                                       |       | 500  |       | kHz        |
| $t_{on-min}$     | Minimum on-time <sup>[1]</sup>        |                                       |       | 50   |       | ns         |
| $t_{off-min}$    | Minimum off-time <sup>[1]</sup>       | $V_{FB}=V_{ref}-0.2V$                 |       | 100  |       | ns         |
| $t_{on-hiccup}$  | Hiccup on time <sup>[1]</sup>         |                                       |       | 2    |       | ms         |
| $t_{off-hiccup}$ | Hiccup waiting time <sup>[1]</sup>    |                                       |       | 10   |       | ms         |
| $t_d$            | EN delay time <sup>[1]</sup>          | From EN high to first switching       |       | 150  |       | $\mu s$    |
| $t_{ss}$         | Soft-start time <sup>[1]</sup>        | From first switching to 95% $V_{ref}$ |       | 1    |       | ms         |
| $T_{jSD}$        | Thermal shutdown threshold            | Rising threshold                      |       | 155  |       | $^\circ C$ |
|                  | Thermal shutdown threshold            | Falling threshold                     |       | 135  |       | $^\circ C$ |
| $I_{leak\_FB}$   | FB pin leakage current                |                                       |       | 0.01 |       | $\mu A$    |



| SYMBOL          | PARAMETER                            | TEST CONDITIONS                      | MIN  | TYP  | MAX  | UNIT       |
|-----------------|--------------------------------------|--------------------------------------|------|------|------|------------|
| EN Logic        |                                      |                                      |      |      |      |            |
| $V_H$           | EN pin logic high threshold          | EN Rising threshold                  | 1.14 | 1.2  | 1.26 | V          |
| $V_{hys}$       | EN pin threshold hysteresis          |                                      |      | 0.2  |      | V          |
|                 | EN pin internal pull-down resistance |                                      |      | 1000 |      | k $\Omega$ |
| Output OVP      |                                      |                                      |      |      |      |            |
| $V_{OVP\_rise}$ | OVP threshold                        | VOUT rising edge, reference to Vref  | 108  | 110  | 112  | %          |
| $V_{OVP\_fall}$ | OVP hysteresis                       | VOUT falling edge, reference to Vref |      | 105  |      | %          |

[1]: Not production tested. Guaranteed by design.



## Typical Characteristics

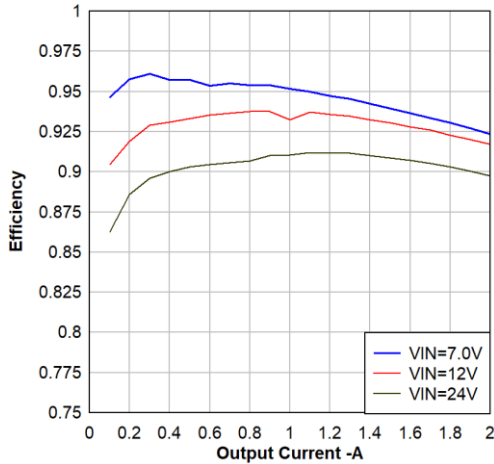


Figure 1.  $V_{OUT}=5.0V$ , Efficiency,  $L=4.7-\mu H$ , LP6432A

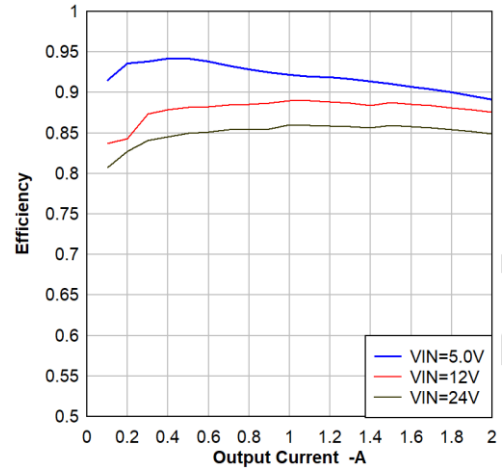


Figure 2.  $V_{OUT}=3.3V$ , Efficiency,  $L=4.7-\mu H$ , LP6432A

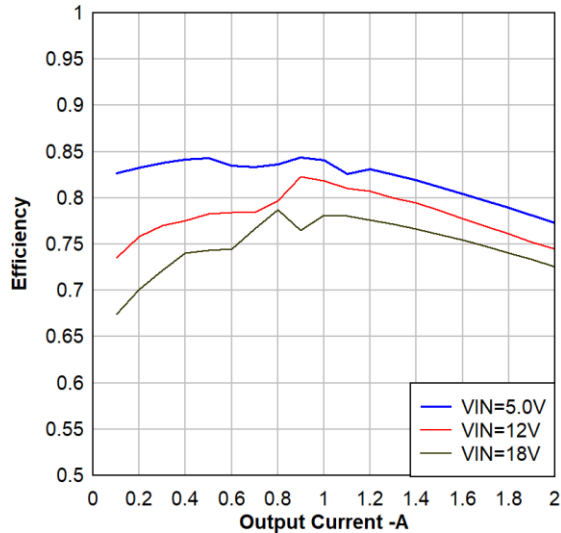


Figure 3.  $V_{OUT}=1.2V$ , Efficiency,  $L=2.2-\mu H$ , LP6432A

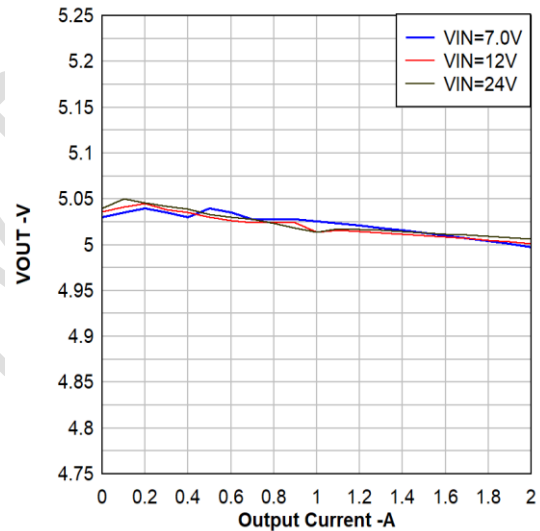


Figure 4.  $V_{OUT}=5V$ , Regulation,  $L=4.7-\mu H$ , LP6432A

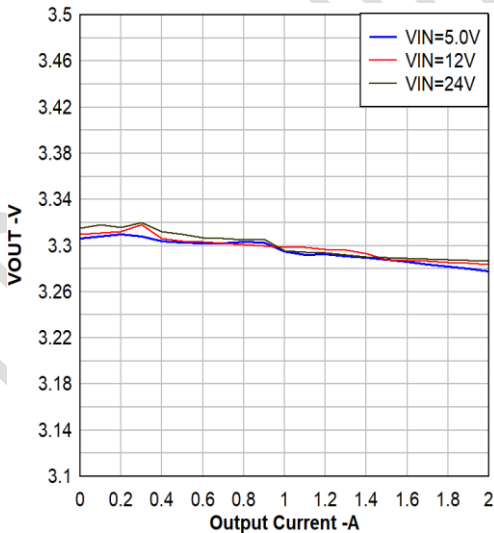


Figure 5.  $V_{OUT}=3.3V$ , Regulation,  $L=4.7-\mu H$ , LP6432A

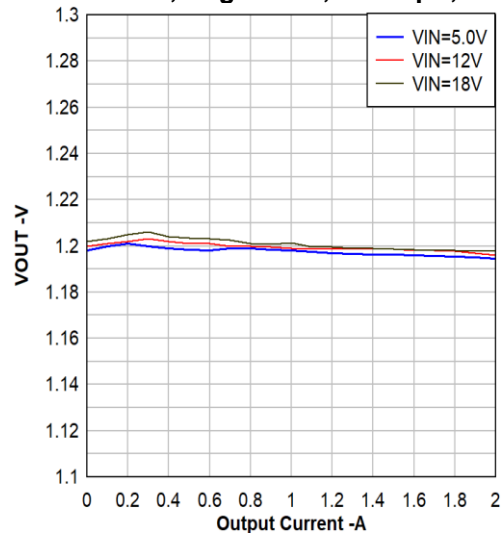


Figure 6.  $V_{OUT}=1.2V$ , Regulation,  $L=2.2-\mu H$ , LP6432A



## Application Waveforms

(Test condition: Vin=12V, Vout=5V, L=4.7μH, Cout=22μF\*2)

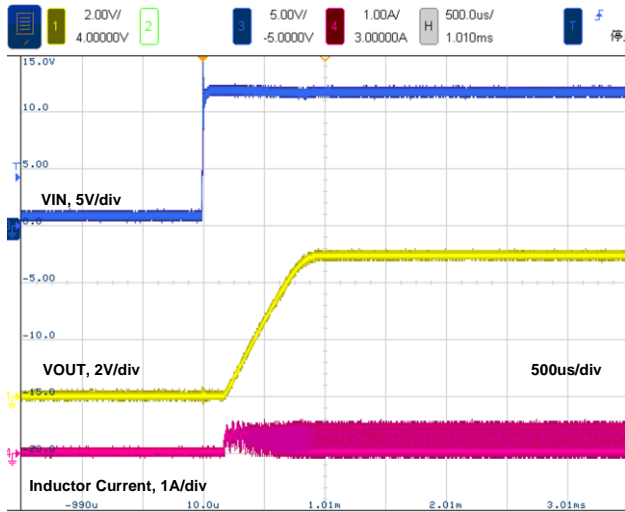


Figure 7. Startup by VIN, 50Ω load

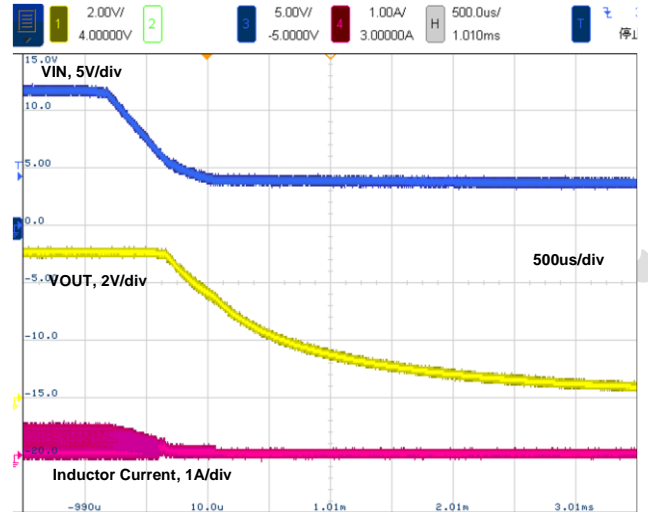


Figure 8. Shutdown by VIN, 50Ω load

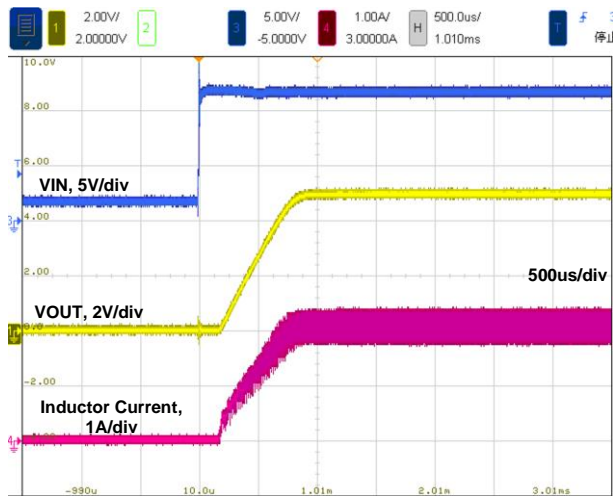


Figure 9. Startup by VIN, 2.5Ω load

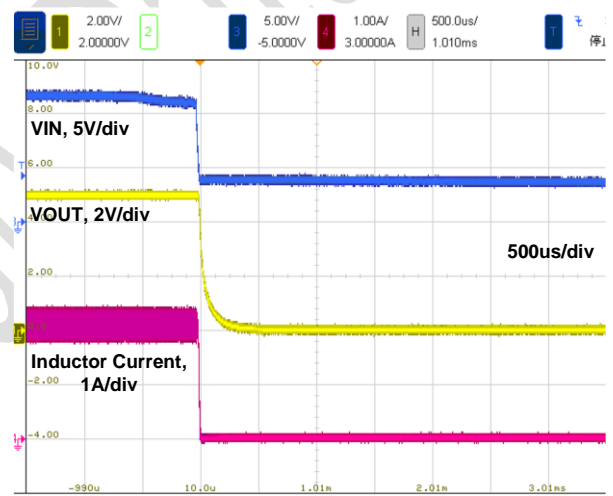


Figure 10. Shutdown by VIN, 2.5Ω load

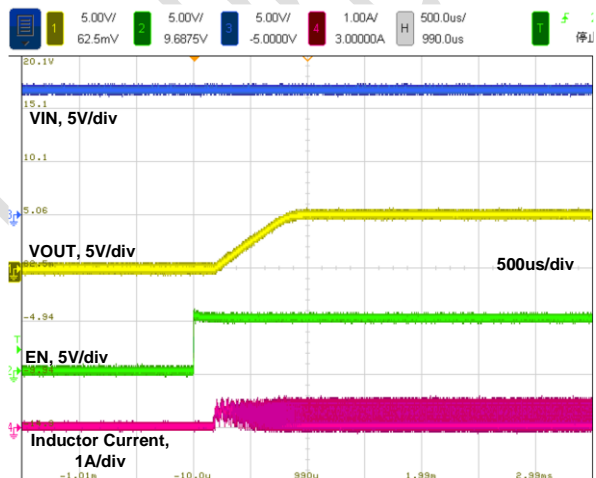


Figure 11. Startup by EN, 50Ω load

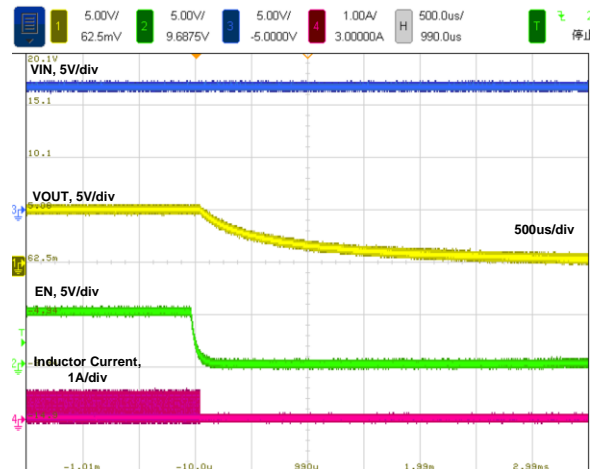


Figure 12. Shutdown by EN, 50Ω load

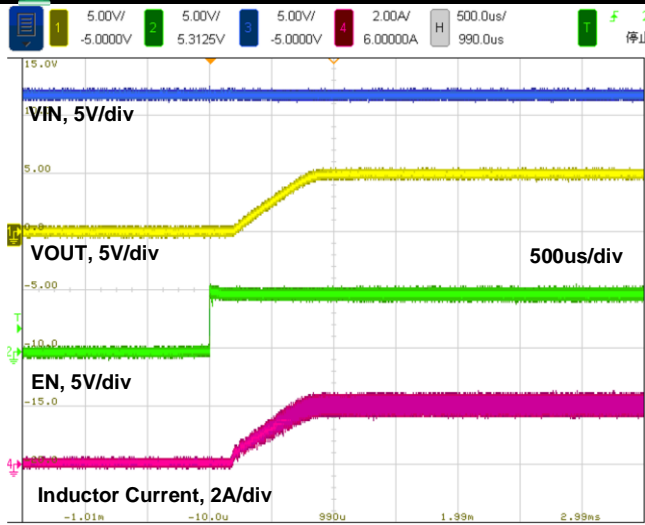


Figure 13. Startup by EN, 2.5Ω load

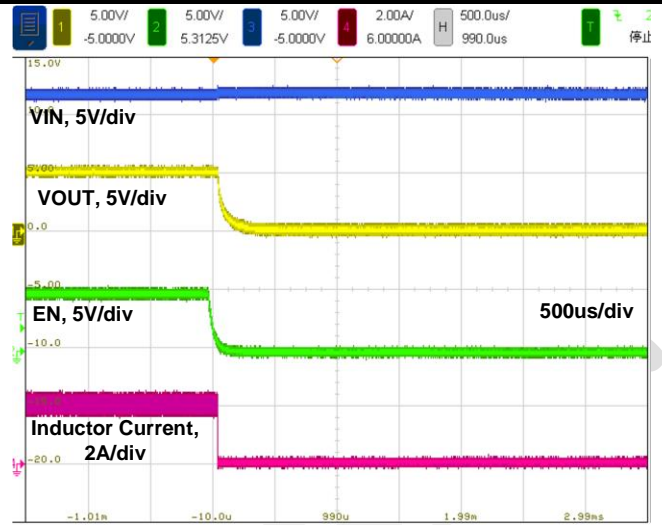


Figure 14. Shutdown by EN, 2.5Ω load

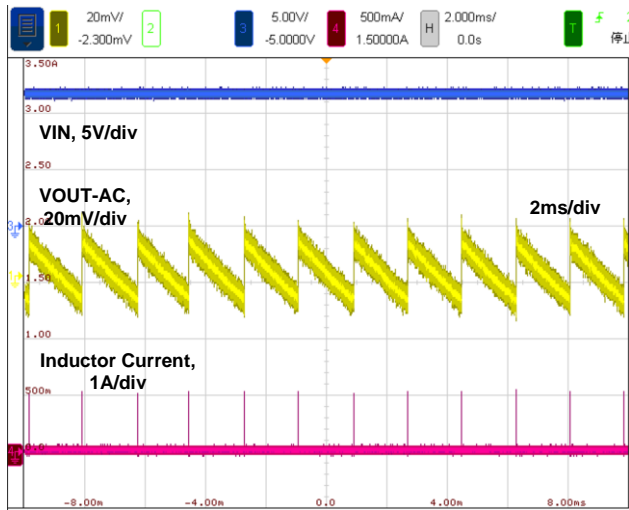


Figure 15. Switching Waveform, 0A load

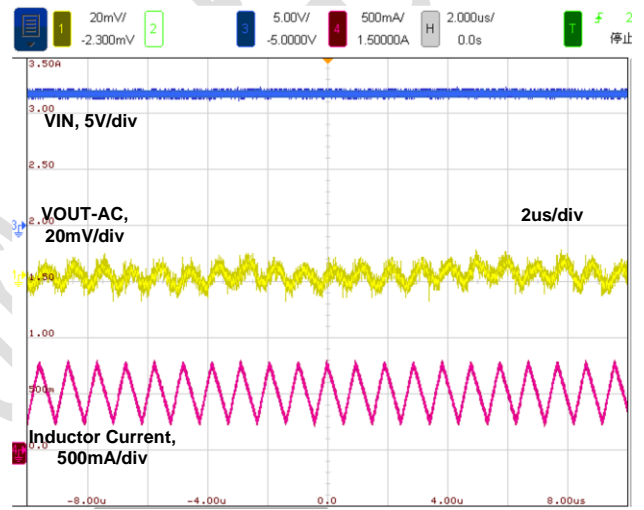


Figure 16. Switching Waveform, 500mA load

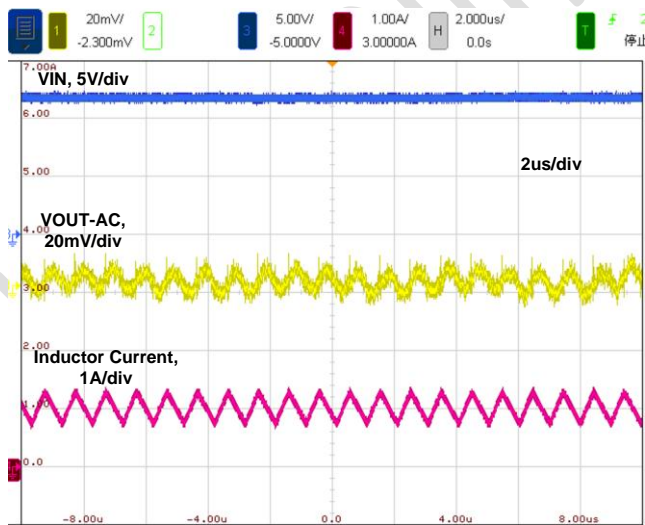


Figure 17. Switching Waveform, 1A load

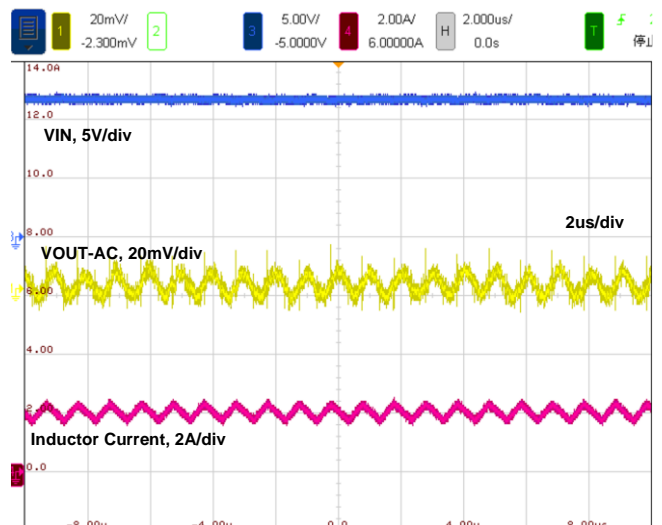


Figure 18. Switching Waveform, 2A load

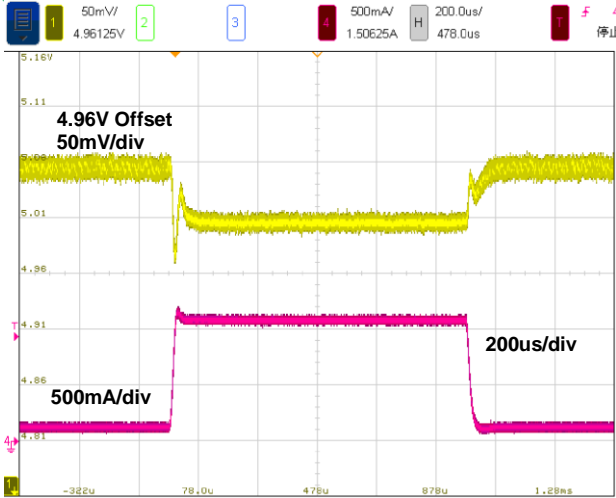


Figure 19. Load Transient, 0.1A-1A-0.1A

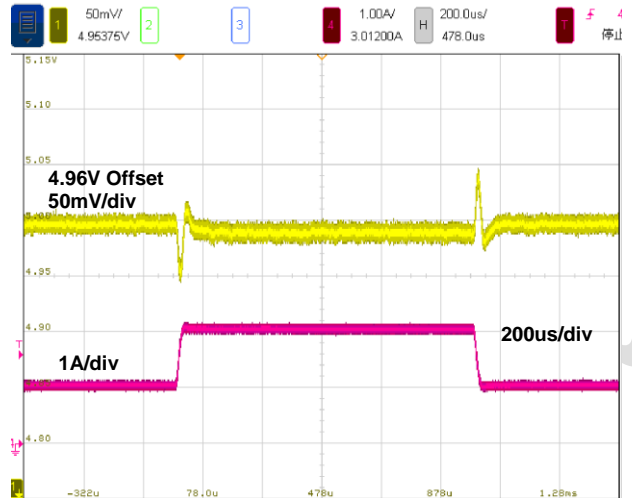


Figure 20. Load Transient, 1A-2A-1A

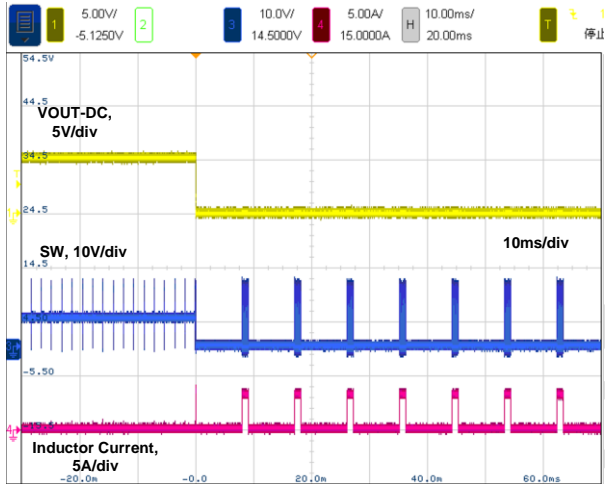


Figure 21. SCP Happen, Hiccup Operation

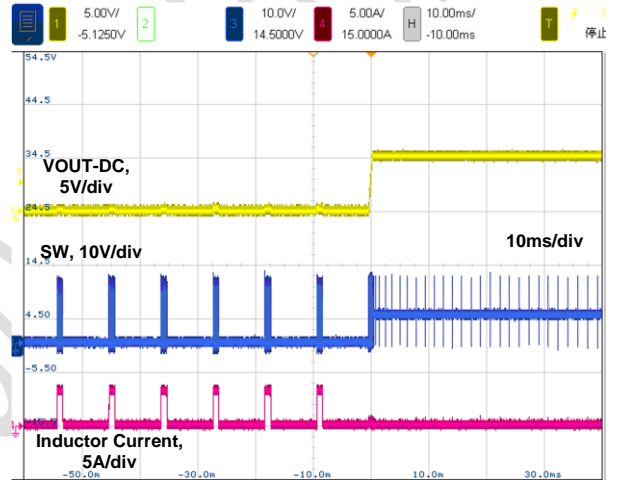
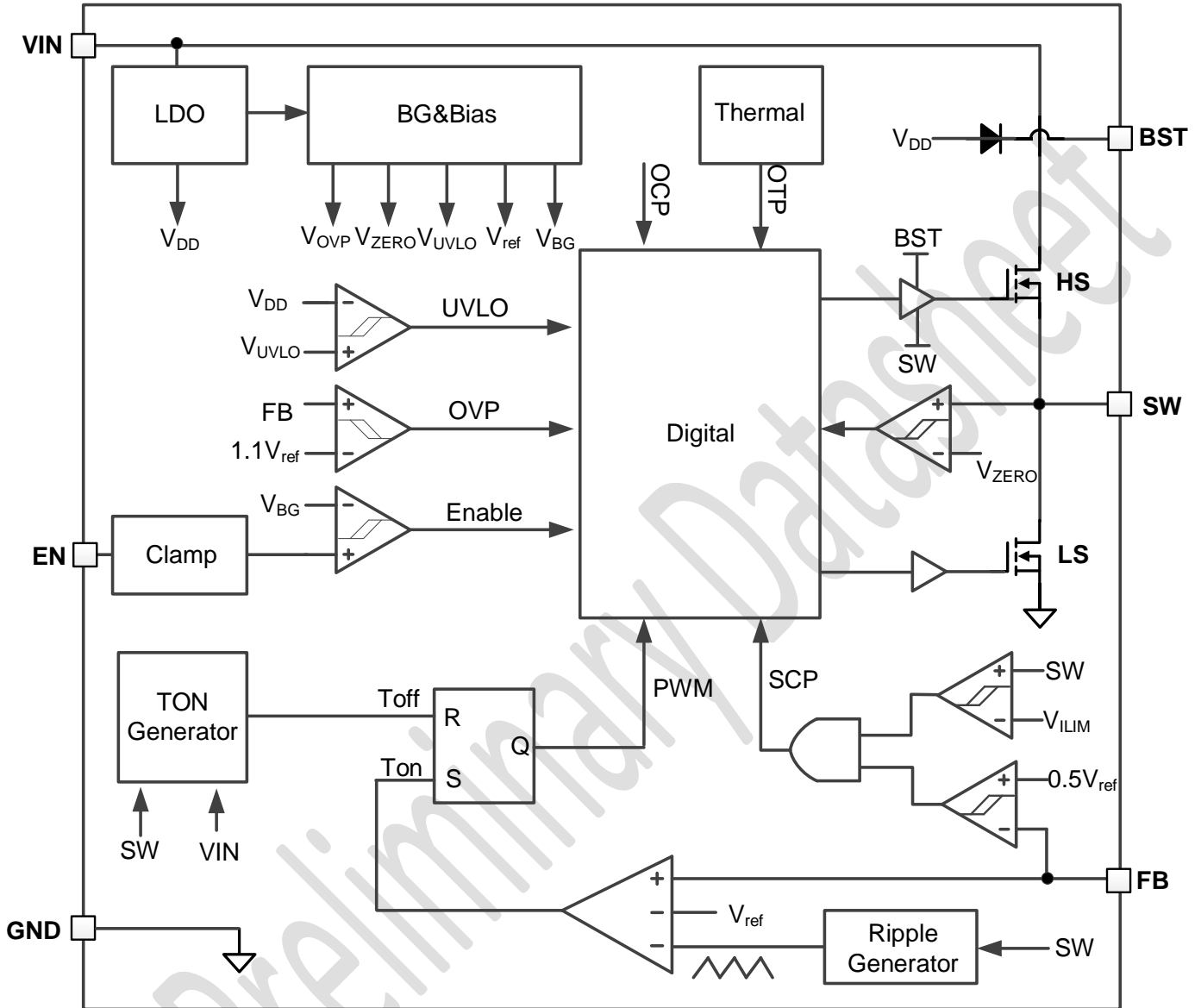


Figure 22. SCP Recovery



## Functional Block Diagram





## Detailed Description

### Overview

The LP6432A is a 2A synchronous buck converter, supporting 4 - 30V input operating voltage range and withstand 36V input voltage. The adaptive COT control scheme enables fast transient respond and minimizes the output capacitance. The LP6432A supports both aluminum polymer capacitors and low-ESR ceramic capacitors without external compensation circuit. The LP6432A automatically transfers between PFM and PWM according to the output current while LP6432AF works in force PWM mode to minimize the output ripple over all the load range.

### Under Voltage Lockout (UVLO)

When the input voltage  $V_{IN}$  is lower than the UVLO threshold, all functions are shut down. When the input voltage is higher than the UVLO rising threshold, the LP6432A can be enabled by the EN pin.

### EN Control

The EN pin can be used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the  $V_{IN}$  is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.2V typically), the LP6432A enables all the internal circuits, delays for 260us, and begins the soft-start (refer to Soft-start section for more details).

The EN pin has an internal 1000k $\Omega$  pull-down resistor to ground.

### Soft-start

The LP6432A integrates soft-start function with a typical time of 600us ( $t_{ss}$ ). After passing the UVLO threshold and enabled by the EN pin with the 250us delay( $t_d$ ), the internal reference voltage ramps from zero to the  $V_{ref}$  in 600us and the output voltage ramps up accordingly.

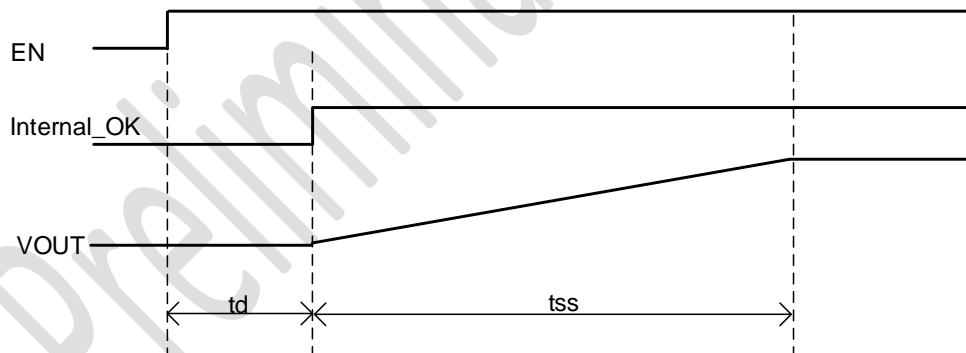


Figure 21. Soft Start Sequence

### Constant-ON Time (COT) Control Scheme

The LP6432A integrates the COT control scheme for pseudo-fixed- frequency operation when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal on-time ( $T_{ON}$ ) generator block monitors the FB-pin voltage and turns on the high-side MOSFET to start a switching cycle, when the FB-pin voltage drops to an internal reference voltage  $V_{ref}$ . Then the internal circuits start to calculate the on-time of the high-side MOSFET, which is proportional to the input voltage and inversely proportional to the output voltage. Once the on-time is finished, the TOFF generator turns off the high-side MOSFET and turns on the low-side MOSFET.

### PFM Operation



The LP6432A is designed to maintain high efficiency at light load by adopting pulse-frequency modulation (PFM). In the PFM, the switching cycle is still initiated by the TON generator monitoring the FB-pin voltage. The high-side MOSFET is turned on for TON time and then turned off, followed by turning on the low-side MOSFET. The inductor current falls when the low-side MOSFET is on. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remain off until a new switching cycle begins, determined by TON generator. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

## Bootstrap Capacitor

The LP6432A integrates two N-MOSFET to achieve high efficiency. The high-side MOSFET is powered by the bootstrap capacitor  $C_{BST}$ , which is between the BST pin and SW pin. A  $1\Omega\sim 100\Omega$  resistor is recommended in series with the bootstrap capacitor  $C_{BST}$  to reduce the switching noise and improve the system reliability.

## Over Current Protection and Short Circuit Protection

The LP6432A protects an over current situation by limiting the inductor valley current. The current of low-side MOSFET is monitored all the time to sense the inductor valley current when the LP6432A is enabled. The high-side MOSFET cannot be turned on if the valley current is higher than the low-side valley current limit, protecting the inductor current from further increasing. The inductor current is limited to the valley current limit plus a half of the inductor ripple current.

The SCP is realized by monitoring the FB-pin voltage when the inductor current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the FB voltage drops to 50% of the  $V_{ref}$  for 1-ms, the LP6432A shuts down. The LP6432A will restart after a typical 10-ms hiccup waiting time. If the SCP condition still holds after soft-start, the LP6432A shuts down again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

## Output Over-voltage Protection

The LP6432A stops switching immediately when the FB voltage rising above  $110\%V_{ref}$  to protect the output capacitor voltage from further increasing. The LP6432A recovers switching when the FB voltage falls below  $105\%V_{ref}$ .

## Thermal Protection

The LP6432A has a thermal protection function. The device will shut down when the internal temperature is higher than  $155^{\circ}\text{C}$  and will restart after the temperature drops below  $135^{\circ}\text{C}$ .



## Application Information

### Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider  $R_{UP}$  and  $R_{DOWN}$  according to the equation below:

$$V_{OUT} = \left( \frac{R_{UP}}{R_{DOWN}} + 1 \right) * V_{ref}$$

When the output voltage is in regulation, the typical voltage at FB pin is 0.6V.

For better accuracy, the  $R_{DOWN}$  is recommended to be lower than 100kΩ to ensure the current flowing through  $R_{DOWN}$  is at least 100 times larger than the FB pin leakage current.

For a 5.0V-output application, a 10kΩ  $R_{DOWN}$  is selected and the  $R_{UP}$  is 73kΩ.

A resistor with higher than 1kΩ but lower than 100kΩ should be placed between the resistor divider and FB pin if a  $C_{ff}$  capacitor is soldered to reduce the switching noise influence.

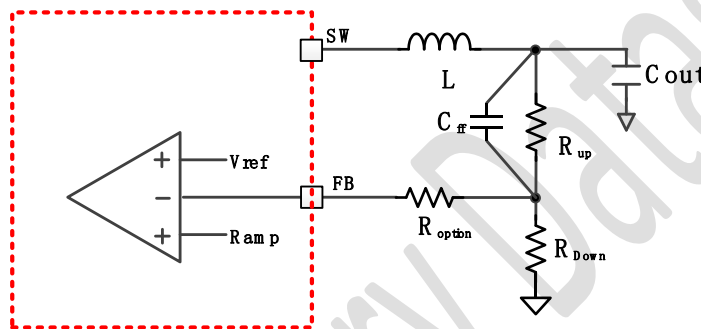


Figure 22. FB connection

### EN Design

The LP6432AX allows the user to design a precise  $V_{IN}$  voltage to enable the converter during power on. The startup sequence can be designed by adjusting the resistor divider of  $R_{UP\_EN}$  and  $R_{DOWN\_EN}$  with the equation below,

$$V_{EN} = \frac{1000k\Omega / R_{DOWN\_EN}}{R_{UP\_EN} + 1000k\Omega / R_{DOWN\_EN}} * V_{IN}$$

where  $V_{EN}$  is the EN rising threshold voltage at which the converter is enabled, which is 1.2V typically. A 47pF-1nF capacitor is recommend to be soldered in parallel with the  $R_{EN\_DOWN}$  to avoid the high-frequency noise influence from the switching node.

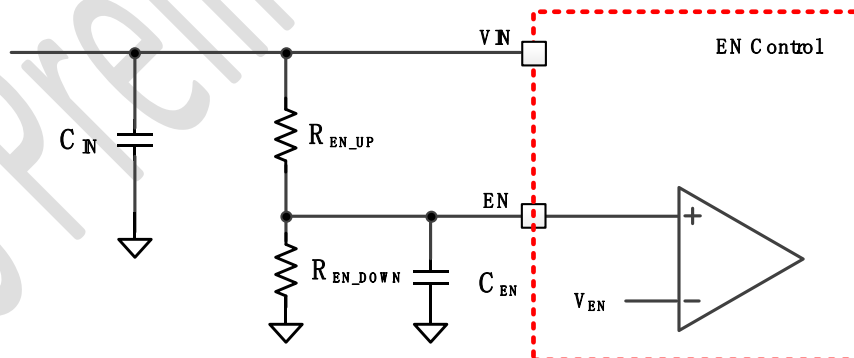


Figure 23. EN connection

### Inductor and Output Capacitor Setting

The inductor ripple is calculated by the equation below:

$$I_{PP} = \left( \frac{V_{OUT}}{L * F_{SW}} * \frac{V_{IN} - V_{OUT}}{V_{IN}} \right)$$



To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.

For a typical 12V input voltage and 5V output voltage, a low DCR value, 2.2- $\mu$ H or 4.7- $\mu$ H inductor is recommended. The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor  $C_{FF}$  can be selected to improve the transient behavior. The typical capacitance can be 10-100pF. For this design, 10V, X5R, 22  $\mu$ F capacitors (GRM21BR61A226ME51) from Murata are soldered at the VOUT to GND. Multiple capacitors should be soldered to keep the system stable because of the voltage rating effect.

**Table 1. Recommend R/L/C values (500kHz)**

| Vout | Inductor-L              | Cout         | R <sub>UP</sub> | R <sub>DOWN</sub> | R <sub>option</sub> | C <sub>ff</sub> |
|------|-------------------------|--------------|-----------------|-------------------|---------------------|-----------------|
| 1.2V | 1.5 $\mu$ H/3.3 $\mu$ H | 22 $\mu$ F*1 | 10 k $\Omega$   | 10 k $\Omega$     | 0-10 k $\Omega$     | NA              |
| 3.3V | 2.2 $\mu$ H~6.8 $\mu$ H | 22 $\mu$ F*2 | 45 k $\Omega$   | 10 k $\Omega$     | 0-10 k $\Omega$     | 22-100pF        |
| 5.0V | 4.7 $\mu$ H ~10 $\mu$ H | 22 $\mu$ F*2 | 73 k $\Omega$   | 10 k $\Omega$     | 0-10 k $\Omega$     | 47-100pF        |



## Bootstrap capacitor

Bootstrap capacitor is critical to drive the high-side MOSFET. A 0.1- $\mu\text{F}$  ceramic capacitor is needed to supply power for the high-side driver. The capacitor should be at least 10V. The resistor  $R_1$  is used to adjust the driver speed to optimize the EMI performance and reliability.

## Input capacitor

A typical 22- $\mu\text{F}$  ceramic capacitor is needed to serve as the bulk capacitor at the VIN pin. An additional 0.1- $\mu\text{F}$  is strongly recommended to provide additional high frequency filtering and should be placed to the VIN pin and GND as close as possible.

## PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place the input capacitors ( $C_2$  and  $C_4$ , 0603 or 0402 size) as close as possible to VIN pin and GND pin and use shortest copper trace connection or GND plane, this is the most critical path and should have the highest priority when designing PCB floorplan. To minimize the switching noise, the SW pin is recommended to layout at the bottom layer by vias.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- $R_1$  is reserved to slow down the switching speed for noise sensitive applications and  $R_3$  with higher than 1k $\Omega$  resistor should be soldered if the feedforward capacitor is soldered at the same time.

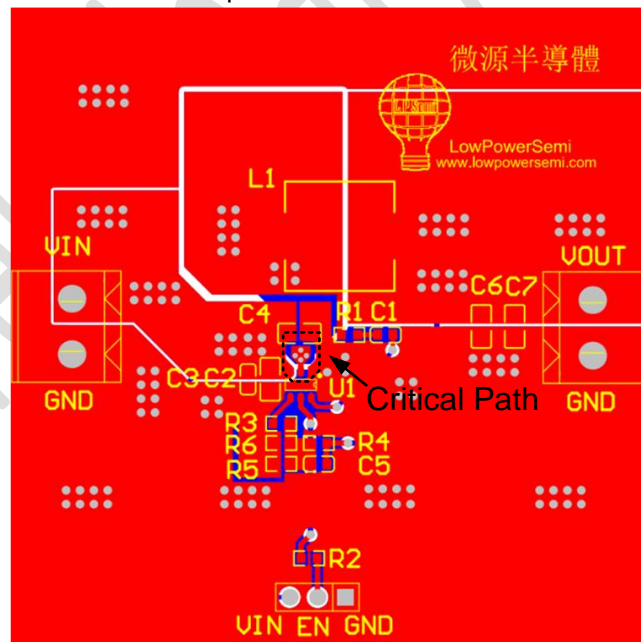
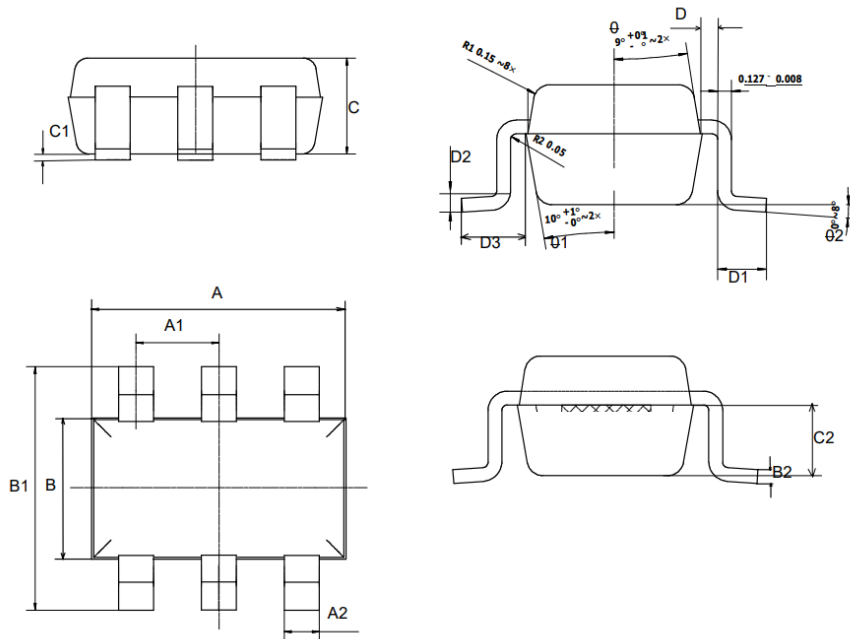


Figure 24. Layout example



## Packaging Information



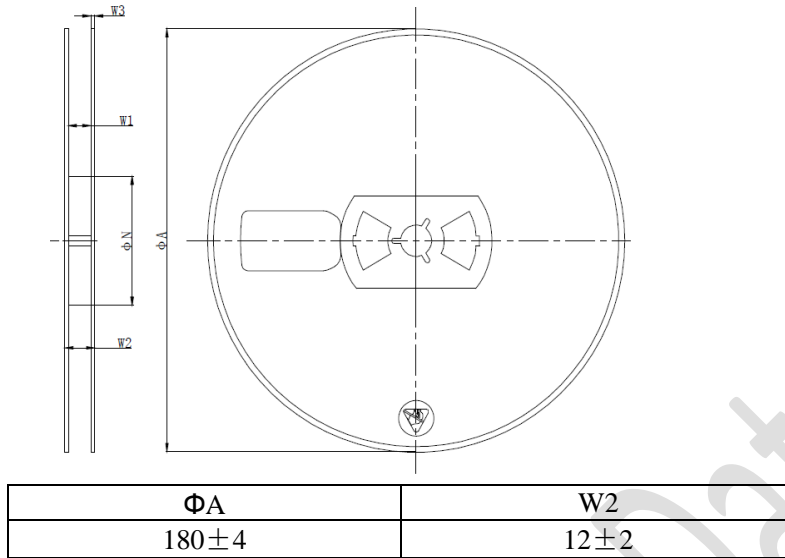
| COMMON DIMENSIONS<br>UNITS MEASURE=MILLIMETER |         |       |       |
|---|---------|-------|-------|
| SYMBOL  | MIN     | MID   | MAX   |
| A   | 2.82    | 2.92  | 3.02  |
| A1  | 0.90    | 0.95  | 1.0   |
| A2  | 0.30    | 0.35  | 0.40  |
| B   | 1.52    | 1.62  | 1.72  |
| B1  | 2.80    | 2.90  | 3.0   |
| B2  | 0.12    | 0.128 | 0.135 |
| C   | 1.05    | 1.10  | 1.15  |
| C1  | 0.03    | 0.08  | 0.13  |
| C2  | 0.6     | 0.65  | 0.7   |
| D   | 0.03    | 0.08  | 0.13  |
| D1  | 0.4     | 0.45  | 0.5   |
| D2  | 0.25TYP |       |       |
| D3  | 0.6     | 0.65  | 0.7   |

1.6x2.9 SOT23-6 package

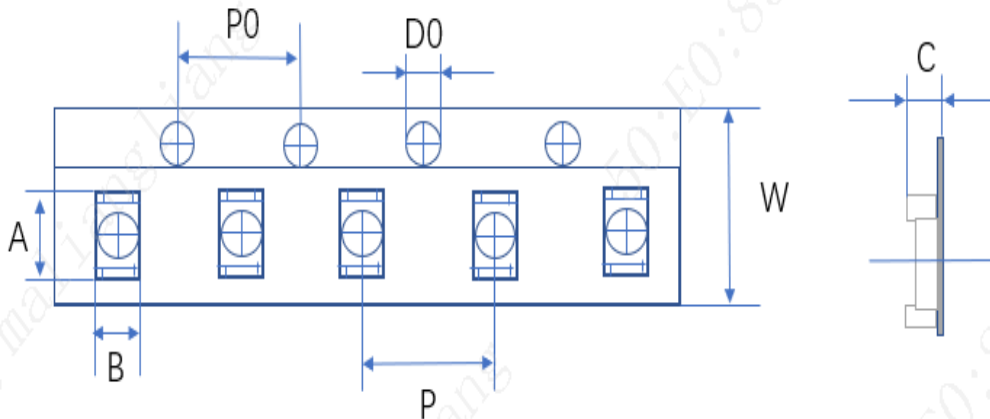


## Tape and Reel Information

### REEL DIMENSIONS (Unit:mm)



### TAPE DIMENSIONS (Unit:mm)



| 口袋宽度A  |      | 口袋长度B  |      | 编带孔中心间距P0 |      | IC中心间距P |      | 孔径D0   |       | 编带宽度W  |      | 编带厚度C  |      |
|--------|------|--------|------|-----------|------|---------|------|--------|-------|--------|------|--------|------|
| 尺寸(mm) | 公差   | 尺寸(mm) | 公差   | 尺寸(mm)    | 公差   | 尺寸(mm)  | 公差   | 尺寸(mm) | 公差    | 尺寸(mm) | 公差   | 尺寸(mm) | 公差   |
| 3.2    | ±0.2 | 3.26   | ±0.2 | 4         | ±0.1 | 4       | ±0.1 | 1.5    | ±0.15 | 8      | ±0.3 | 1.4    | ±0.2 |

### PIN1 AND TAPE FEEDING DIRECTION

