Features

- **Input Supply Voltage Range**
  - 2.8V to 14.0V input supply
- **Current-mode boost regulator**
  - 1.2MHz switching frequency
  - Integrated 24V/3.5A 130mΩ NMOSFET
  - Fast transient response to pulsed load
  - High efficiency up to 90%
  - Adjustable high-accuracy output voltage(±2%)
  - Over current protection
  - Over voltage protection
- **VGH positive charge pump controller**
- **VGL negative charge pump controller**
- **Integrated high performance operational amplifier**
  - ±150mA output short-circuit current
  - Adjustable delay time fixed 180ms
  - 25V/us fast slew rate
  - 10MHz bandwidth
- **Low-voltage detection circuit**
- **VGH Delay controller**
  - Adjustable delay time
- **Over Temperature Protection**
- **RoHS Compliant and 100% Lead(Pb)-Free**
- **Compact Package: QFN4×4-24**

Applications

- TFT LCD for Notebooks
- TFT LCD for Monitors
- TFT LCD for TV

Order Information

LP6286H □□□-□

- F: Spread Spectrum
- F: Green
- Package Type
  QV: QFN4X4-24

General Description

The LP6286HQVF-F is an integrated power supply solution optimized for small to medium size thinfilm transistor (TFT) liquid crystal displays (LCD's).

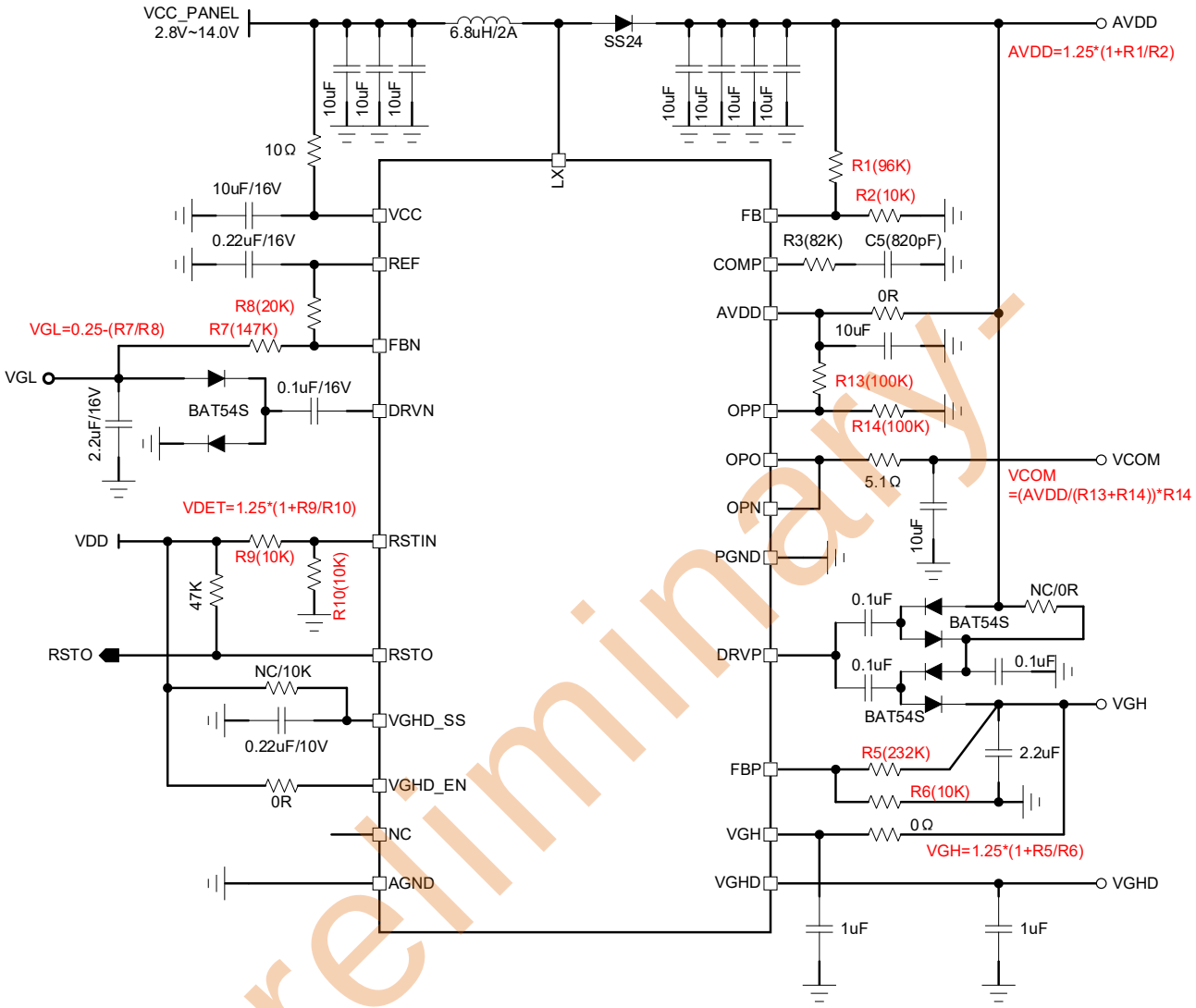
The boost converter operates at the frequency of 1.2MHz. The integrated N-channel FET has a typical current limit of 3.5A and can support output voltages up to 18V.

The gate-on and gate-off charge pumps provide regulated TFT-LCD gate-on and gate-off supplies. Both outputs can be adjusted by external resistive voltage-dividers.

The integrated operational amplifier is typically used for LCD VCOM driving; the output can sink or source up to 150mA short-circuit current. This operational amplifier features fast slew rate (25V/us), wide bandwidth (20MHz).

A built-in voltage detector generates a reset signal when the input voltage drops below a specified level. The reset signal is active low, and the detecting level is decided by an external resistor divider.

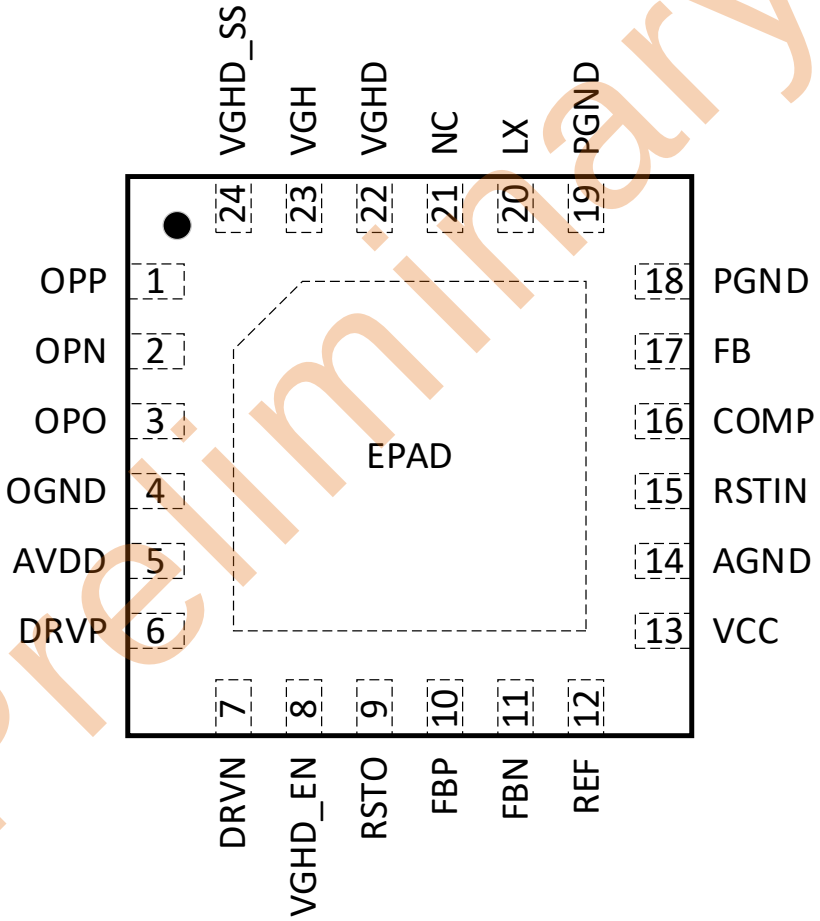
Typical Application Circuit



Device Information1

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LP6286HQVF-F	LPS LP6286 HYWX	MSL3	QFN4X4-24	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



LP6286HQVF-F QFN4X4-24

Note: Recommend connecting the Thermal Pad to the Ground for excellent power dissipation.

Pin Description

Pin#	Name	Description
1	OPP	Operational amplifier positive input.
2	OPN	Operational amplifier negative input.
3	OPO	Operational amplifier output.
4	OGND	Ground for operational amplifier and charge pumps.
5	AVDD	Charge pump supply and operational amplifier supply.
6	DRVP	Positive charge pump driving output.
7	DRVN	Negative charge pump driving output.
8	VGHD_EN	Control pin for VGHD Enable.
9	RSTO	Voltage detector output for reset, active low. RSTO is an open-drain output.
10	FBP	Positive charge pump feedback sense input.
11	FBN	Negative charge pump feedback sense input.
12	REF	Reference output. All power outputs are disabled until REFexceeds its UVLO threshold.
13	VCC	Supply for PWM, reference and other circuits.
14	AGND	Analog ground.
15	RSTIN	Voltage detector divider input.
16	COMP	Boost converter error amplifier compensation node.
17	FB	Boost converter feedback voltage sense input.
18	PGND	Boost converter power ground (source of the internal NMOS switch).
19	PGND	Boost converter power ground (source of the internal NMOS switch).
20	LX	Boost converter switching node (drain of the internal NMOS switch).
21	NC	NC
22	VGHD	Supply voltage for gate driver.
23	VGH	Input to VGHD.
24	VGHD_SS	Function1: VGHD startup delay input; charged with a constant 5uA current. Function2: VGHD_SS is high level before the AVDD was turned on, VCOM delay 180ms turn on.
25	EPAD	Thermal Pad, connect to AGND

Absolute Maximum Ratings (Note1)

VCC to AGND ---------- -0.3V to +16.5V
LX to GND ---------- -0.3V to +22V
AVDD to GND ---------- -0.3V to +20V
OPP, OPN, OPO to OGND ---------- -0.3V to AVDD+0.3V
DRVP, DRVN to GND ---------- -0.3V to AVDD+0.3V
VGHD_EN,RST to AGND ---------- -0.3V to +7.0V
FBP, FBN, REF,RSTIN to AGND ---------- -0.3V to +7.0V
COMP, FB to PGND ---------- -0.3V to +7.0V
VGHD_SS to GND ---------- -0.3V to +7.0V
VGH,VGHD to GND ---------- -0.3V to +38V
AGND, OGND, PGND to GND ---------- -0.3V to +0.3V

Note1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 2KV
CDM (Charge Discharge Model) ---------- 500V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information(Note2)

Junction Temperature (TJ) ---------- 150℃
Operating Junction Temperature Range (TJ) ---------- -40℃ to 150℃
Ambient Temperature Range ---------- -40℃ to 85℃
Storage Temperature Range ---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 73℃/W
θ_{JC} (Junction-to-Case Thermal Resistance) ---------- 13℃/W
PD (Continuous Power Dissipation) ---------- 1.7W

Note3: Please refer to 1in^2 of 1oz PCB Layout Section.

Electrical Characteristics

(VCC=5.0V , AVDD=12V, AGND=OGND=PGND=GND= 0V TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VCC	VCC input voltage range		2.8		14.0	V
AVDD	AVDD input voltage range		6		18	V
VCC_{UVLO_R}	VCC under voltage lockout rising	Rising	2.6	2.7	2.8	V
VCC_{UVLO_F}	VCC under voltage lockout falling	Falling	2.4	2.5	2.6	V
VAA_{UVLO_R}	AVDD pin voltage detect	Rising	2.3	2.4	2.5	V
VAA_{UVLO_F}	AVDD pin voltage detect	Falling	2.1	2.2	2.3	V
I_{VCC1}	VCC operating current	V_{FB}=1.5V, no switching		1.2		mA
I_{VCC2}	VCC operating current	V_{FB}=1.2V, switching on		2.0		mA
I_{AVDD}	AVDD pin operating current	OPA,DRVP,DRVN ON AVDD=12V		3		mA
SPR	The spread spectrum frequency jitter		-5.0		5.0	%
SPF	The spread spectrum frequency modulation			11		KHz
T_{SD}	Thermal Shutdown Temperature	Rising, Hys.=30℃	---	150	---	°C
T_{HYS}	Thermal Shutdown Hysteresis		---	30	---	°C
REFERENCE VOLTAGE						
REF	Reference voltage	I_{VREF}=100uA	1.238	1.250	1.262	V
REF_{LINE}	REF line regulation	I_{VREF}=100uA, VCC=3.3V to 14V	---	5	10	mV
REF_{LOAD}	REF load regulation	I_{VREF}=0~100uA		5	10	mV
RST Output						
RST_{RISING}	RESET IN detect voltage Rising dege	VCC Rising	1.25	1.30	1.35	V
$RST_{FALLING}$	RESET IN detect voltage Falling dege	VCC falling	1.20	1.25	1.30	V
RST_{I_IN}	RSTIN input current	TA=+25℃	-40	0	40	nA
VRST	RSTIN output voltage	I_{SINK}=1mA			0.2	V
RST_{BLANK}	RST output blanking time	From VCC rises above VCC UVLO_R	135	150	165	mS
VGHD Control						
VGH	VGH input voltage range				37	V
I_{VGH}	VGH input current	VGHD_EN=High			600	uA
	VGH intput current	VGHD_EN=Low			300	uA
VIH	VGHD_EN input high voltage		1.6			V
VIL	VGHD_EN input low voltage				0.6	V
R_{DOWN}	VGHD_EN internal pull low resistor		320	400	480	KΩ
R_{DS_HIGH}	VGH to VGHD switch on resistance	VGHD_EN=High		25	50	Ω
R_{VGHD}	VGHD to GND pull down resistance	VGHD_EN=0V		4.7		KΩ

Electrical Characteristics

(VCC=5.0V , AVDD=12V, AGND=OGND=PGND=GND= 0V TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Boost Regulator						
PON_{DELAY}	Boost Power on Delay time	VCC>2.8V,AVDD>2.8V		5		mS
$AVDD_{SS}$	Boost power on softstart time			10		mS
$FAULT_{TIME}$	Boost Duration to trigger fault condition	FB UVLO trigger	45	50	55	mS
VFB	Boost FB pin feedback voltage		1.238	1.250	1.262	V
FB_{UVLO}	Boost FB under voltage protection		0.95	1.00	1.05	V
FB_{SCP}	Boost FB short output protection	AVDD softstart finish	0.25	0.30	0.35	V
I_{FB}	Boost FB pin input current	V_{FB}=1V to 1.5V	-100		100	nA
V_{AVDD}	Boost output voltage range	AVDD output>VIN+1.5V	VCC		18	V
	Boost FB load regulation	0<Iload<full, transient only	-2		+2	%
FB_{LINE}	Boost FB line regulation	V_{COMP}=1.25V, VCC=3.7 to 14V		0.05	0.15	%/V
I_{LIMIT}	Boost LX current limit	V_{FB}=1.1V Duty cycle=75%	3.0	3.5	4.0	A
LX_{RDSON}	Boost LX on-resistance	ILX=200mA		0.15	0.2	Ω
LX_{LEAK}	Boost LX leakage current	VLX=20V, TA=+25℃		0.01	10	uA
$FOSC_{AVDD}$	Boost oscillator frequency		1.0	1.2	1.4	MHz
$DUYT_{MAX}$	Boost maximum duty cycle		86	90	94	%
Positive Charge-Pump Regulator						
V_{AVDD}	VGH pump supply range (From AVDD)		6		18	V
PON_{DELAY}	VGH power on delay time	Boost softstart finish		5		mS
$FOSC_{CP}$	VGH pump operating frequency		500	600	700	KHz
V_{FBP}	VGH FBP regulation voltage		1.23	1.25	1.27	V
I_{FBP_BIAS}	VGH FBP input bias current	V_{FBP}=1.5V, TA=+25℃	-100		100	nA
R_{DRVPP}	VGH DRVP P-ch on-resistance			3	10	Ω
R_{DRVPN}	VGH DRVP N-ch on-resistance			3	10	Ω
FBP_{UVLO}	VGH FBP under voltage protection		0.95	1.00	1.05	V
$FAULT_{TIME}$	VGH Duration to trigger fault condition	FBP UVP trigger	45	50	55	mS
VGH_{SS}	VGH power on softstart time			3.0		mS

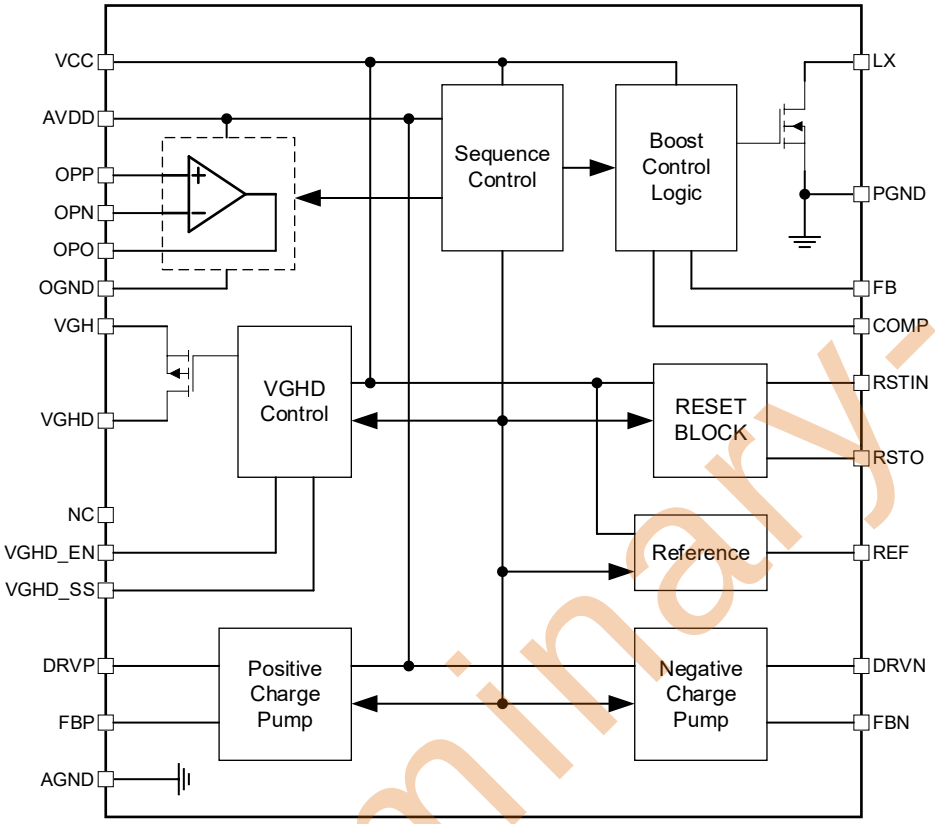
Electrical Characteristics

(VCC=5.0V , AVDD=12V, AGND=OGND=PGND=GND= 0V TA= 25℃)

The device is not guaranteed to function outside its operating conditions. Parameters with MIN and/or MAX limits are 100% tested at +25℃, unless otherwise specified.

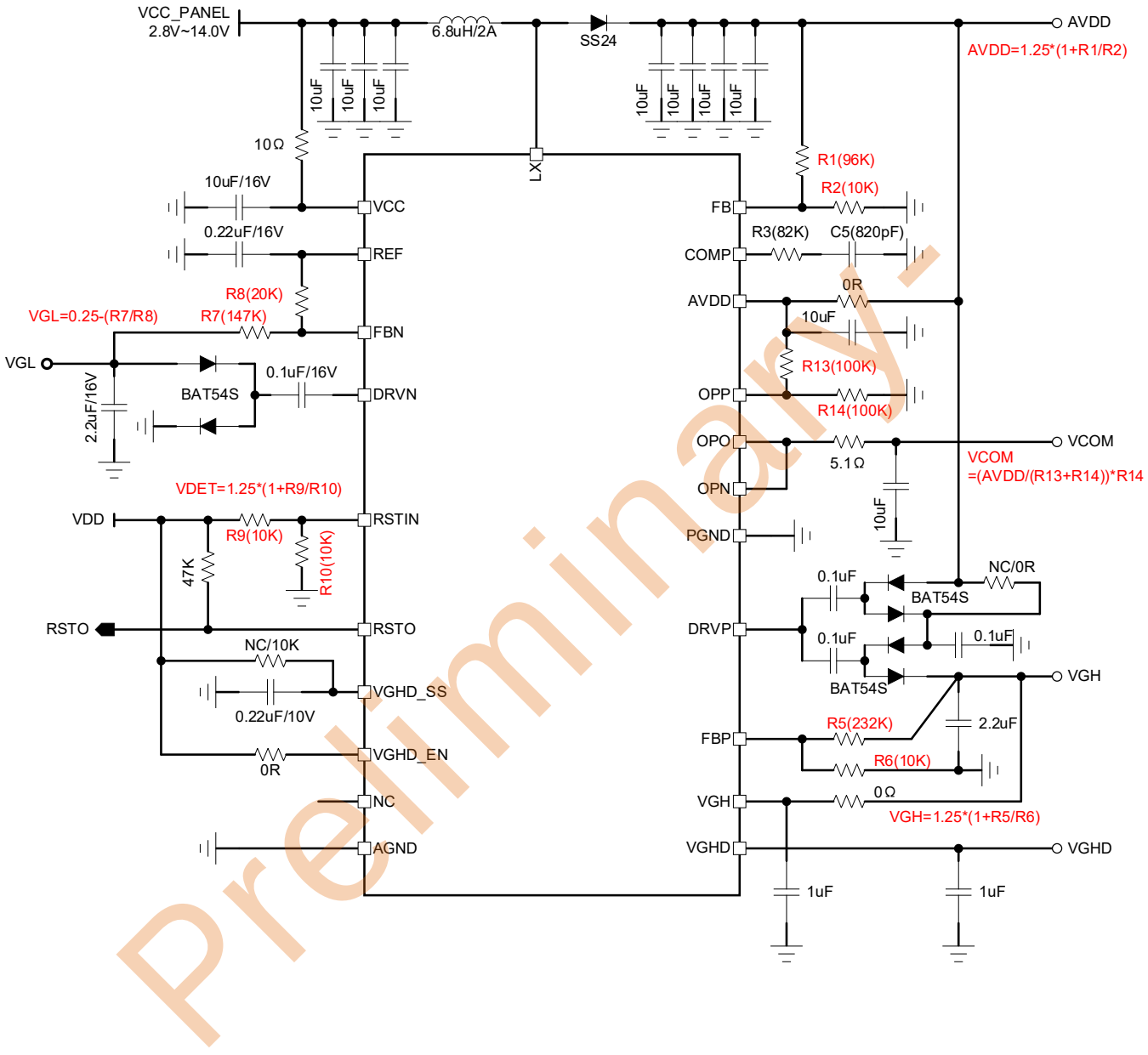
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Negitive Charge-Pump Regulator						
V_{AVDD}	VGL pump supply range (From AVDD)		6		18	V
PON_{START}	VGL power on start time	Boost 1/2*softstart		1/2		
$FOSC_{CP}$	VGL pump operating frequency		500	600	700	KHz
V_{FBN}	VGL FBN regulation voltage		235	250	265	mV
I_{FBN_BIAS}	VGL FBN input bias current	V_{FBN}=0V, TA=+25℃	-40		40	nA
R_{DRVNP}	VGL DRVN P-ch on-resistance			3	10	Ω
R_{DRVNN}	VGL DRVN N-ch on-resistance			3	10	Ω
FBN_{UVLO}	VGL FBN under voltage protection		0.4	0.45	0.5	V
$FAULT_{TIME}$	VGL Duration to trigger fault condition	FBN UVP trigger	45	50	55	mS
VGL_{SS}	VGL power on softstart time			3.0		mS
Operational Amplifier						
V_{AVDD}	OPA supply range (From AVDD)		6		18	V
V_{OVP}	AVDD pin over voltage threshold		18	19	20	V
I_{AVDD}	AVDD for OPA supply current	AVDD=16V Buffer configuration V_{OPA+}=AVDD/2, no load		1	2	mA
V_{OS}	OPA input offset voltage	V_{OPA-}, V_{OPA+}=AVDD/2 TA=+25℃	-10	2	10	mV
I_{BIAS}	OPA input bias current	V_{OPA-}, V_{OPA+}=AVDD/2 TA=+25℃	-100		100	nA
CM	OPA input common mode voltage range		0		VAA	V
VOH	OPA output voltage swing high	Buffer configuration OPAO, I_{OUT}=20mA	VAA-0.35			V
VOL	OPA output voltage swing low	Buffer configuration OPAO, I_{OUT}=-20mA			0.35	V
SR	OPA slew rate	VOUT 20% to 80%, CL=10pF, RL=10K	25	40		V/uS
BW	OPA -3Db bandwidth	CL=10pF, RL=10K	5	10		MHz
I_{SHORT}	OPA short circuit current	Buffer configuration V_{OPA+}=AVDD/2 Short to GND (sourcing)	100	200		mA
I_{SHORT}	OPA short circuit current	Buffer configuration V_{OPA+}=AVDD/2 Short to AVDD (sinking)	100	200		mA

Functional Block Diagram



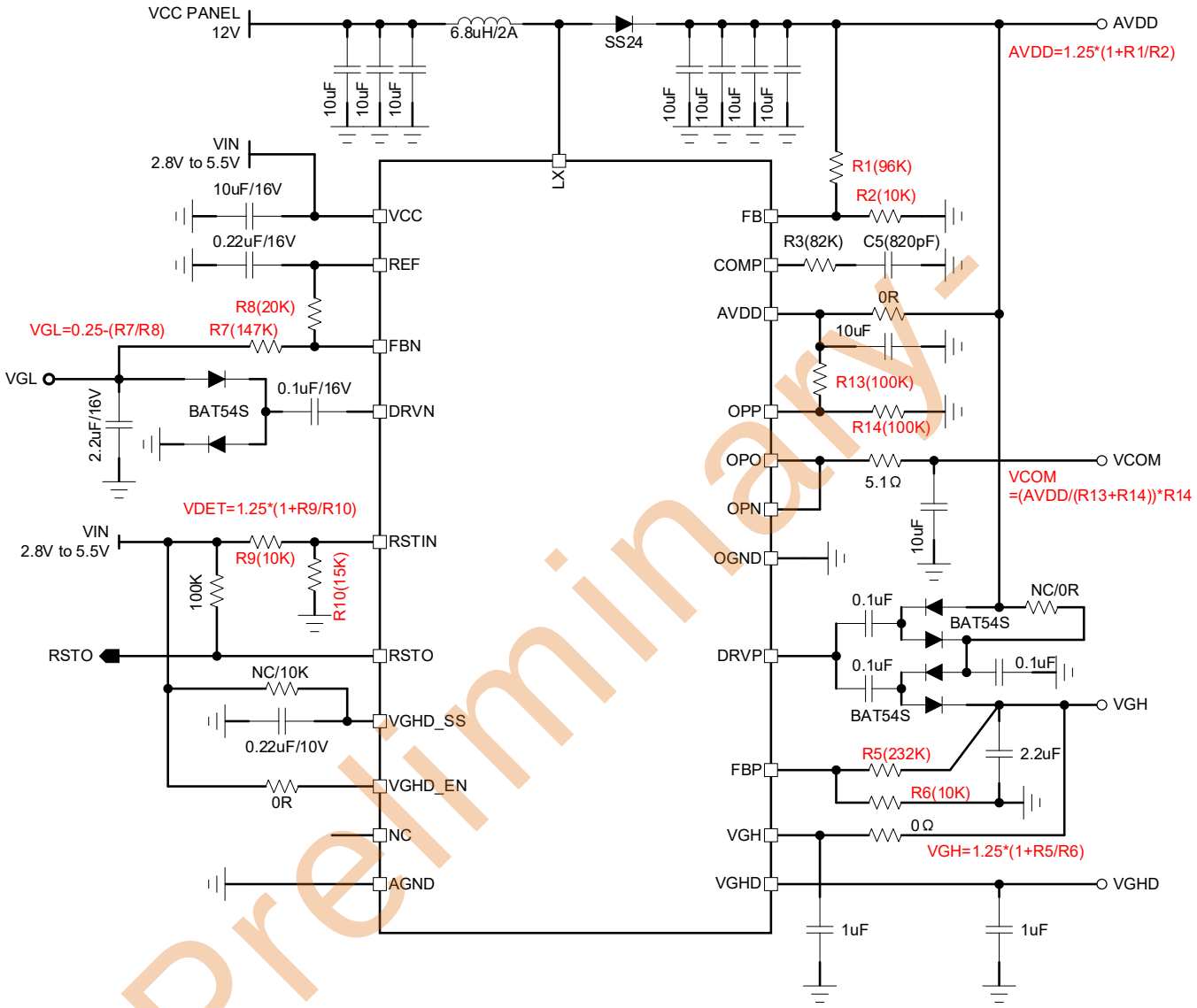
Typical Application Circuit

Single Power Supply



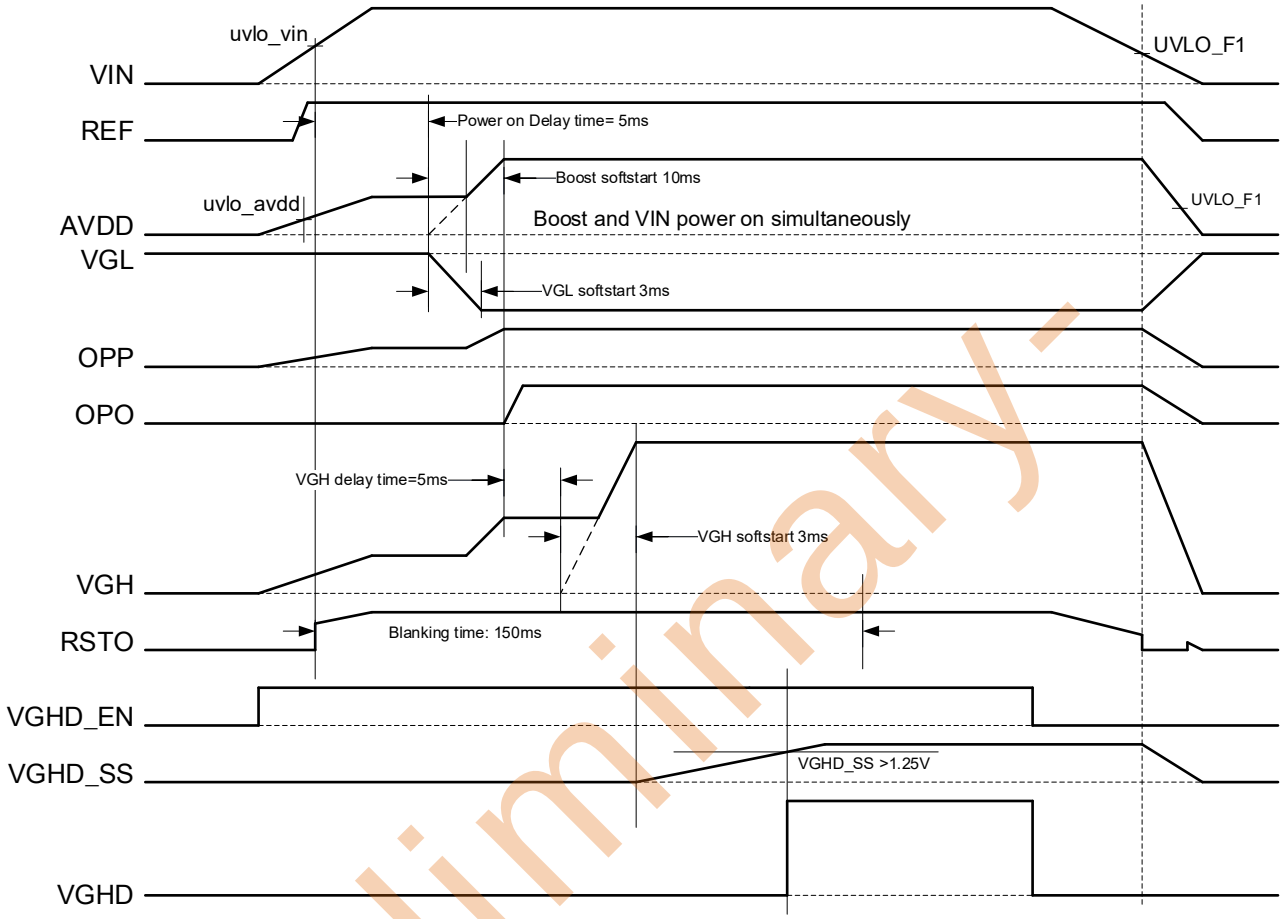
Typical Application Circuit

Dual Power Supply



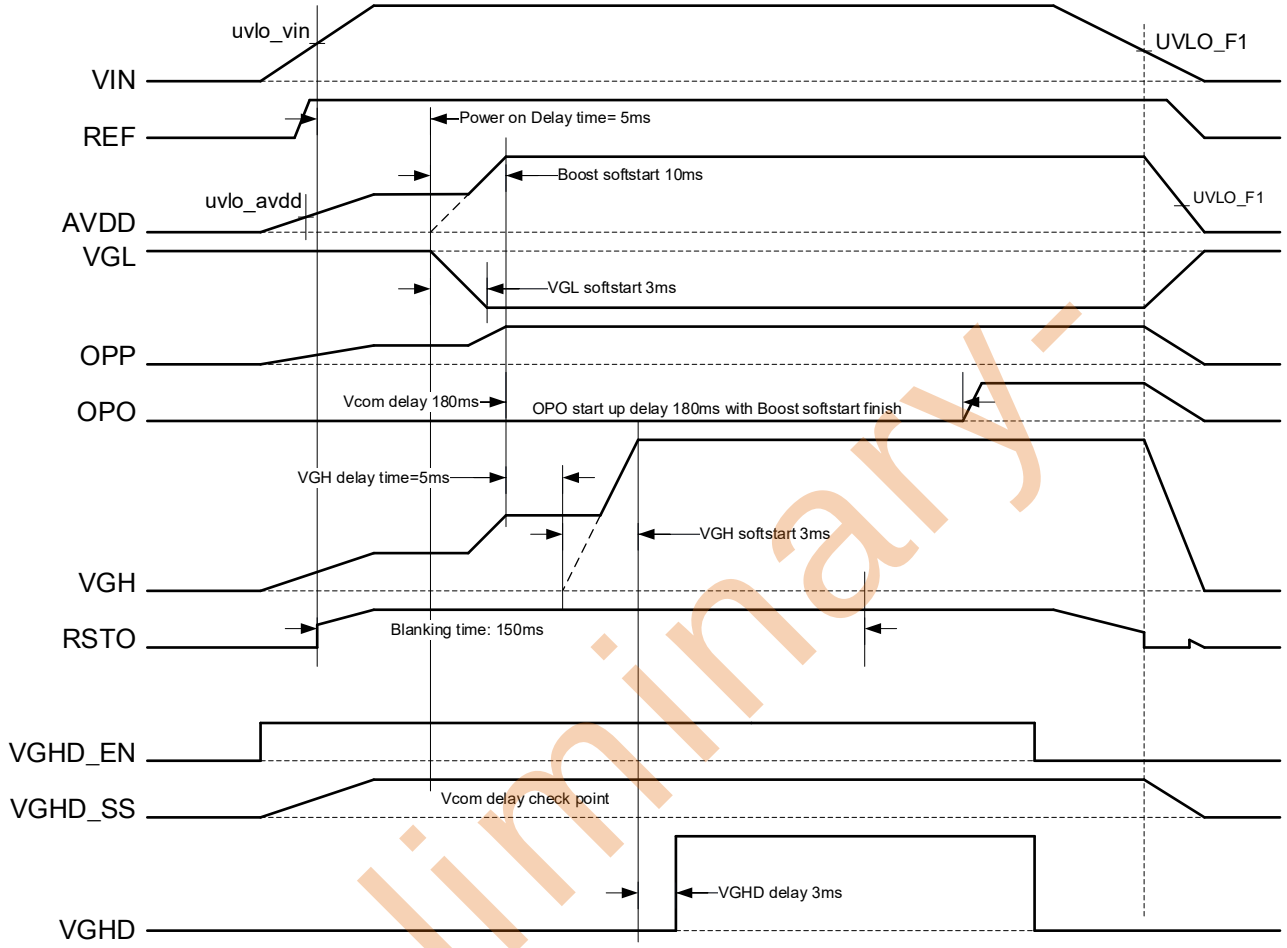
Timing Diagram1

VCC and Boost input power is the same



Timing Diagram2

VCC and Boost input power is the same, and VGHD_SS pull high to VCC



Application Information

The LP6286HQVF-F contains a high performance boost regulator to generate voltage for source driver supply, and gate-on, gate-off charge pumps for gate driver supply. It also includes of a high current rail-to-rail operation amplifier for VCOM, a VGH delay output control and a voltage detector. For more detail description and the component selection are as follows.

Boost Regulator

Description

The boost regulator is a high efficiency current-mode PWM architecture with 1.2MHz operation frequency. It performs fast transient responses to generate source driver supplies for TFT LCD display. The high operation frequency allows smaller components to minimize the thickness of LCD panel. To regulate the output voltage is to set resistive voltage-divider sensing at FB pin. The error amplifier varies the COMP voltage by sensing the FB pin to regulate the output voltage. For better stability, the slope compensation signal that combined with the current sense signal will be compared with the COMP voltage to determine the curret trip point and duty cycle.

Inductor Selection

A 4.7uH or 10uH inductor is recommended for small ripple applications. Small form factor and high efficiency are the major concerns for most LP6286HQVF-F applications. Inductor with low core losses and small DCR(cooper wire resistance) are good choice for LP6286HQVF-F applications.

To keep all current load conditions are in the continuous current mode(CCM), we can calculate the approximate inductor value by the following formula:

$$L > \frac{Eff.typ * (V_{OUT} - V_{IN}) * {V_{IN}}^2}{2 * F_{OSC} * I_{OUT.MIN} * {V_{OUT}}^2}$$

Where $I_{OUT.MIN}$ is the minimum loading current, and the expected efficiency(Eff.typ) is taken from an appropriate curve in the typical performance characteristics.

Output Capacitor Selection

The total output voltage ripple has two components:
the capacitive ripple caused by the charging and discharging of the output capacitance, and the ohmic ripple due to the capacitor's equivalent series resistance (ESR):

$$V_{RIPPLE} = V_{RIPPLE(C)} + V_{RIPPLE(ESR)}$$

$$V_{RIPPLE(C)} \approx \frac{I_{OUT} * (V_{OUT} - V_{IN})}{C_{OUT} * F_{OSC} * V_{OUT}}$$

$$V_{RIPPLE(ESR)} \approx I_{PEAK} * R_{ESR(COUT)}$$

Where I_{PEAK} is the peak inductor current. For ceramic capacitors, the output voltage ripple is typically dominated by $V_{RIPPLE(COUT)}$. The voltage rating and temperature characteristics of the output capactor must also be considered.

Diode Selection

Schottky diodes, with their low forward voltage drop and fast reverse recovery, are the ideal choices for LP6286HQVF-F applications. The forward voltage drop of a Schottky diode represents the conduction losses in the diode, while the diode capacitance (CT or CD) represents the switching losses. For diode selection, both forward voltage drop and diode capacitance need to be considered. Schottky diodes with higher current ratings usually have lower forward voltage drop and larger diode capacitance, which can cause significant switching losses of the LP6286HQVF-F. A Schottky diode rated at 2A is sufficient for most LP6286HQVF-F applications.

Output Voltage Setting
The regulated output voltage is calculated by the follow formula:

$$V_{OUT} = 1.25V * \left(1 + \frac{R1}{R2}\right)$$

The recommended value for R2 should be up to 100KΩ without some sacrificing. Place the resistor divider as close as possible to the chip can reduce noise sensitivity.

Loop Compensation
The voltage feedback loop can be compensated with an external compensation network consisted of R3, C5 as Typical Application Circuit. Choose R3 to set high frequency integrator gain for fast transient response and C5 to set the integrator zero to maintain loop stability. Follow the equations below to obtain better transient response and stable performance for those low-ESR output capacitor applications:

$$R3 = \frac{235 * V_{IN} * V_{OUT} * C_{OUT}}{L * I_{OUT.MAX}}$$

$$C5 = \frac{V_{OUT} * C_{OUT}}{10 * I_{OUT.MAX} * R3}$$

Soft-Start
The LP6286HQVF-F provides internal soft-start function to minimize the inrush current. When power on, an internal constant current charges a built-in capacitor. The rising voltage rate on COMP pin will be limited during the charging period and the inductor peak current will also be limited at the same time. When power off, the built-in capacitor will be discharged for next soft start time.

Over Current Protection
The LP6286HQVF-F main boost converter has the function of peak current protection to limit peak inductor current. It prevents large current damaging the inductor and diode. During the ON-time, once the inductor current exceeds the current limit, the internal LX switch turns off immediately and shortens the duty cycle. Therefore, the output voltage drops if the over-current conditionoccurs. Actual current limit is always larger than the nominal value because of the internal circuit delay.

Over Temperature Protection
The LP6286HQVF-F main boost converter has thermal protection function to prevent the excessive power dissipation from overheating. When the junction temperature exceeds 150°C, it will shut down the device and require VDD power-on-reset (POR) to restart.

Under Voltage Protection
If the boost regulator feedback voltage (FB) or the charge pumps feedback voltage (FBP,FBN) exceed the fault-detection threshold, the LP6286HQVF-F activates an internal timer. If the fault condition continues for 50ms, the PWM will latch off and won't restart until VDD power is cycled. The under-voltage protection is disabled during the soft-start time.

Frequency Spread Spectrum
The LP6286HQVF-F uses switching frequency jitter to spread the switching frequency spectrum to improve EMI performance. This reduces the spectrum spike around the switching frequency and its harmonic frequencies. The frequency jitter range is from -3.7% to +4.6%. The modulation frequency is 11 KHz

Gate on Regulator - VGH

The gate-high regulator is to provide the TFT-LCD gate on voltage. The charge pump can provide a programmable output voltage. To regulate the output voltage must set the resistive voltage-divider sensing at FBP pin. The error amplifier varies the difference voltage by sensing FBP pin to regulate the output voltage as the following equation:

$$V_{GH} = 1.25V * \left(1 + \frac{R5}{R6}\right)$$

Besides, the Schottky diodes with a current rating should equal to or greater than two times of the average charge pump input current.

Gate off Regulator - VGL

The gate-off charge-pump regulator is typically used to generate the negative supply rail for the TFT LCD gate driver ICs. The error amplifier compares the FBN with internal voltage 0.25V to regulate the setting voltage. The output voltage as the following equation:

$$V_{GL} = 0.25V - \left(\frac{R7}{R8}\right)$$

Operational Amplifier

The function of the operational amplifier is to drive the LCD backplane VCOM. The operational amplifier features ±150mA output short circuit current, 25V/μs slew rate.

Voltage Detector

The voltage detector monitors the RSTIN voltage to generate a reset signal while RSTIN is lower than the detecting level and the detecting level is decided by an external resistor divider.

$$V_{DET} = V_{RSTIN} * \left(1 + \frac{R9}{R10}\right) = 1.25V * \left(1 + \frac{R9}{R10}\right)$$

$$V_{HYS} = 50mV * \left(1 + \frac{R9}{R10}\right)$$

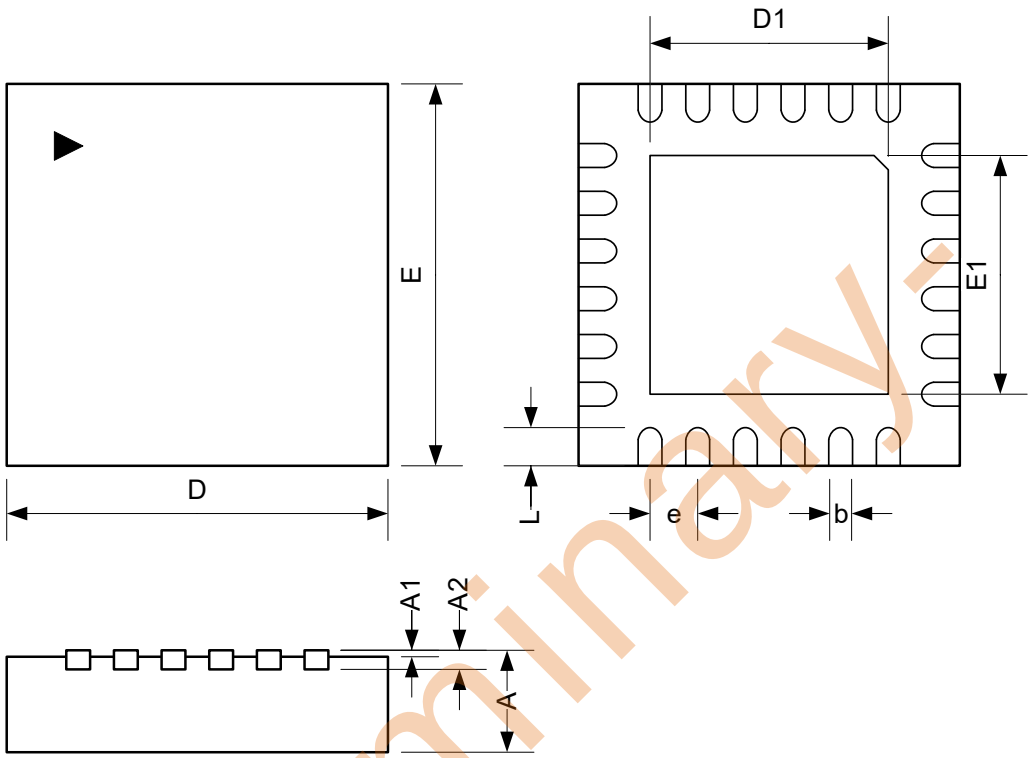
The controller would issue a blanking period about 163ms after VCC reaching UVLO threshold. During the blanking period, voltage detector would ignore the VCC drop and keep RSTO in high impedance. After the blanking period and if RSTIN goes below 1.25V, RSTO is pulled low indicating low RSTIN input. RSTO stays low until VCC falls below approximately 1V. Then RSTO cannot be held low any more and RSTO is pulled up by the external resister. For more detail timing information, please reference the Power-On Power-Off Timing Chart.

Protection Table

Block	Protection	Work Condition	Behavior	Recovery
Boost	OCP	3.0A(min.)		
	UVP	FB<1.0V, after 50ms	LX stop switching, IC shutdown and latch	VCC re-power up
	SCP1	AVDD<uvlo_f (2.4V) (at start up finished)	LX stop switching, IC shutdown and latch	VCC re-power up
	SCP2	FB<0.3V (at start up finished)	LX stop switching, IC shutdown and latch	VCC re-power up
	OVP	FB>1.4V	LX stop switching	Vout<OVP-Hys, FB Hys 0.1V(typ.) LX switch at next clk.
	OVP	AVDD pin > 19V	LX stop switching	Vout<OVP-Hys,Hys=0.5V(typ.) LX switch at next clk.
POS Pump	UVP	FBP<1.0V, Ater 50ms	IC shutdown and latch	VCC re-power up
NEG Pump	UVP	FBN>0.45V, Ater 50ms	IC shutdown and latch	VCC re-power up
OPA	OCP	±150mA	Current limit keep	N/A
	SCP	±150mA	Current limit keep	N/A
SYS	OTP	IC temp > 150℃	IC shut down	Recovery of hysteresis Temperature of hysteresis: 20℃

Packaging Information

QFN4X4-24



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.0276	0.0295	0.0315
A1	0.00	---	0.05	0.0000	---	0.0020
A2	0.20 REF			0.0079 REF		
D	3.90	4.00	4.10	0.1535	0.1575	0.1614
E	3.90	4.00	4.10	0.1535	0.1575	0.1614
D1	2.55	2.70	2.80	0.1004	0.1063	0.1102
E1	2.55	2.70	2.80	0.1004	0.1063	0.1102
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
e	0.5 BSC			0.0256 BSC		
L	0.30	0.40	0.50	0.0118	0.0157	0.0197