Features

- Easy-to-use standalone high-efficiency 1-cell switching charger
  - Proprietary sensorless technique
  - 4.1V to 6.2V input voltage with 28V absolute maximum input voltage rating
  - Resistor programmable charge voltages 4.1V/4.2V/4.25V/4.35V and 3.6V/4.2V/4.40V/4.45V
  - 3.5A maximum fast charge current
  - 1.2MHz switching frequency
  - 94% high efficiency @ VBAT=3.8V, ICHG=2A
  - 91% high efficiency @ VBAT=3.8V, ICHG=3A
  - Input voltage regulation to allow weak input power source to charge battery (VINDPM)
  - Support trickle charge, precharge, Constant Current (CC) charge and Constant Voltage (CV) charge, charge termination and recharge
- High charge accuracy
  - +/- 0.5% charge voltage regulation
  - +/- 6% charge current regulation
- High integration
  - Integrated all MOSFETs
  - Internal loop compensation
  - LED charge indication driver
- Protections
  - Cycle-by-cycle current limit protection
  - Input under-voltage lockout (UVLO)
  - Input over-voltage protection (OVP)
  - Cold/hot battery temperature monitoring
  - Junction temperature thermal regulation
  - Charge safety timer
- Packaging
  - DFN3x3-10
  - RoHS compliant and halogen free
  - 100% lead (Pb) free
  -

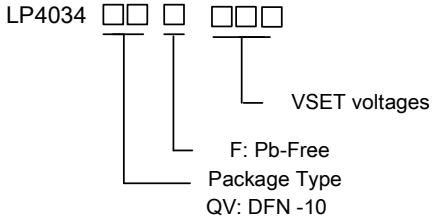
Applications

- Portable battery powered devices
- Gaming devices
- Charging docks and cradles
- E-Cigarette

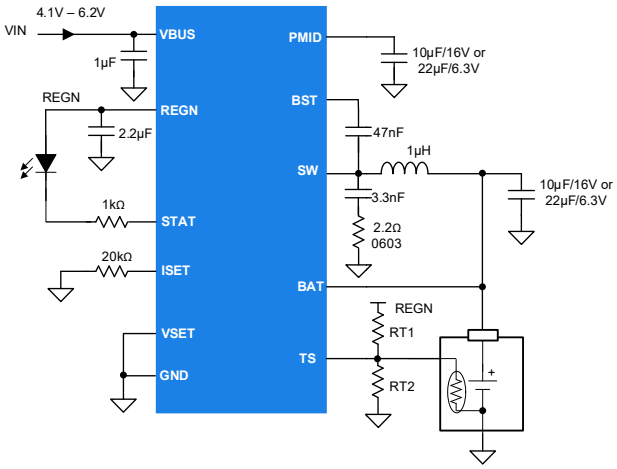
General Description

The LP4034 is a standalone 1-cell switching battery charger providing up to 3.5A charge current to the battery from 4.1V to 6.2V input voltage. The charge current is programmable by a resistor connected from ISET to GND and the charge voltage is programmable by a resistor connected from VSET to GND. The charge can be enabled and disabled from ISET pin. The LP4034 operates at 1.2MHz switching frequency allowing a small-size 1uH inductor for 3.5A fast charging. The patent-protected integrated current sensing technique eliminates external sensing resistor allowing very high charge efficiency, low BOM cost and small footprint. The precharge, fastcharge and termination current accuracy is competitive compared to external-resistor-based current sensing architecture. LP4034 is available in DFN3x3-10 package.

Order Information



Application Circuit

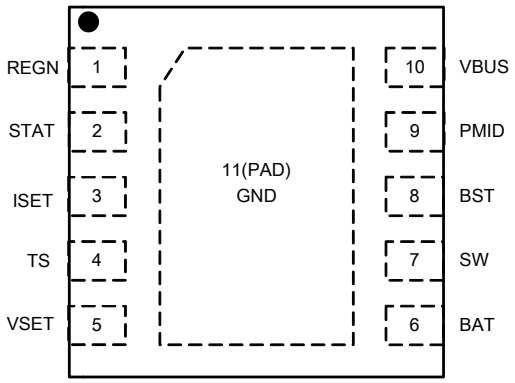


(BOM are shown in Figure 11)

Device Information

Part Number	Battery Voltage	Top Marking	Package	Moisture Sensitivity Level	Shipping
LP4034QVF	4.1V/4.2V/4.25V/4.35V	LPS LP4034 YWX	DFN-10	MSL3	5K/REEL
LP4034QVF-445	3.6V/4.2V/4.40V/4.45V	LPS LP4034 445YWX	DFN-10	MSL3	5K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

Pin Diagram



DFN3x3-10 (Top View）

Pin Description

Pin #	Name	Description
1	REGN	Positive LDO output. Connect a 2.2μF ceramic capacitor from REGN to GND. The capacitor should be placed close to the IC.
2	STAT	Charge status indication output. Connect a LED from REGN pin to STAT pin via a current limiting resistor. The STAT pin indicates charger status: • Charge in progress: STAT pin is pulled LOW • Charge complete or charger in SLEEP mode: STAT pin is OPEN • Fault mode: STAT pin blinks
3	ISET	Charge current program input. Connect a 1% resistor RISET from this pin to ground to program the charge current. If ISET pin is floating or pulled high (>1.3V), charge is disabled. If ISET pin is pulled low, charge is disabled. No capacitor is allowed to connect at this pin.
4	TS	Battery temperature sense thermistor input. Charge is suspended if the battery thermistor temperature is out of range. Leave the TS pin floating if TS pin function is not used.
5	VSET	Charge voltage setting input. VSET pin sets battery charge/regulation voltage. Program battery regulation voltage with a resistor connected from VSET to GND. No capacitor is allowed to connect at this pin. For LP4034QVF: • RVSET floating (>200kΩ+/-10%): V_{BATREG} = 4.1V • RVSET = 51 kΩ +/-10%: V_{BATREG} = 4.35V • RVSET = 10kΩ +/-10%: V_{BATREG} = 4.25V • RVSET shorted to GND (< 510Ω): V_{BATREG} = 4.2V LP4034QVF-445: • RVSET floating (>200kΩ+/-10%): V_{BATREG} = 4.2V • RVSET = 51 kΩ +/-10%: V_{BATREG} = 4.40V • RVSET = 10kΩ +/-10%: V_{BATREG} = 4.45V • RVSET shorted to GND (< 510Ω): V_{BATREG} = 3.6V
6	BAT	Battery connection pin. Connect this pin to node of inductor output terminal and battery pack positive terminal. ≥10uF capacitor is recommended to connect to this node.
7	SW	Switching node. Internally SW node is connected to the source of the n-channel HSFET and the drain of the N-channel LSFET. Connect this pin to a terminal of external inductor.
8	BST	High-side MOSFET driver supply input. BST is internally connected to the cathode of the internal boot-strap diode. Connect 47nF bootstrap capacitor from BST to SW.
9	PMID	Connected to the drain of the reverse blocking N-channel MOSFET (RBFET) and the drain of high-side MOSFET (HSFET). Place ceramic 10μF on PMID to GND and place it as close as possible to IC.
10	VBUS	Charger input connection. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1uF ceramic capacitor from VBUS to GND and place it as close as possible to IC.
11	GND	Power ground and analog ground. The GND is down-bonded to the pad.

Absolute Maximum Ratings (Note)

VBUS, PMID voltage to GND ---------- -0.3V to 28V
SW, BAT Voltage to GND ---------- -0.3V to 9V
BST to SW Voltage to GND ---------- -0.3V to 6V
REGN, STAT, ISET, TS, VSET Voltages to GND ---------- -0.3V to 6V
STAT Sink Current ---------- 6mA
REGN Source Current ---------- 16mA
Maximum Junction Temperature (Tj) ---------- 150℃
Storage Temperature Range ---------- -40℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model) ---------- 2kV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 45℃/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage	4.1		6.2	V
I_{CHG}	Fast Charge Current	0.35		3.5	A
V_{BAT}	Battery Charge Voltage	4.1		4.4	V
T_J	Operating Junction Temperature Range (T_J)	-40		125	℃
T_A	Ambient Temperature Range	-40		85	℃
L	Output Inductance(1)	0.7	1	2.64	μH
C_{REGN}	REGN LDO Capacitance (1) (3)	1	2.2	4.7	μF
C_{IN}	Input Capacitance (1) (2)	0.6	1	4.7	μF
C_{PMID}	PMID Capacitance(1) (2)	4	10	40	μF
C_{BAT}	BAT Capacitance(1) (3)	4	10	40	μF

Notes:

(1) The values recommended in the table are effective inductance and capacitance.

(2) X7R and 16V or higher voltage rating are recommended.

(3) X7R and 10V or higher voltage rating are recommended.

Electrical Characteristics

(The specifications are at V_{VBUS_LOWV} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, L=1uH, T_J = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT						
I_{Q_BAT}	Battery reverse current	VBAT= VSW = 4.5V, VBUS pin floating			1	μA
I_{Q_BAT}	Battery leak current	Charge is terminated, V_{BAT}=4.5V			5	μA
I_{Q_BAT}	Battery leak current	ISET pin floating, V_{BAT}=4.5V			5	μA
I_{Q_BAT}	Battery leak current	ISET pin short, V_{BAT}=4.5V			5	μA
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS}=5V, I_{REGN}=16mA	4.2		5.0	V
I_{REGN}	REGN LDO output current				16	mA
I_{REGN}	REGN LDO short circuit protection			20		mA
MOSFETS						
R_{DSON_Q1}	RBFET on-resistance	V_{VVBUS}=5V		38		mΩ
R_{DSON_Q2}	HSFET on-resistance	V_{VVBUS}=5V		55		mΩ
R_{DSON_Q3}	LSFET on-resistance	V_{VVBUS}=5V		48		mΩ
INPUT VOLTAGE						
V_{VBUS}	VBUS operation range		4.1		6.2	V
V_{VBUS_LOWV}	REGN turn-on threshold	V_{VBUS} rising	3.65	3.75	3.85	V
$V_{VBUS\_LOWV\_HYS}$	REGN turn-on threshold hysteresis	V_{VBUS} falling		300		mV
V_{SLEEP}	Into sleep mode threshold	V_{VBUS} falling, V_{VBUS}-V_{BAT}	30	60	90	mV
V_{SLEEPZ}	Exit sleep mode threshold	V_{VBUS} rising, V_{VBUS}-V_{BAT}	110	150	250	mV
V_{INDPM_MIN}	Minimum V_{INDPM}	V_{BAT}=3.5V	3.9	4.0	4.1	V
V_{INDPM}	V_{INDPM}	V_{BAT}=4.0V V_{INDPM}=V_{BAT}+0.25V	4.175	4.25	4.325	V
$V_{VBUS\_OVP\_RISE}$	V_{VBUS} input overvoltage threshold	V_{VVBUS} rising	6.2	6.4	6.6	V
$V_{VVBUS\_OVP\_HYS}$	VBUS input overvoltage threshold hysteresis	V_{VVBUS} falling		0.5		V

Electrical Characteristics

(The specifications are at V_{VBUS_LOWV} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, L=1uH, T_J = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CHARGER						
V_{BATREG}	Charge voltage regulation	LP4034QVF	4.079	4.1	4.121	V
			4.179	4.2	4.221	V
			4.328	4.35	4.372	V
			4.22	4.25	4.273	V
V_{BATREG}	Charge voltage regulation	LP4034QVF-445	4.179	4.2	4.221	
			4.375	4.4	4.425	
			4.425	4.45	4.475	
			3.576	3.6	3.624	
I_{CHG}	Fast charge current	R_{ISET} = 40kΩ, V_{VBUS}=5V, V_{BAT}=3.8V	940	1000	1060	mA
		R_{ISET} = 20kΩ, V_{VBUS}=5V, V_{BAT}=3.8V		2000		mA
		R_{ISET} = 13.3kΩ, V_{VBUS}=5V, V_{BAT}=3.8V		3000		mA
I_{PRECHG}	Precharge current	R_{ISET} = 40kΩ, V_{VBUS}=5V, V_{BAT}=2.5V	70	100	130	mA
		R_{ISET} = 20kΩ, V_{VBUS}=5V, V_{BAT}=2.5V		200		mA
		R_{ISET} = 13.3kΩ, V_{VBUS}=5V, V_{BAT}=2.5V		300		mA
I_{TERM}	Termination current	R_{ISET} = 40kΩ, V_{VBUS}=5V	70	100	130	mA
		R_{ISET} = 20kΩ, V_{VBUS}=5V		200		mA
		R_{ISET} = 13.3kΩ, V_{VBUS}=5V		300		mA
$V_{BAT\_SHORT\_RISE}$	V_{BAT} short rising threshold	Battery short to precharge	2.05	2.20	2.35	V
I_{BAT_SHORT}	Trickle charge current	V_{VBUS}=5V, V_{BAT}=1.0V	50	60	70	mA
$V_{BAT\_SHORT\_FALL}$	V_{BAT} short falling threshold	Precharge to battery short	1.85	2.0	2.15	V
$V_{BAT\_LOWV\_RISE}$	V_{BAT} fast charge rising threshold	Precharge to fast charge	2.9	3.0	3.1	V
$V_{BAT\_LOWV\_FALL}$	V_{BAT} fast charge falling threshold	Fast charge to precharge charge	2.6	2.7	2.8	V
V_{RECHG_HYS}	Recharge threshold	V_{BAT} falling		160		mV
STAT						
f_{STAT_BLK}	Blinking frequency	50% duty		1		Hz
I_{STAT_PD}	STAT pull-down current				6	mA

Electrical Characteristics

(The specifications are at V_{VBUS_LOWV} < V_{VBUS} < V_{VBUS_OVP} and V_{VBUS} > V_{BAT} + V_{SLEEP}, L=1uH, T_J = 25°C unless otherwise noted)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SWITCHING CONVERTER						
F_{SW}	Switching Frequency		1080	1200	1320	kHz
I_{HSFET_OCP}	HSFET Over Current Protection			5.4		A
I_{LSFET_OCP}	LSFET Reverse Current Protection			1.8		A
D_{MAX}	Maximum duty cycle			97		%
ISET SETTING						
V_{ISET}	ISET pin regulated voltage		0.985	1	1.015	V
K_{ICHG}	Charge current setting ratio	I_{CHG}(A) = K_{ICHG} / RISET(kΩ)		40		AxkΩ
COLD/HOT THERMISTOR COMPARATOR						
V_{T1}%	T_{COLD} (0°C) threshold, charge suspend if V_{TS} is above the threshold	V_{TS} rising, as percentage of V_{REGN}		73.5		%
V_{T1}%		V_{TS} falling, as percentage of V_{REGN}		71.5		%
V_{T3}%	T_{HOT} (45°C) threshold, charge suspend if V_{TS} is below the threshold	V_{TS} falling, as percentage of V_{REGN}		47.25		%
V_{T3}%		V_{TS} rising, as percentage of V_{REGN}		48.25		%
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Thermal regulation		110	120	135	°C
T_{SHUT_RISE}	Thermal shut down	Temperature rise		150		°C
T_{SHUT_FALL}	Thermal shut down	Temperature fall		120		°C
TIMING REQUIREMENTS						
t_{TERM}	Termination deglitch time			100		ms
t_{SAFETY_FAST}	Fast charge safety timer	V_{BAT} > $V_{BAT\_LOWV\_RISE}$		20		hr
t_{SAFETY_PRE}	Precharge safety timer	V_{BAT} < $V_{BAT\_LOWV\_RISE}$		2.0		hr

Typical Characteristics

(L=1μH, C_1, C2, C3, C5=10μF, C4= 2.2μF and T_J = 25°C unless otherwise noted; the schematic is as shown in Figure 11)

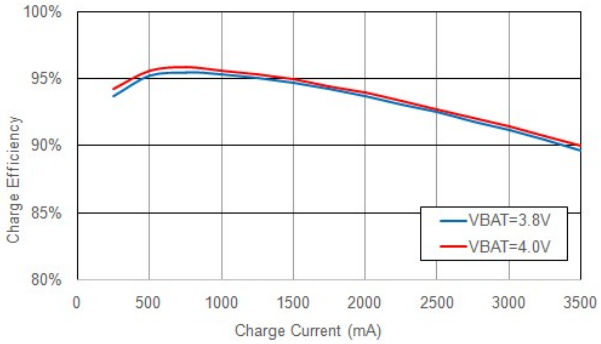


Figure 1. Battery Charge Efficiency
(Inductance: L = 1uF, 4.0mmx4.0mm, DCR=25mΩ)

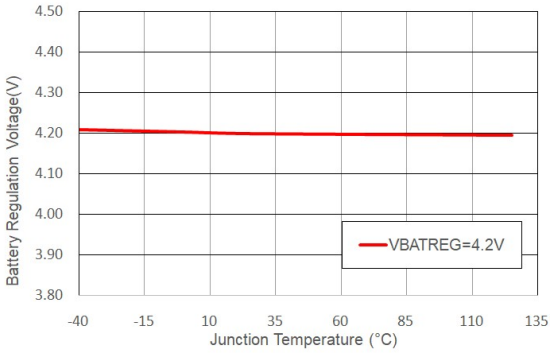


Figure 2. Battery Regulation Voltage vs. Junction Temperature (VSET tied to GND)

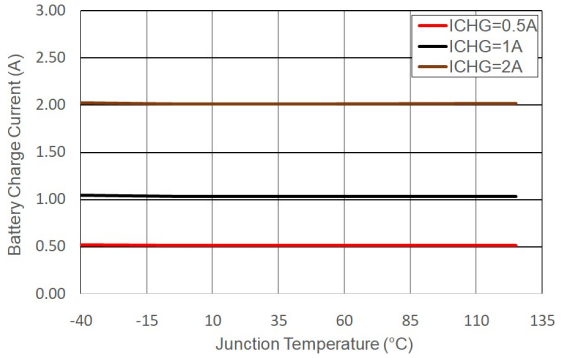


Figure 3. Charge Current vs. Junction Temperature

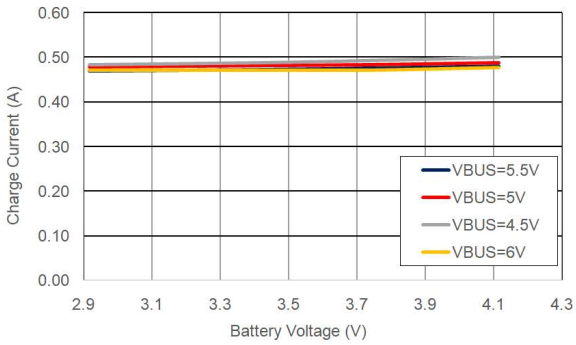


Figure 4. Charge current vs. Battery Voltage (RISET=82kΩ)

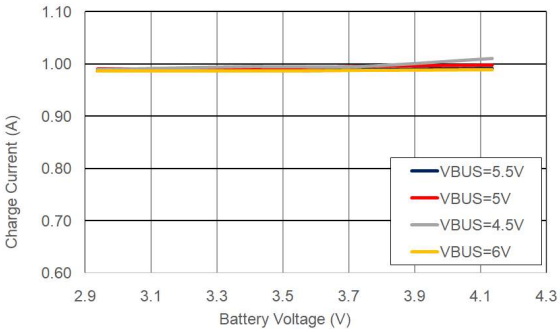


Figure 5. Charge current vs. Battery Voltage (RISET=40kΩ)

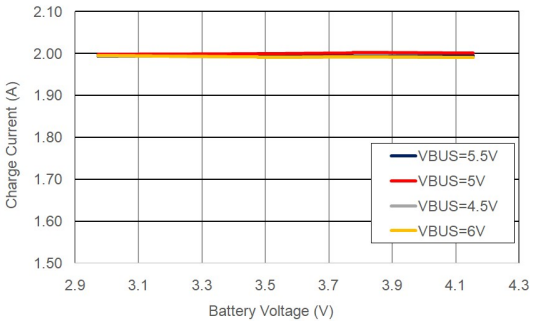


Figure 6. Charge current vs. Battery Voltage (RISET=20kΩ)

Typical Characteristics

(L1=1μH, C_1, C2, C3, C5=10μF, C4= 2.2μF and T_J = 25°C unless otherwise noted; the schematic is as shown in Figure 11)

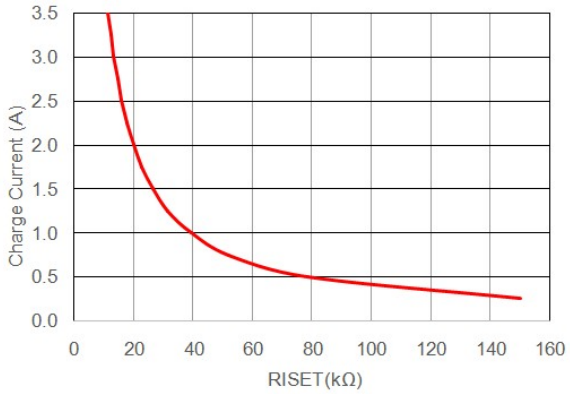


Figure 7. Charge Current vs. Charge Current Setting Resistance RISET

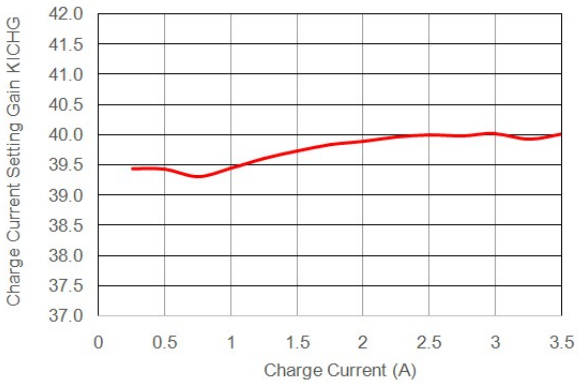
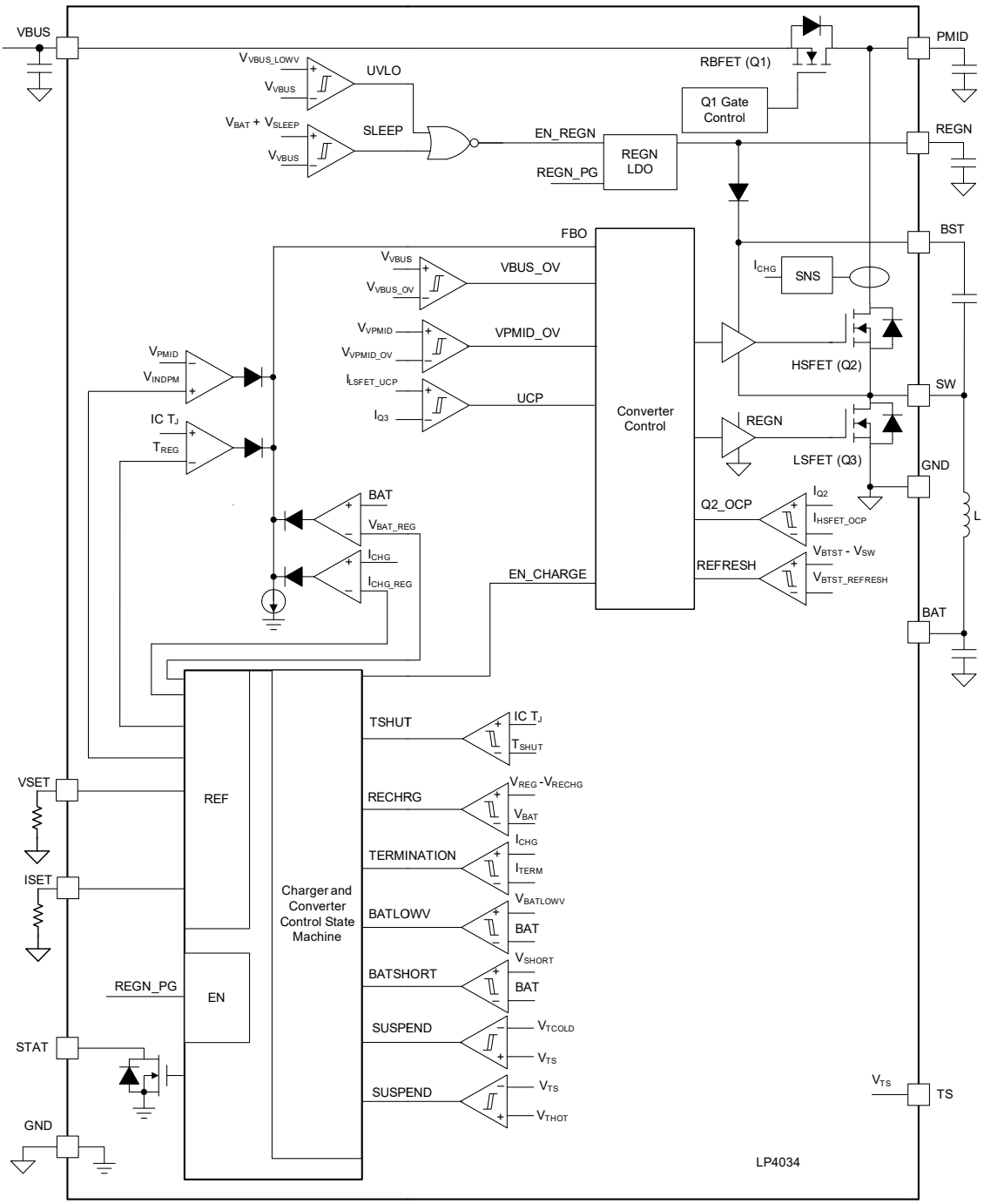


Figure 8. Charge Current Setting Gain vs. Charge Current

Functional Block Diagram



Detailed Description

Overview

The LP4034 is a highly-integrated switching charger for 1-cell Li-Ion and Li-Polymer batteries. The charge voltage is set by an external resistor connected from VSET pin to GND and the charge current is set by an external resistor connected from ISET pin to GND. The charge current is programmable up to 3.5A. To initiate a charge cycle, the conditions of charger power-up must be met. The device charges battery in four modes: trickle charge, pre-charge, Constant Current (CC) charge, and Constant Voltage (CV) charge. The charger terminates the charge cycle when the charge current is below termination threshold I_{TERM} and charge voltage is above recharge threshold. When a fully charged battery's voltage is discharged below recharge threshold, the device automatically starts a new charging cycle and safety timer starts counting. The STAT pin output indicates the charging status of charging, charging complete or charge disabled or charging faults. Charge safety timer is built in to enhance the charger's safety features.

REGN LDO Power-up

The REGN LDO supplies part of internal bias circuits as well as the HSFET and LSFET gate driver. The REGN also supplies STAT LED indication and internal and external TS resistor dividers. The REGN LDO is enabled after sleep comparator deglitch time, VSET detection time and REGN delay time if the below conditions are met:

- V_{VBUS} above V_{VBUS_LOWV}
- V_{VBUS} above V_{BAT} + V_{SLEEPZ}

REGN LDO remains on in fault mode. REGN LDO is powered from VBUS only.

Converter and Charger Power-up

Following REGN LDO successful power-up, if there is no below faults detected and ISET pin is normal, converter powers up and charge is enabled. The faults include:

- Input OVP fault: V_{VBUS} > V_{VBUS_OVP}
- TS cold/hot fault
- Safety timer fault
- Junction temperature is above T_{SHUT}

Device Functional Mode

The device operates in different modes depending on VBUS voltage, battery voltage and ISET pin connection. The functional modes are listed in the following table.

Table 1: Device Functional Mode

MODE	CONDITIONS	REGN	CHARGE	STAT
ISET Pin Open/Short	ISET open or short to GND	ON	NO	OPEN
HiZ Mode	V_{VBUS} < V_{VBUS_LOWV}	OFF	NO	OPEN
Sleep Mode	V_{VBUS} > V_{VBUS_LOWV} V_{VBUS} < V_{BAT+} V_{SLEEP_Z}	OFF	NO	OPEN
Charge Mode	V_{VBUS} > V_{VBUS_LOWV} V_{VBUS} > V_{BAT} + V_{SLEEP_Z} V_{VBUS} < $V_{VBUS\_OVP\_RISE}$	ON	YES	SHORT to GND
Charge Termination Mode	V_{VBUS} > V_{VBUS_LOWV} V_{VBUS} > V_{BAT} + V_{SLEEP_Z} V_{VBUS} < $V_{VBUS\_OVP\_RISE}$ No faults and charge is terminated	ON	NO	OPEN
Fault Mode	Any of the faults below if charge mode is initiated: • Input OVP • TS Cold/Hot • Thermal Shutdown • Safety timer expires	ON	NO	BLINKING

Battery Charge Profile

In Charge Mode as shown in the table of Device Functional Mode, the devices charge the battery in four sub-charge-modes: trickle charge, pre-charge, Constant Current (CC) charge and Constant Voltage (CV) charge as shown in Figure 9. If the battery voltage falls below VBAT_SHORT_FALL, the battery charge battery with trickle charge current IBAT_SHORT, when the battery voltage rises above VBAT_SHORT_RISE and below VBAT_LOWV_RISE, the charger charges battery in precharge mode with charge current at IPRECHG. Fast charge starts once battery voltage rises above VBAT_LOWV_RISE. When battery voltage is close to battery charge voltage VBATREG, the charger goes into CV mode and charge current starts to decreases. When charge current decreases below termination current ITERM, charge is terminated and charge cycle ends. Following charge termination, if the battery voltage follows below (VBATREG – VRECHG_HYS), a new charge cycle restarts.

Trickle Charge

The device charges the battery at a fixed charge current I_{BAT_SHORT} if the battery is below V_{BAT} < V_{BAT_SHORT}.

Precharge

The device charges the battery at 10% of programmed fast charge current I_{CHG} in precharge mode. Precharge is enabled in charge mode when the precharge condition $V_{BAT\_SHORT\_RISE}$ < V_{BAT} < $V_{BAT\_LOWV\_RISE}$ are met.

Constant Current (CC) Charge

CC charge is also called fast charge. The device charges the battery from Buck converter at current level of K_{ICHG} / RISET, where K_{ICHG} is the gain of charge current setting. Fast charge starts when fast charge conditions are met.

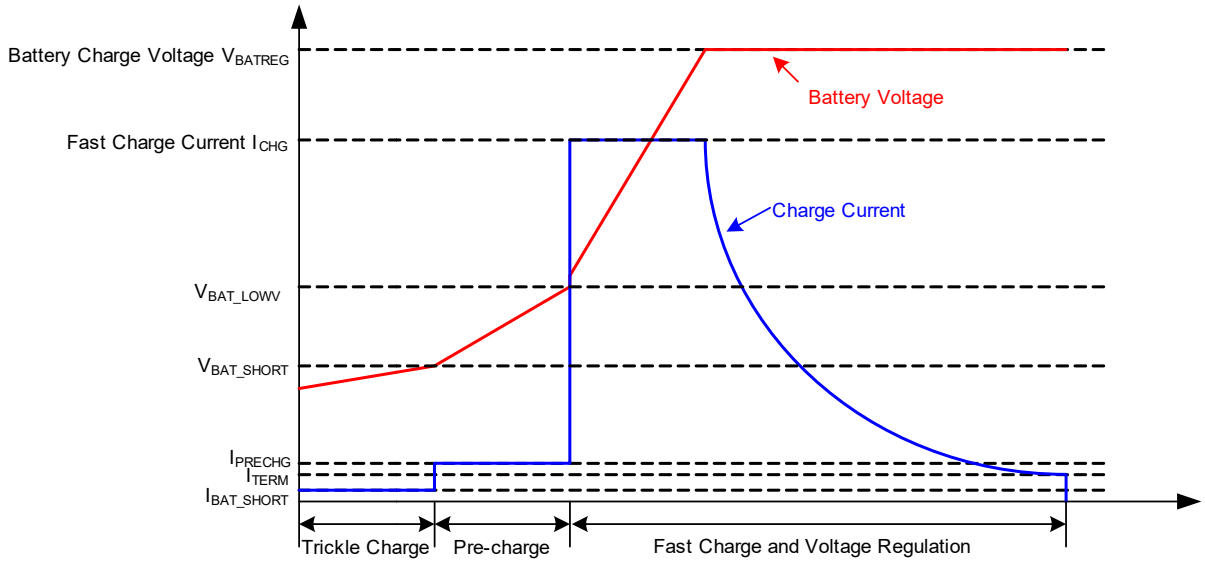


Figure 9. Battery Charge Profile

Table 2. Charge Current in Charge Mode

CHARGE MODE	BATTERY VOLAGE V_{BAT}	CHARGE CURRENT	TYPICAL VALUES (mA)
Trickle Charge	$V_{BAT} < V_{BAT\_SHORT\_FALL}$	I_{BAT_SHORT}	60
Precharge	$V_{BAT\_SHORT\_RISE} < V_{BAT} < V_{BAT\_LOWV}$	I_{PRECHG}	10% of I_{CHG}
Fast Charge	$V_{BAT\_LOWV} < V_{BAT} < V_{BATREG}$	I_{CHG}	K_{ICHG} / RISET
CV Charge	$V_{BAT\_LOWV} < V_{BAT} < V_{BATREG}$	$< I_{CHG}$	Variable

Constant Voltage (CV) Charge

With the battery voltage charged up, the BAT pin voltage reaches the battery regulation voltage V_{BATREG} and the charge current starts to decrease from fast charge current I_{CHG}. The actual battery voltage keeps increasing until charge termination is triggered.

Charge Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold (V_{BATREG} - V_{RECHG_HYS}) and the charge current is below termination current I_{TERM} for deglitch time t_{TERM}. The termination current threshold I_{TERM} is 10% of fast charge current I_{CHG}, which is set by the RISET resistor connected at ISET pin.

Battery Recharge

Once a charge cycle is terminated, safety timer is disabled. If battery voltage V_{BAT} decreases below the recharge threshold (V_{BATREG} - V_{RECHG_HYS}) and the charge mode conditions are met, the charger is enabled again and safety timer is reset and starts counting. Besides recharge, charge cycle could restart if V_{VBUS} voltage is recycled or ISET pin is released from an open/short/pulled-up condition.

Battery Temperature Monitoring

The charger device provides a single NTC thermistor input TS pin for battery temperature monitor. RT1 and RT2 resistor programs the cold temperature T1 and hot temperature T3. In the Equations (1) and (2), RNTC,T1 is NTC thermistor resistance value at temperature T1 and RNTC,T3 is NTC thermistor resistance values at temperature T3. VT1% and VT3% can be found n the Electronic Characteristics table. Select 0°C to 45°C for battery charge temperature range, then NTC thermistor 103AT-2 resistance are RNTC,T1 = 27.28 kΩ (at 0°C) and RNTC,T3 = 4.91 kΩ (at 45°C). From Equation (1) and Equation (2), RT1 and RT2 are derived as below, which is the resistance to set the charge temperature range 0 to 45°C.

- RT1 = 4.52 kΩ
- RT2 = 23.2 kΩ

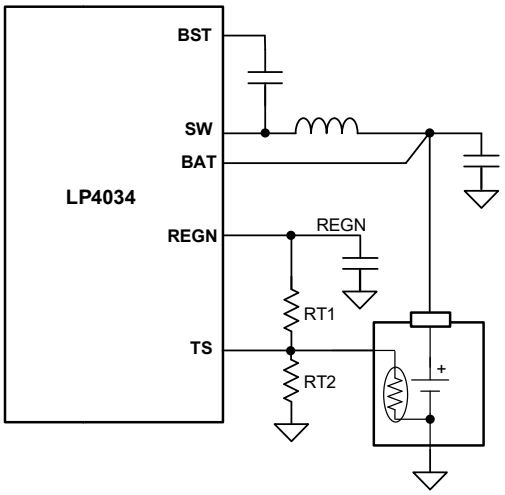


Figure 10. Battery Temperature Monitoring

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T3} \times \left(\frac{1}{V_{T3}\%} - \frac{1}{V_{T1}\%}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}\%} - 1\right) - R_{NTC,T3} \times \left(\frac{1}{V_{T3}\%} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{T1}\%} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (2)$$

Fault Mode

Any fault below triggers the charger into fault mode:

- Input OVP
- TS Cold/Hot
- Thermal Shutdown
- Safety timer expiration

In fault mode, the charger stops charging and STAT pin blinks. For any faults other than safety timer expiration, the safety timer continues counting until safety timer expires. In fault mode, REGN LDO keeps on and RBFET Q1 is off. Once a fault is cleared, the charger goes back to charge mode if charge conditions are met. The converter goes through soft-start process when going back to charge mode from a fault mode.

ISET Pin Open and Short

To protect against ISET pin open and short, the charger immediately shuts off once ISET pin is open or short to GND. ISET pin can be used as enable input for charge enable or disable. If ISET pin is pulled higher than 1.3V, charge is disabled as well. When ISET pin is released from open or short or pulled-high, the charger goes through soft-start process.

Charge Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 20 hours when the battery voltage is above VBAT_LOWV threshold and 2 hours below VBAT_LOWV threshold. When the safety timer expires, charge is suspended. Safety timer is reset and starts to count each time when charge conditions are met. From the fault mode, one of the following conditions can enable charge and reset safety timer.

• Battery voltage falls below recharge threshold

• VBUS voltage is recycled

• ISET pin is released from ISET short, open or pulled-high conditions

If the safety timer expires, the charger goes into fault mode and STAT starts blinking. If any faults other than safety timer expiration cause the charger going into fault mode, STAT starts blinking and safety timer continue counting until safety timer expires if a fault stays valid. If a fault is cleared, the charger is out of fault mode and the safety timer continues counting.

Input Over Voltage Protection

The device integrates the functionality of an input over-voltage protection (OVP). The input OVP threshold is $V_{VBUS\_OVP\_RISE}$. During an input over-voltage event, the charger is disabled and goes into fault mode.

Input Voltage Dynamic Power Management (VINDPM)

When the input current of the device exceeds the current capability of the power supply, the charger device regulates PMID voltage by reducing charge current to avoid crashing the input power supply. VINDPM dynamically tracks the battery voltage. The actual VINDPM regulation is the higher of VINDPM_MIN and (VBAT + 250mV). To charge a battery, the input voltage must be higher than actual VINDPM threshold.

Thermal Regulation (TREG)

The device monitors the junction temperature TJ to avoid overheating the chip and limit the device surface temperature. When the internal junction temperature exceeds thermal regulation limit TREG, the device lowers down the charge current. During thermal regulation, the average charging current is usually below the programmed battery charging current. In thermal regulation, termination is temporarily disabled but safety timer continues counting.

Thermal Shutdown (TSHUT)

The devices have thermal shutdown built in to turn off the charger when device junction temperature exceeds TSHUT. The charger is re-enabled when the junction temperature is 25°C below TSHUT. During thermal shutdown, charge is suspended and the charger goes into fault mode.

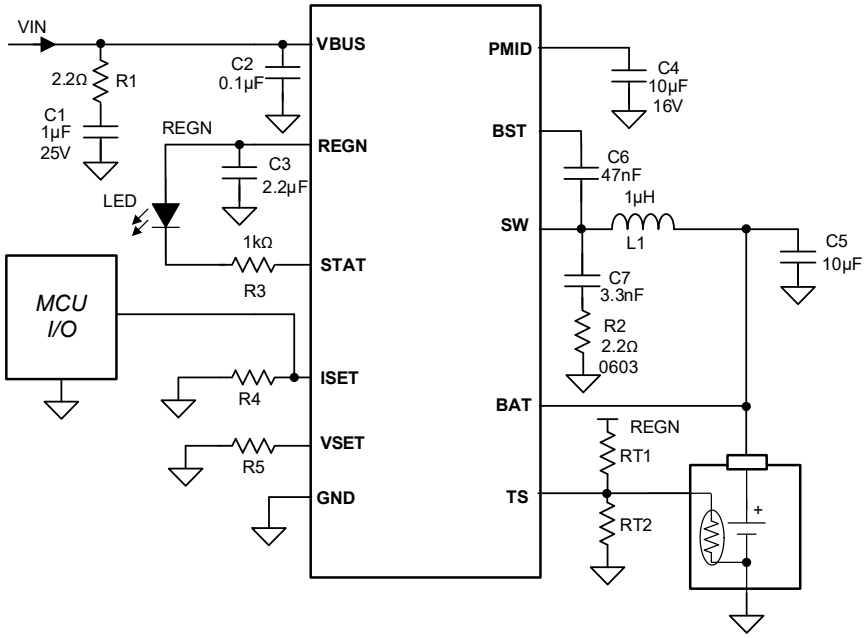
Application and Implementation

Application Information

The device can be used for general purpose high efficiency fast charger. The charge voltage can be programmable by a resistor from VSET pin to GND and charge current is programmable by a resistor from ISET pin to GND. The charge can be enabled or disabled by a MCU GPIO port.

To achieve best EMI performance, a 0.1μF capacitor C2 and a snubber capacitor C7 and snubber resistor R2 are recommended. The PMID capacitor C4 selection and layout are very critical for the charger performance. Considering capacitance decreasing with higher voltage bias, a 16V/10μF X5R ceramic capacitor or two 10V/10μF X5R capacitors shall be placed close to PMID pin and routed to GND with shortest wide path on PCB.

Application Schematic



Designator	Values	Part Number(s)	Manufacturer	Package Size	Specifications
C1	1 μF ±10%	GRM155R61E105KA12D	Murata	0402	Ceramic, X5R, 25V
C3	2.2 μF ±10%	GRM188R71A225KE15D	Murata	0603	Ceramic, X5R, 10V
C4, C5	10 μF ±10%	GRM188R61C106MA73	Murata	0603	Ceramic, X5R, 16V
	22μF ±10%	GMC04X5R226M6R3NT	Murata	0402	Ceramic, X5R, 6.3V
L1	1 μH ±20%	MPIM252010F1R0M-LF	Microgate	2.5x2.0x1.0	Irate=3.2A, DCR=28mΩ
L1	1 μH ±20%	CMLB041B-1R0MS	Cyntec	4.75x4.45x1.2	Irate=5.0A, DCR=42mΩ

Figure 11: Typical Applications Schematic

Charge Voltage Setting

Battery charge voltage is programmed by a resistor connected at the VSET pin. When the REGN LDO startup conditions are met, and before the REGN LDO powers up, the internal VSET detection circuit is enabled to detect VSET pin resistance and set battery charge voltage accordingly. The VSET detection circuit is disabled after detection is complete and changing resistance values on the fly does not change the battery charge voltage for charge safety. VSET detection is re-enabled once the REGN LDO is recycled.

Charge Current Setting

The charger current is set by the resistor value at the ISET pin according to the equation below:

$$I_{CHG}\ (A) = K_{ICHG}\ (A \cdot k\Omega) / RISET(k\Omega) \quad (3)$$

K_{ICHG} is current setting gain that is listed in Electrical Characteristics table and RISET is the resistor value from ISET pin to GND. K_{ICHG} is typically 40 (A·kΩ) and the typical values vs. charge currents are illustrated in Figure 8 in Typical Characteristics.

Application and Implementation (Continued)

Application Curves

(Schematic as shown in Figure 11)

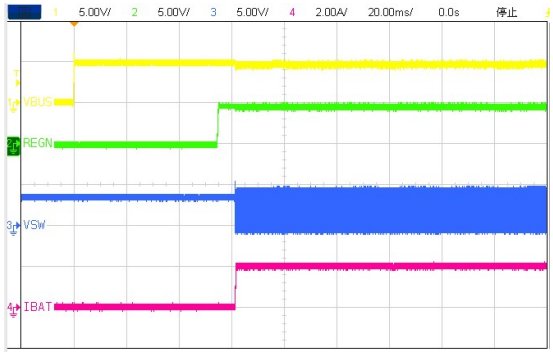


Figure 12. Startup from VBUS
(V_{VBUS}=5V, V_{BAT}=3.8V, I_{CHG}=2A)

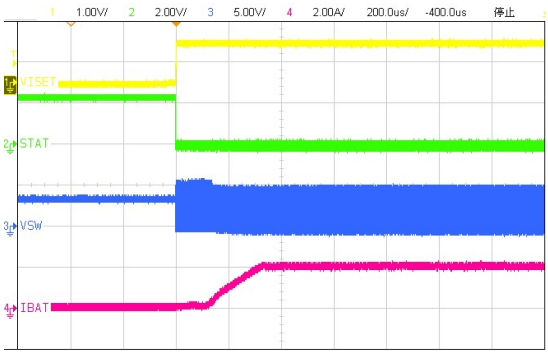


Figure 13. ISET Released from Short
(V_{VBUS}=5V, V_{BAT}=3.8V, I_{CHG}=2A)

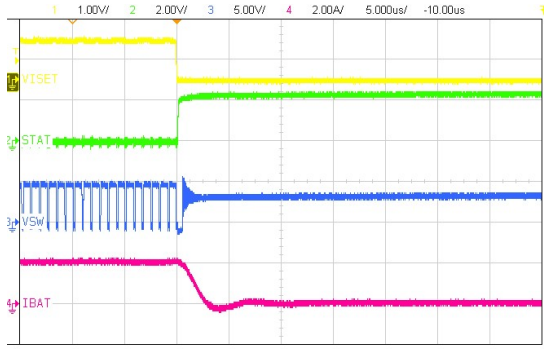


Figure 14. ISET Short
(V_{VBUS}=5V, V_{BAT}=3.8V, I_{CHG}=2A)

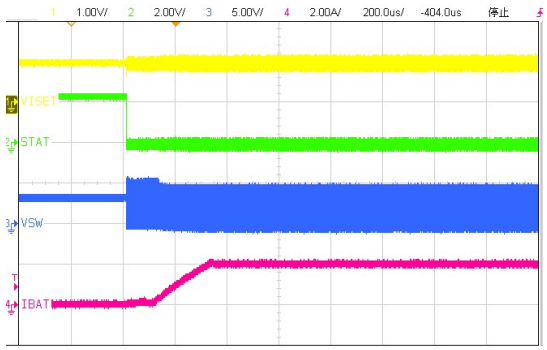


Figure 15. RISET Pulled to GND from Floating
(V_{VBUS}=5V, V_{BAT}=3.8V, I_{CHG}=2A)

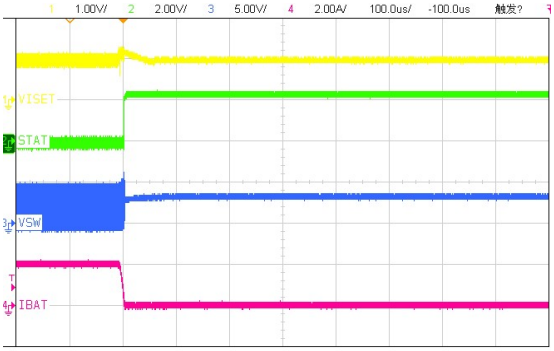


Figure 16. RISET Floated from GND
(V_{VBUS}=5V, V_{BAT}=3.8V, I_{CHG}=2A)

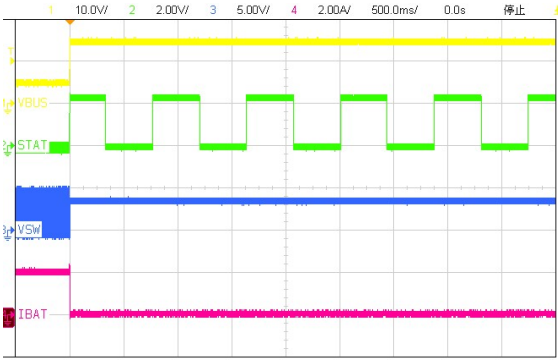


Figure 17. Input Over Voltage
(V_{VBUS}=5V to 15V, V_{BAT}=3.8V, I_{CHG}=2A)

PCB Layout Guideline

Appropriate PCB layout is important in the power supply design. Good PCB layout minimizes EMI and noises, allows good output voltage regulation and achieves higher efficiency. The following design considerations are recommended:

- Using a ceramic capacitor to decouple PMID pins to GND on top layer or through GND copper plane with short and wide copper path.
- Decouple VBUS and REGN pins to GND on top layer and place decoupling capacitors as close to those pins as possible. Always avoid vias if possible because they have parasitic inductance and resistance. If vias are inevitable, always use more than one vias in parallel to decrease parasitics for power traces.
- Connect GND pad to the ground plane on the bottom side with multiple vias that is for both heat dissipation and electrical connection.
- Minimize switching SW node size and trace lengths and keep it away from ISET and BAT traces.
- An example of 20mmx10mm 2-layer PCB layout is shown in Figure 18.

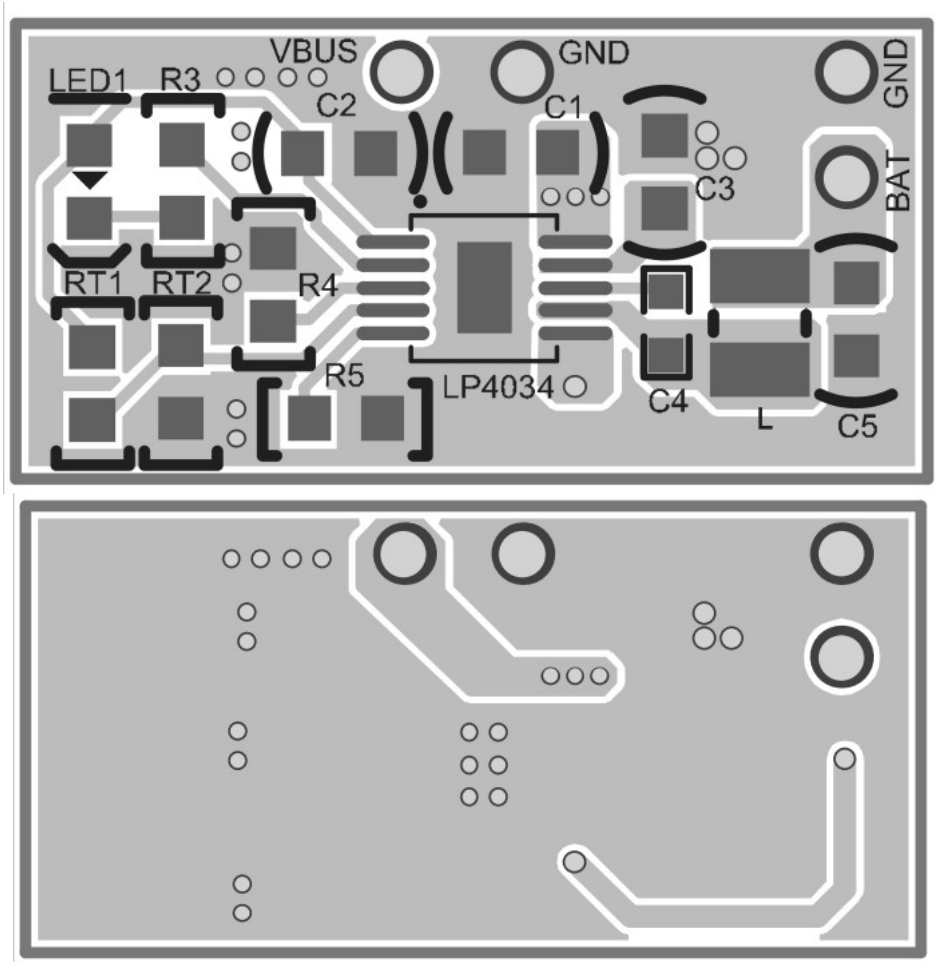
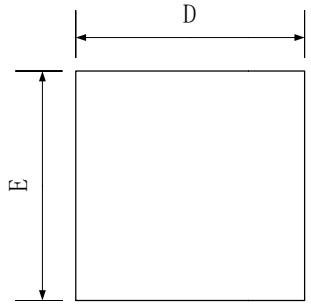


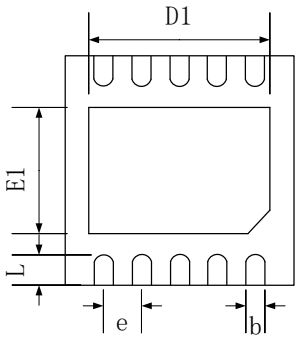
Figure 18. 2-layer PCB Layout Example

Packaging Information

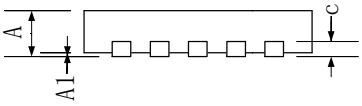
DFN-10



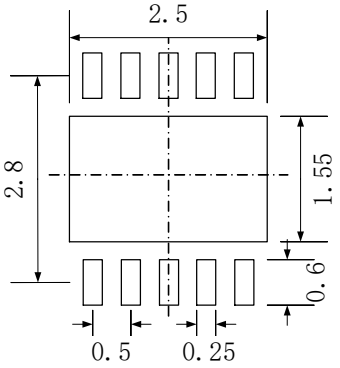
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
B	0.18	0.25	0.30
C		0.20 REF	
D	2.90	3.00	3.10
D1	2.40	2.50	2.60
E	2.90	3.00	3.10
E1	1.45	1.55	1.65
E		0.50 BSC	
L	0.30	0.40	0.50

Revision	Date	Change Description
Rev 0.6	12/25/2023	Initial Release
Rev 0.7	2/27/2024	RT1=4.52kΩ, RT2=23.2 kΩ on Page 14
Rev 0.8	7/27/2024	Update Figure 11 and application circuit on 1st page
Rev. 0.9	12/25/2024	VSET option update
Rev. 0.91	3/1/2025	Add LP4034QVF-445 part number
Rev. 1.0	06/06/2025	Remove watermark