LP3984H

High PSRR Fast Transient Response LDO

Features

- Wide Input Voltage Range: 2.0V to 6.0V
- Adjustable Output Voltage: 0.8V to 5.0V
- Fixed Output Voltage: 1.2, 1.5, 1.8, 2.5, 2.8, 3.0, 3.3V
- Maximum Load Current Up to 600mA
- High PSRR: 82dB@1kHz, V_{OUT}=3.3V
- Low Quiescent Current: 75μA
- Low Noise: 100μV_{RMS}@V_{OUT}=2.8V
- Low Dropout Voltage:
  - 70mV @ 100mA Load, V_{OUT}=3.3V
  - 210mV @ 300mA Load, V_{OUT}=3.3V
  - 430mV @ 600mA Load, V_{OUT}=3.3V
- Output Voltage Accuracy: ±2% @ 1mA typical
- Thermal Shutdown Protection
- Excellent Load/Line Transient Response
- Line Regulation: 0.01%/V typical
- Load Regulation: 30mV typical
- Robust ESD capability:
  - Human Body Model: 2kV
  - Charged Device Model: 1kV
- Package: SOT23-5, DFN1x1-4
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Digital cameras
- Audio devices
- Set-top Box
- Television
- WIFI
- Portable and battery-powered equipment
- Post regulation

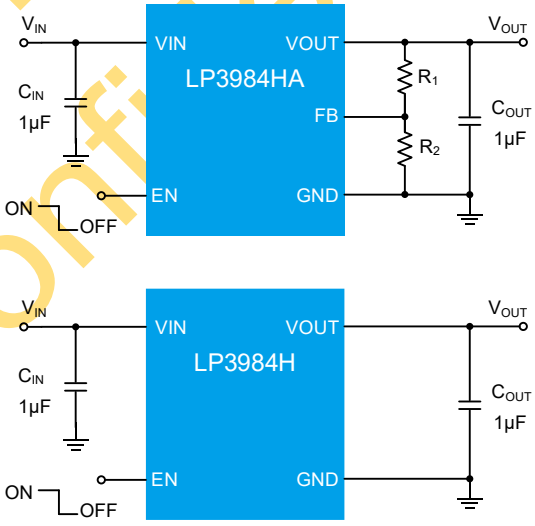
General Description

The LP3984H family are high performance low dropout（LDO）voltage regulators with high PSRR, fast transient response, and high accuracy. The devices with advanced CMOS process are suitable for many applications that require regulated supplies of up to 600mA load current.

The LP3984H family include standard fixed voltage of 1.2V, 1.5V, 1.8V, 2.5V, 2.8V, 3.0V, 3.3V and adjustable output voltages of 0.8V to 5.0V with an external resister divider. The devices are stable with a 1.0μF or greater ceramic output capacitor. The devices are protected from short circuit by a current limit function and from over-heating by a thermal overload protection.

The devices are available in standard DFN-4 (1mmx1mm) and SOT23-5 packages.

Typical Application Circuit



Order Information

LP3984H-□□ □□ □

- OUT Voltage
  - A: Adjustable
  - 12: 1.2V
  - 15: 1.5V
  - 18: 1.8V
  - 25: 2.5V
  - 28: 2.8V
  - 30: 3.0V
  - 33: 3.3V
- Package Type
  - B5: SOT23-5
  - QV: DFN-4
- F: Pb Free

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Device Information

Part Number	Top Marking	OUT Voltage	Moisture Sensitivity Level	Package	Shipping
LP3984HAB5F	LPS 4AYWX	Adjustable	MSL3	SOT23-5	3K/REEL
LP3984H-12B5F	LPS 4BYWX	1.2V	MSL3	SOT23-5	3K/REEL
LP3984H-15B5F	LPS 4NYWX	1.5V	MSL3	SOT23-5	3K/REEL
LP3984H-18B5F	LPS 4CYWX	1.8V	MSL3	SOT23-5	3K/REEL
LP3984H-25B5F	LPS 4DYWX	2.5V	MSL3	SOT23-5	3K/REEL
LP3984H-28B5F	LPS 4HYWX	2.8V	MSL3	SOT23-5	3K/REEL
LP3984H-30B5F	LPS 4GYWX	3.0V	MSL3	SOT23-5	3K/REEL
LP3984H-33B5F	LPS 4EYWX	3.3V	MSL3	SOT23-5	3K/REEL
LP3984H-12QVF	4BW	1.2V	MSL3	DFN1x1-4	12K/REEL
LP3984H-18QVF	4CW	1.8V	MSL3	DFN1x1-4	12K/REEL
LP3984H-28QVF	4HW	2.8V	MSL3	DFN1x1-4	12K/REEL
LP3984H-30QVF	4GW	3.0V	MSL3	DFN1x1-4	12K/REEL
LP3984H-33QVF	4EW	3.3V	MSL3	DFN1x1-4	12K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

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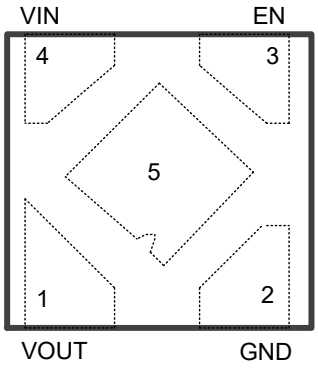
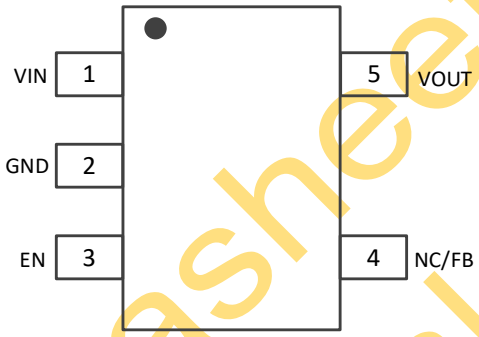
Pin Diagram



DFN1x1-4（top view）



SOT23-5（top view）

Pin Description

Pin		Name	Description
DFN-4	SOT23-5		
1	5	VOUT	Output pin. Bypass with a 1μF or greater ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin as possible.
2	2	GND	Ground.
3	3	EN	Enable pin. Active high. Driving EN over 1V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode.
4	1	VIN	Supply input pin. Must be closely decoupled to GND with a 1μF or greater ceramic capacitor. Place the capacitor as close as to the pin as possible.
	4	NC/FB	No connection. / Feedback pin. Adjustable version only. This is used to set the output voltage. The reference voltage is 0.8V.

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Absolute Maximum Ratings (Note 1)

VIN Pin to GND ---------- -0.3~6.5V
VOUT, EN, FB Pin to GND ---------- -0.3~V_{IN}
Maximum Junction Temperature (T_J) ---------- 150℃
Operating Ambient Temperature Range (T_A) ---------- -40℃ to 85℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
Storage Temperature range(T_{STG}) ---------- -65℃ to 125℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Thermal Information

Thermal Resistance (DFN-4, θ_{JA}) (Note 2) ---------- 256 °C/W
Thermal Resistance (SOT23-5, θ_{JA}) (Note 2) ---------- 203 °C/W
Thermal Resistance (DFN-4, θ_{JC}) (Note 2) ---------- 105 °C/W
Thermal Resistance (SOT23-5, θ_{JC}) (Note 2) ---------- 55 °C/W

Note 2. Measured using 2S2P JEDEC standard PCB with ambient temperature < 25°C

ESD Susceptibility

HBM (Human Body Model) ---------- 2kV
CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions

Input Voltage ---------- 2.0 V to 6.0V
Operating Junction Temperature Range (T_J) ----------40℃ to 150℃
Ambient Temperature Range ---------- -40℃ to 85℃

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Electrical Characteristics

(The specifications are at T_A=25℃, V_{IN} = V_{FB}*(1+R_1/R_2)+1V, R_1=160kΩ, R_2=51kΩ, C_{IN}=C_{OUT}=1μF, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT							
V_{IN}	Input Voltage Operation Range			2		6	V
I_Q	DC Supply Quiescent Current	V_{EN}=V_{IN}, I_{LOAD}=0mA			75	100	μA
I_{SD}	Shutdown Current	V_{EN}=0V			0.4	1	μA
OUTPUT VOLTAGE AND CURRENT							
V_{OUT}	Output Voltage Accuracy	I_{LOAD}=1mA		-2%		2%	
V_{FB}	FB Voltage	I_{LOAD}=1mA		0.784	0.8	0.816	V
$\frac{\Delta V_{LINE}}{\Delta V_{IN} \times V_{OUT}}$	Output Voltage Line Regulation	V_{IN}=V_{OUT}+0.5V~6V I_{LOAD}=1mA			0.02		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{LOAD} from 1mA to 600mA			30		mV
I_{OUT_MAX}	Max Load Current	V_{EN}=V_{IN}			600		mA
I_{LIMIT}	Load Current Limit	V_{OUT}=0.9*$V_{OUT(Nom)}$		620	720		mA
I_{SHORT}	Short Current Limit	V_{OUT} short to GND			65		mA
V_{DROP}	Dropout Voltage	V_{OUT}=3.3V, I_{LOAD}=100mA			70		mV
		V_{OUT}=3.3V, I_{LOAD}=300mA			210		mV
		V_{OUT}=3.3V, I_{LOAD}=600mA			430		mV
e_N	Output Noise	10Hz to 100kHz, V_{OUT}=3.3V, I_{LOAD}=20mA			115		μV_{RMS}
		10Hz to 100kHz, V_{OUT}=2.8V, I_{LOAD}=20mA			100		μV_{RMS}
		10Hz to 100kHz, V_{OUT}=1.8V, I_{LOAD}=20mA			75		μV_{RMS}
		10Hz to 100kHz, V_{OUT}=1.2V, I_{LOAD}=20mA			60		μV_{RMS}
PSRR	Power Supply Rejection Ratio	V_{IN}=(V_{OUT}+1V)$_{DC}$+0.2V_{P-P}, I_{OUT}=20mA, V_{OUT}=3.3V	f=1kHz		82		dB
			f=10kHz		68		
			f=100kHz		49		
R_{DIS}	Auto-Discharge Resistance				130		Ω
THERMAL SHUTDOWN							
T_{SD}	Thermal Shutdown Threshold				160		℃
T_{SD_HYS}	Thermal Shutdown Hysteresis				20		℃
EN LOGIC							
V_{ENH}	EN Logic High Voltage			1.0			V
V_{ENL}	EN Logic Low Voltage					0.4	V
I_{EN}	EN Input Current	VEN=0 to 5.5V			120		nA

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Typical Characteristics

(T_J = 25℃, LP3984HA, V_{IN} = V_{FB}*(1+R_1/R_2)+1V, R_1=160kΩ, R_2=51kΩ, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1.0μF, unless otherwise noted.)

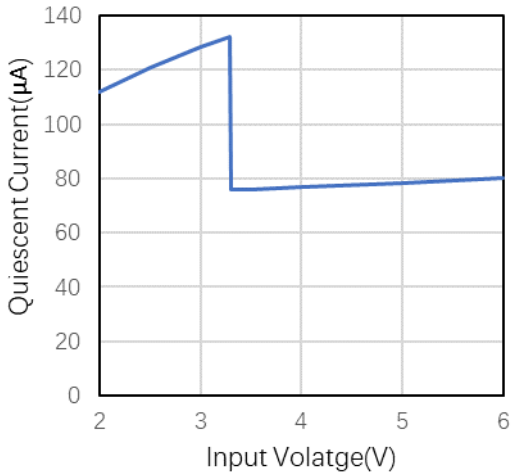

Figure 1 Quiescent Current vs Input Voltage,

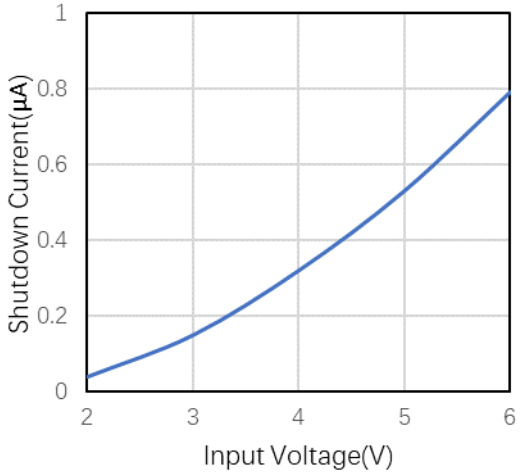

Figure 2. Dropout Voltage vs Output Current

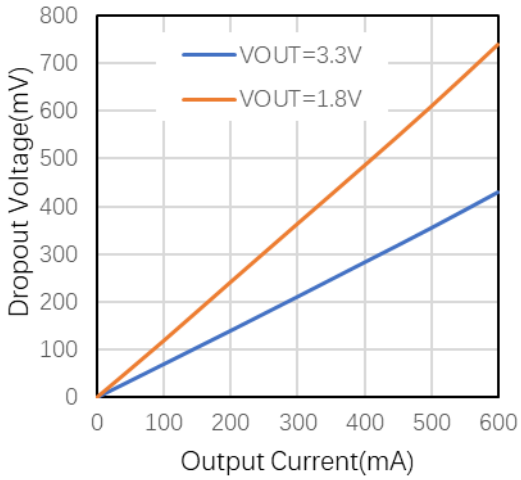

Figure 3 Dropout Voltage vs Output Current

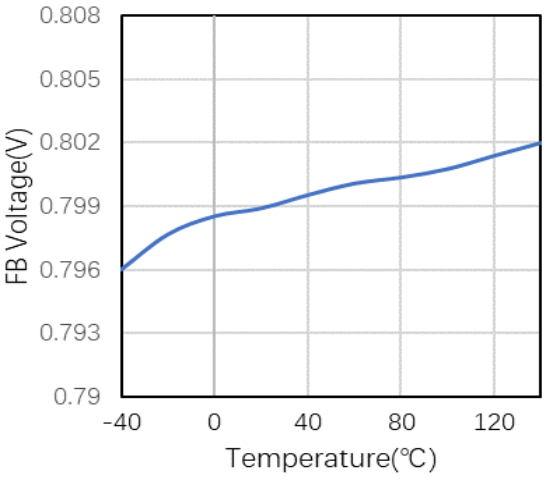

Figure 4 FB Voltage vs Temperature

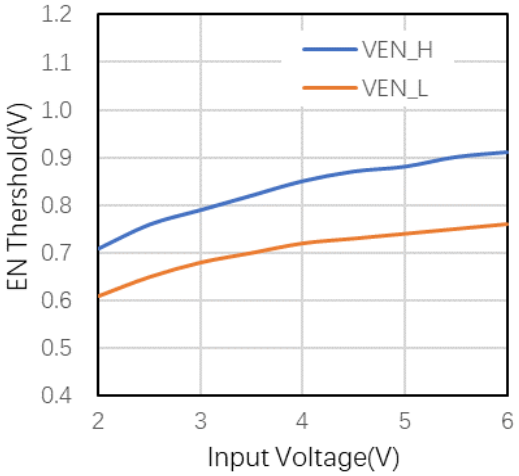

Figure 5 EN Threshold vs Input Voltage

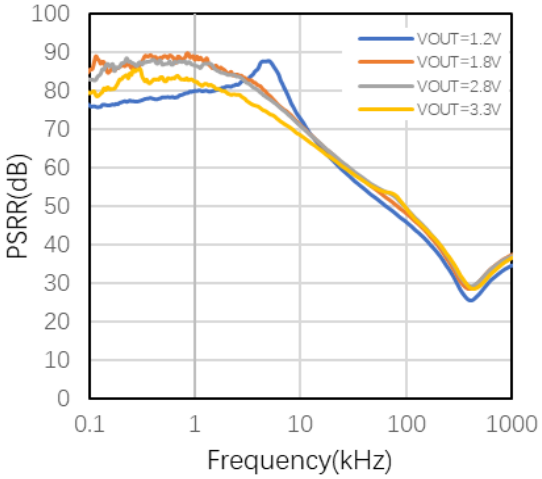

Figure 6 PSRR vs Frequency，I_{OUT}=20mA

Typical Characteristics(continued)

(T_J = 25℃, LP3984HA, V_{IN} = V_{FB}*(1+R_1/R_2)+1V, R_1=160kΩ, R_2=51kΩ, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1.0μF, unless otherwise noted.)

Start up and Turn off with EN:(I_{OUT}=1mA)

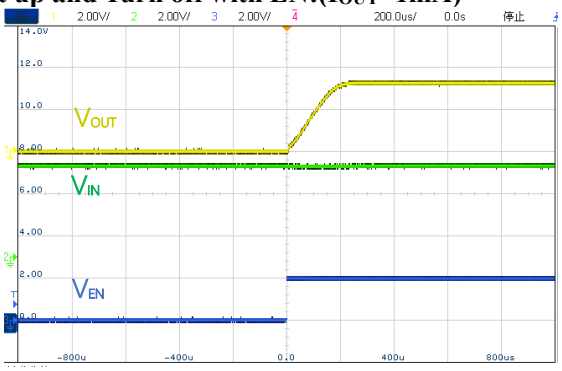

Figure 7 Start up with EN on

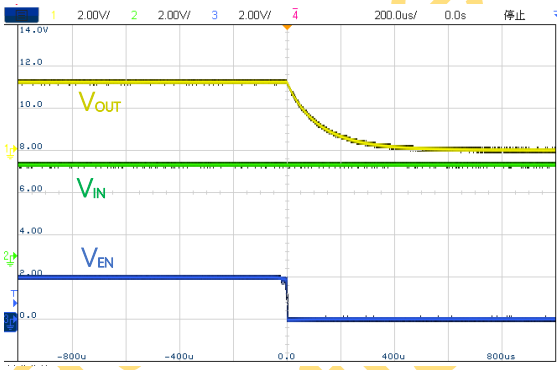

Figure 8 Turn off with EN off

Line Transient: V_{IN}=3.8V <->5V

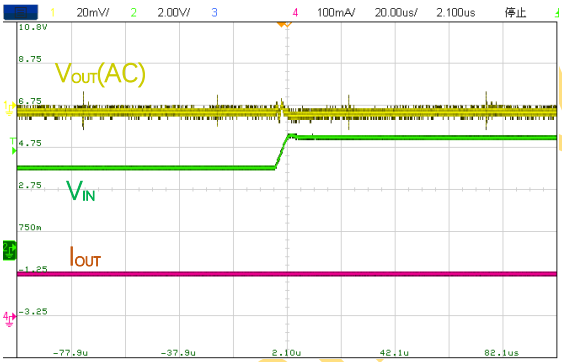

Figure 9. Line Transient V_{IN}=3.8V-> 5V

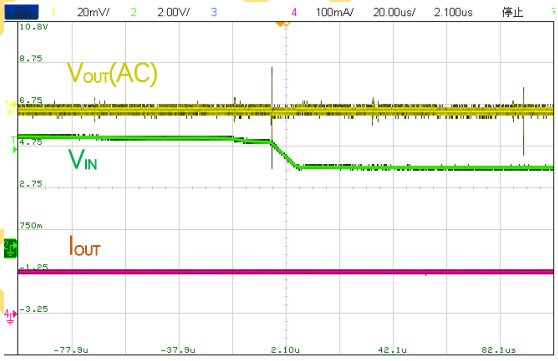

Figure 10. Line Transient V_{IN}=5V-> 3.8V

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Typical Characteristics(continued)

(T_J = 25℃, LP3984HA, V_{IN} = V_{FB}*(1+R_1/R_2)+1V, R_1=160kΩ, R_2=51kΩ, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1.0μF, unless otherwise noted.)

Load Transient: I_{OUT}=1mA <->100mA in 1μs

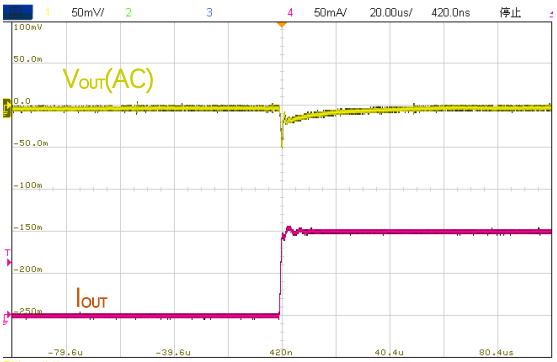

Figure 11. Load Transient 1mA->100mA, V_{IN}=4.3V, V_{OUT}=3.3V

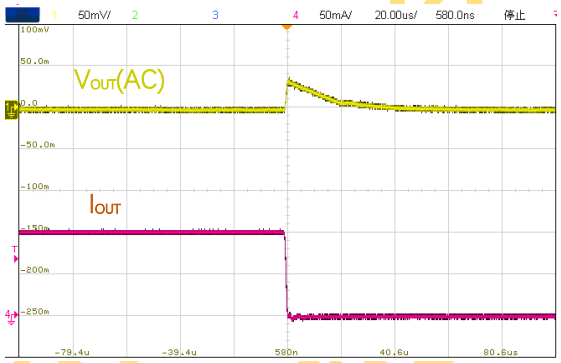

Figure 12. Load Transient 100mA->1mA, V_{IN}=4.3V, V_{OUT}=3.3V

Load Transient: I_{OUT}=1mA <->300mA in 1μs

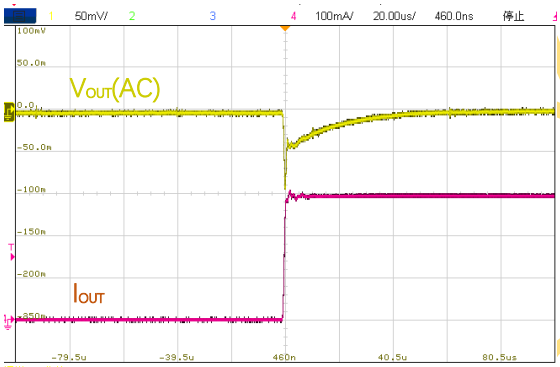

Figure 13. Load Transient 1mA->300mA, V_{IN}=4.3V, V_{OUT}=3.3V

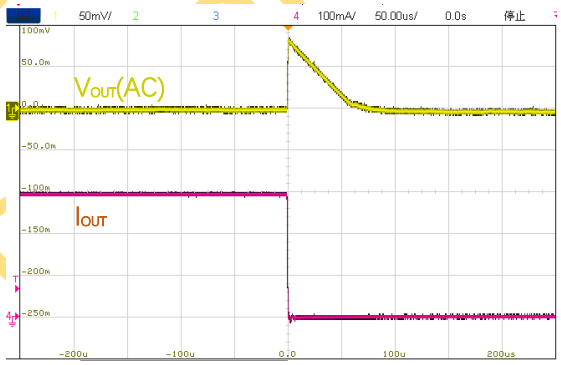

Figure 14. Load Transient 300mA->1mA, V_{IN}=4.3V, V_{OUT}=3.3V

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Functional Block Diagram

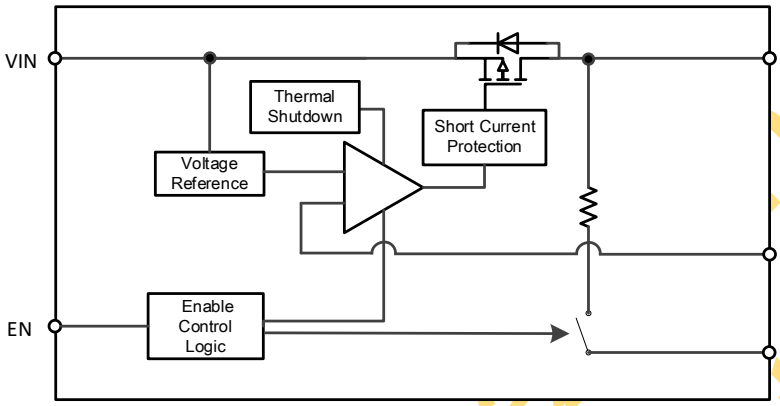

Figure 15. LP3984HA functional block diagram

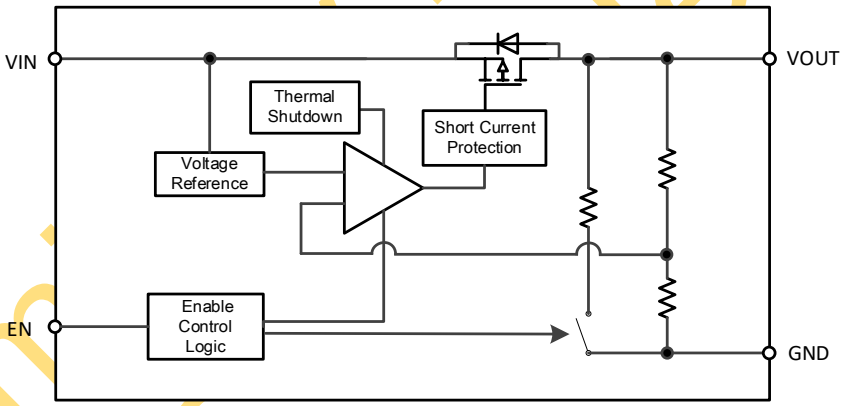

Figure 16. LP3984H-XX functional block diagram

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Detailed Description

Overview

The LP3984H family are high performance, low dropout linear regulators with fixed 1.2V to 3.3V output voltages or adjustable voltage of 0.8V to 5.0V and up to 600 mA output current capability. Optimized for using with ceramic capacitors, the device provides excellent transient performance and suitable for powering digital circuits.

Internally, the devices consist of a voltage reference, an enable control logic, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares a reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

Adjustable Output Voltage

LP3984HA output voltage is adjustable, which is programmed by an external resistor divider. The output can be calculated be by the following equation:

$$V_{OUT}= (1+ R_1/ R_2) \times V_{REF}$$

Where V_{REF} is the internal reference voltage, which is 0.8V in LP3984HA. It recommends R2 resistance ranges from 10kΩ to 100kΩ.

Enable Function

The EN pin is a high active logic input pin. The internal power element is turned off when EN pin is tied low. When the EN pin is pulled high or left floating, the LP3984H will be activated and output voltage according to the setting.

Auto Discharge

The LP3984H has a quick discharge function. When the device is disabled by the pulled-down EN pin, a discharge resistor is connected between VOUT and GND. The resistance is 130Ω typically.

Short Current Limit Protection

When the output current at the VOUT pin is higher than current limit threshold or the VOUT pin is short to GND, the short current limit protection will be triggered and clamp the output current to approximately 100mA to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

When the internal junction temperature of LP3984H family devices exceed the junction thermal shutdown threshold (160℃ typical), the devices will shut down the output, after the junction temperature falls below 140℃ , the VOUT voltage will resume.

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Application Description

Thermal Consideration

The reason that causes thermal shutdown protection of an LP3984H device is the power dissipation. Nearly all of the power dissipation is generated by the internal PMOS pass device. The power dissipation can be calculated approximately as,

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

where P_D is the power dissipation.

For example, when the device has an input voltage of 5.5V, an output voltage of 1.2V, and the load current of 300mA. In this situation, the device dissipates the power calculated as below,

$$P_D = (5.5V - 1.2V) \times 300mA = 1.29W$$

This power dissipation of the LDO device in the SOT23-5 or DFN-4 package will trigger thermal shutdown protection at high ambient temperature. Then a trade-off must be made between the output current, cost, and thermal requirements of the application.

Input Capacitor

Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. A 1μF-10uF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitches and noise. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

The LP3984H requires a minimum output capacitance of 1μF for output voltage stability. The recommended output capacitance is from 1μF to 10μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitor should be located as close to the LDO output as practically possible.

Layout Considerations

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practically possible to the respective LDO pins. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible with a wide and component-side copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB, opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device.

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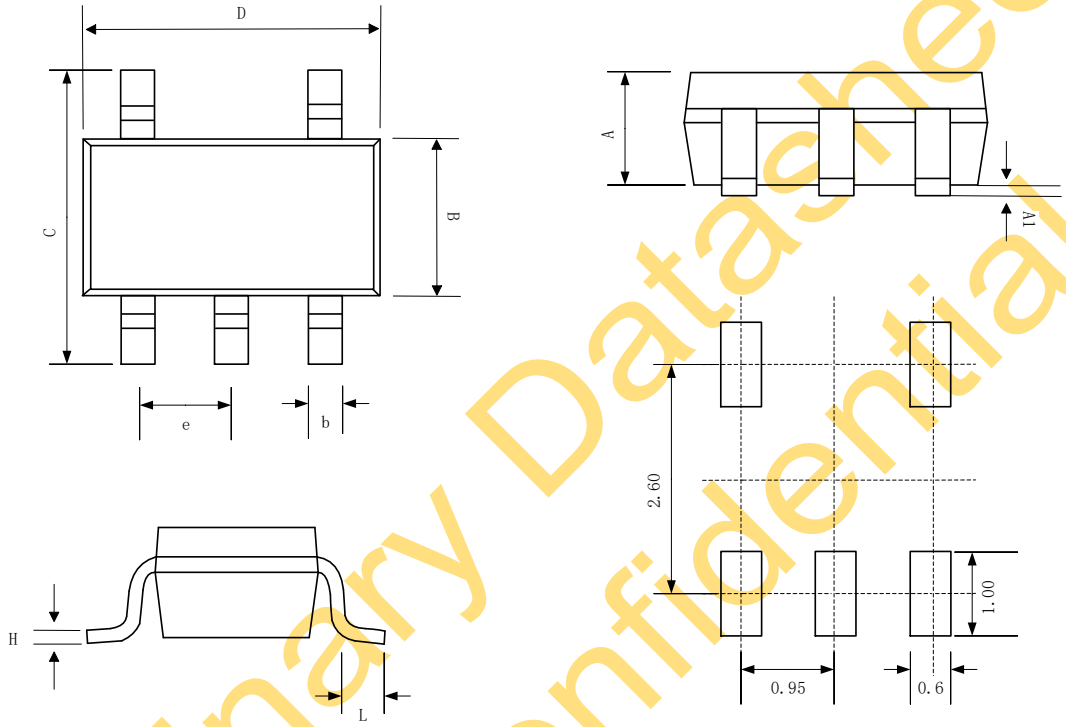
Packaging Information

SOT23-5



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.889	1.100	1.295
A1	0.000	0.050	0.152
B	1.397	1.600	1.803
b	0.28	0.35	0.559
C	2.591	2.800	3.000
D	2.692	2.920	3.120
e	0.95BSC		
H	0.080	0.152	0.254
L	0.300	0.450	0.610

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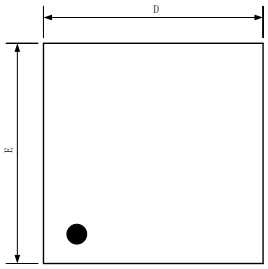
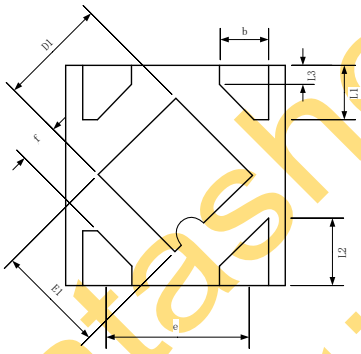
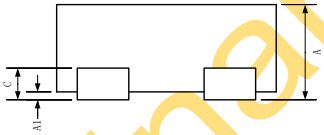
DFN1x1-4



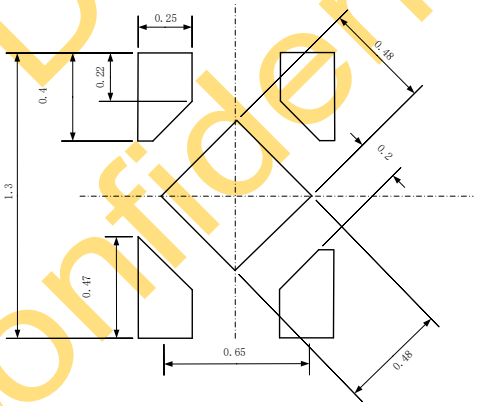
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Recommended Land Pattern

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.35	-	0.50
A1	0.00	0.02	0.05
b	0.20	0.25	0.30
c	0.07	0.12	0.17
D	0.95	1.00	1.05
D1	0.43	0.48	0.55
E	0.95	1.00	1.05
E1	0.43	0.48	0.55
e	0.65BSC		
L1	0.2	0.25	0.30
L2	0.27	0.32	0.37
L3	0.09REF		
f	0.18REF		

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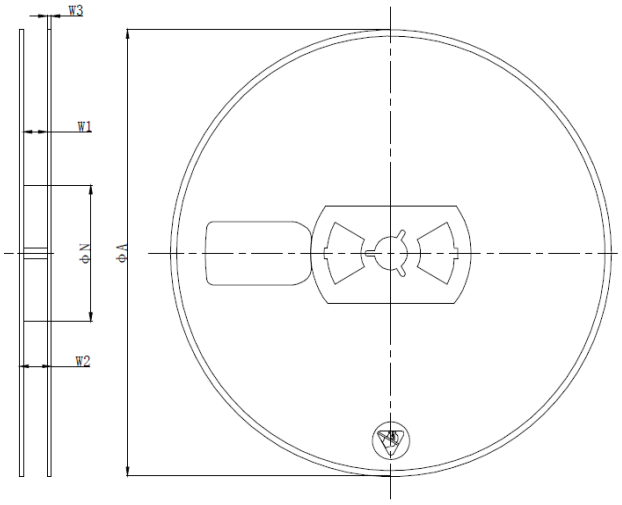
Tape and Reel Information

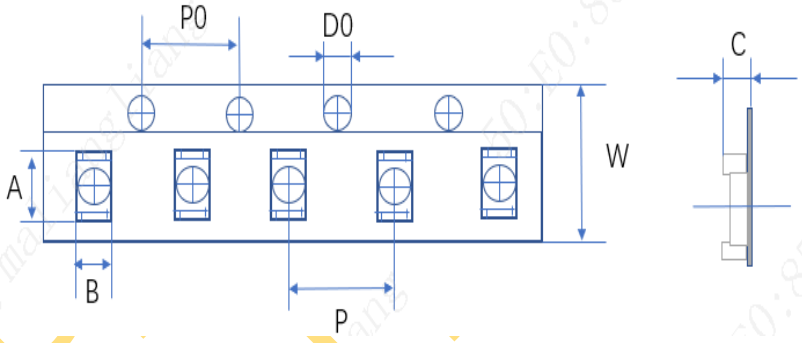
SOT23-5

REEL DIMENSIONS



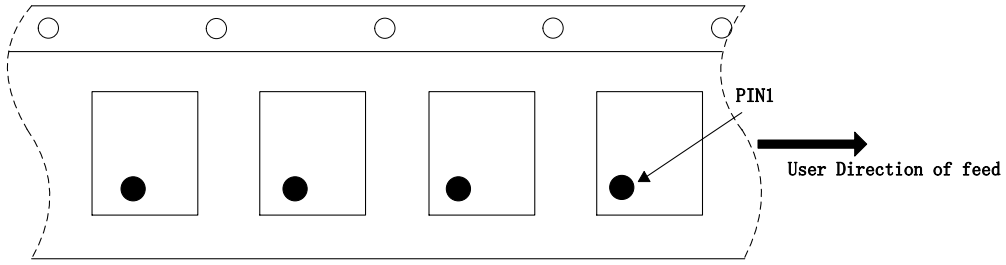
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.00	3.20	3.40
B	3.06	3.26	3.46
P0	3.90	4.00	4.10
P	3.90	4.00	4.10
D0	1.35	1.50	1.65
W	7.70	8.00	8.30
C	1.20	1.40	1.60

PIN1 AND TAPE FEEDING DIRECTION



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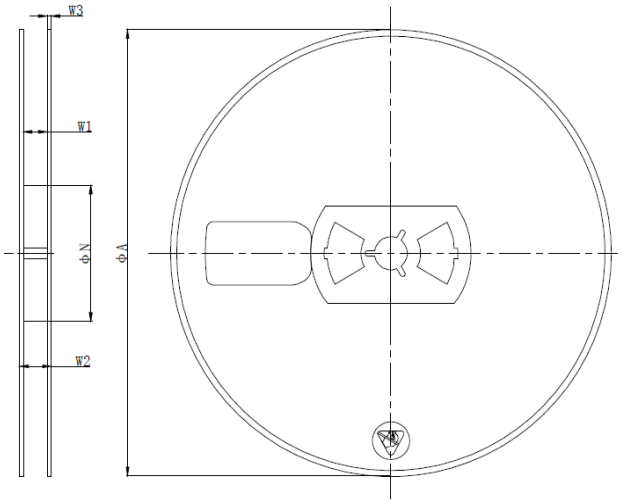
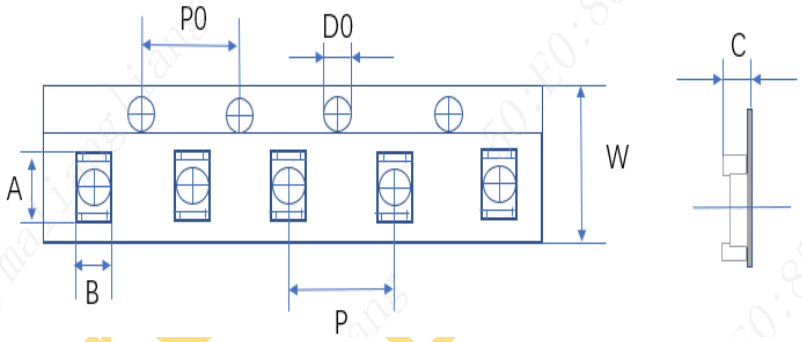
DFN1x1-4

REEL DIMENSIONS



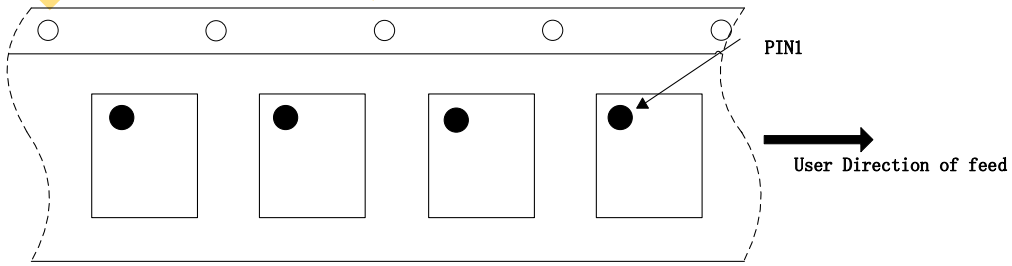
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	176.00	180.00	184.00
W2	10.00	12.00	14.00

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.96	1.16	1.36
B	0.96	1.16	1.36
P0	3.80	4.00	4.20
P	1.80	2.00	2.20
D0	1.30	1.50	1.70
W	7.90	8.00	8.30
C	0.30	0.50	0.70

PIN1 AND TAPE FEEDING DIRECTION



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Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350~2000	Volume mm³ ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

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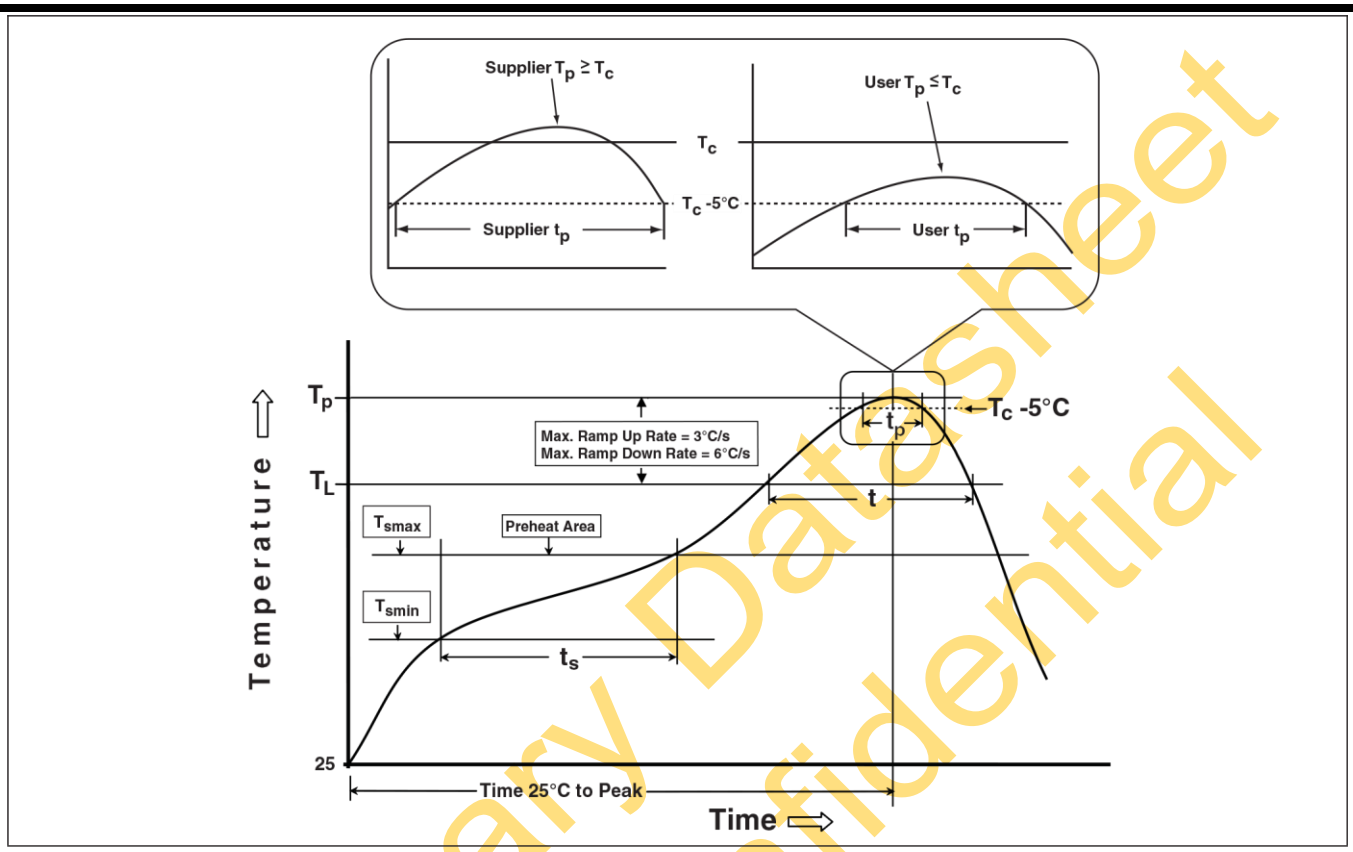

Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;

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