LPQ6512

TFT LCD Integrated Power Module for Automotive

Features

- Input Supply Range : 2.5V ~ 5.5V
- IIC Interface
- Power-on and Power-off Sequence Free
- PAVDD Programmable Output Voltage 5V to 8.15V
- PAVDD Output Current Capability up to 400mA
- NAVDD Programmable Output Voltage -5V to –8.15V
- NAVDD Output Current Capability up to 400mA
- VGH Programmable Output Voltage 7V to 30V
- VGH Output Current Capability up to 60mA
- VGH Output Voltage Temperature Compensation
- VGL Programmable Output Voltage -6V to -18V
- VGL Output Current Capability up to 60mA
- VCOM 8bits Programmable Output Voltage
- Outputs Power-off Discharge Function
- Programmable Voltage Detector
- AEC-Q100 Grade 2 Qualified
- Built in UVLO,UVP,OVP,SCP and OTP Protection
- Compact Package: QFN5X5-32

Applications

- Infotainment LCD PANEL

Order Information

LPQ6512 □ □ □

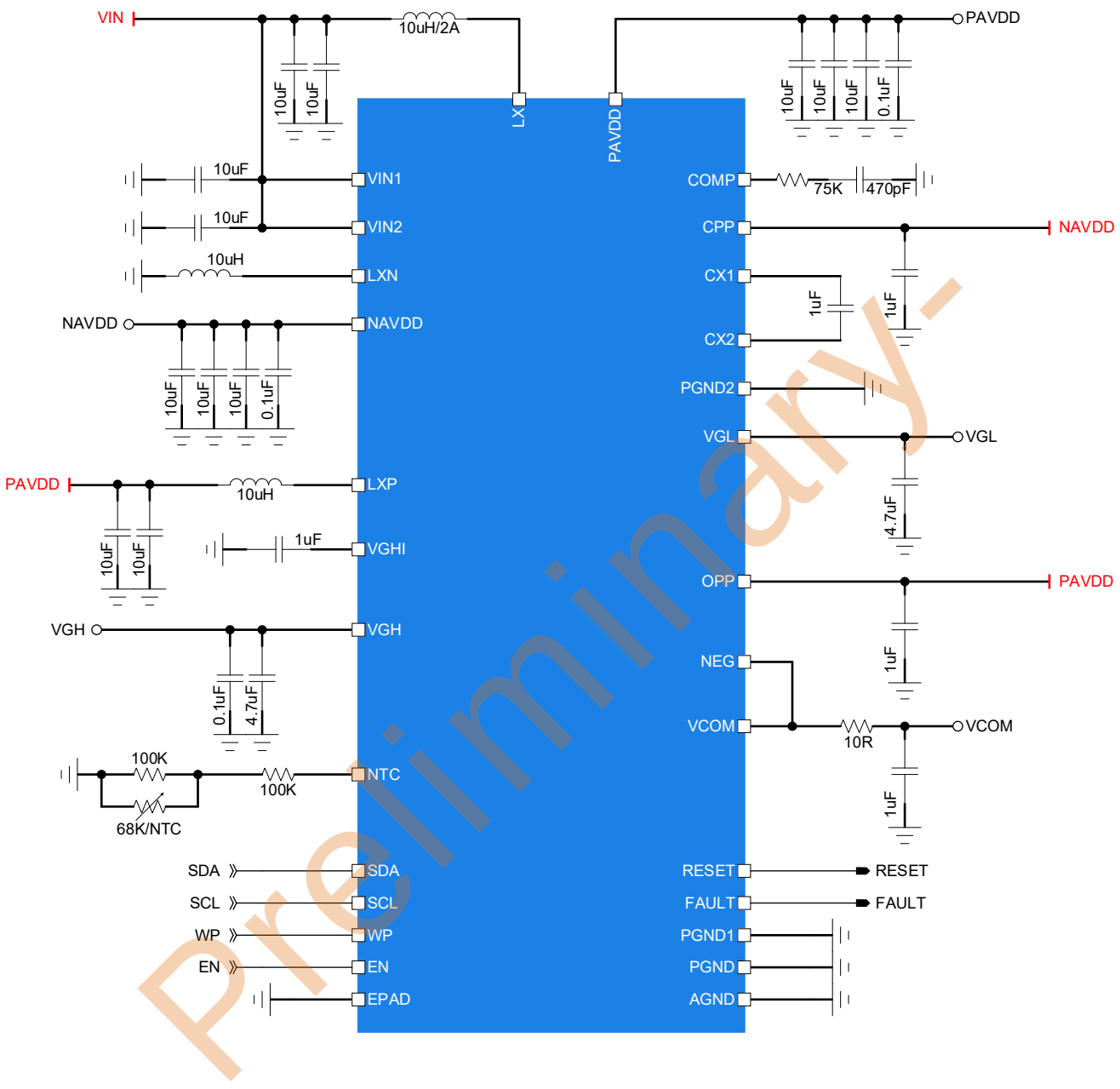
- F:Green
- Package Type
  QV:QFN5X5-32

General Description

The LPQ6512QVF is an I2C interface programmable power management IC. The IC includes two synchronous boost converters for PAVDD and VGH, one synchronous NAVDD buck-boost, one VGL charge pump, one high performance VCOM with 8-bit Calibrator and one RESET voltage detector. With available in a QFN5X5-32 package, this device is suitable for automotive TFT-LCD panel.

The IC can operate from 2.5V to 5.5V input voltages.High switching frequency operation prevent that the switching noise to interfere AM band. Current-limit functions are provided for all internal- switch converters, and output-fault shutdown protects all converters against output-fault conditions, and output the FAULT signal to communicate with automotive computer. Programmable soft-start functions for all output voltage to limit input inrush current during startup.

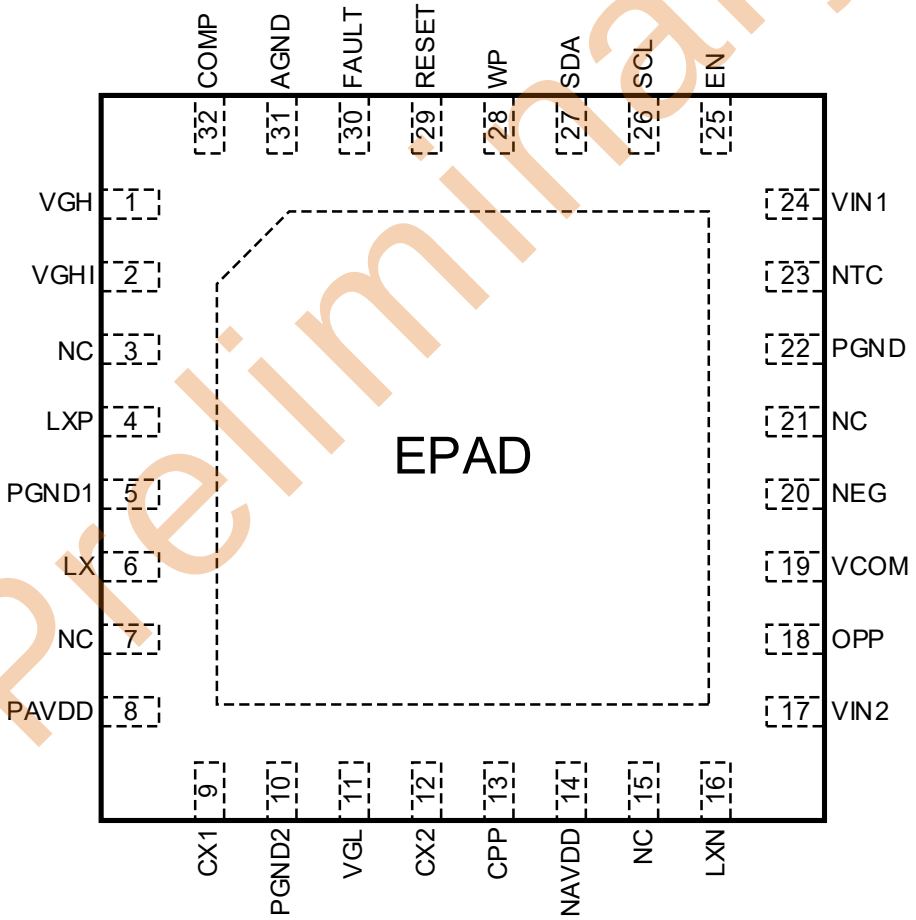
Typical Application Circuit



Device Information

Part Number	Top Marking	Moisture Sensitivity Level	Package	Shipping
LPQ6512QVF	LPS LPQ6512 YWX	MSL3	QFN5X5-32	3K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.				

Pin Diagram



QFN5X5-32

Pin Description

Pin#	Name	Description
1	VGH	VGH boost converter output.
2	VGHI	VGH boost converter output without sequence control. The output is not isolated from input.
3	NC	No internal connection.
4	LXP	Switching node of VGH boost converter.
5	PGND1	Power ground of PAVDD and VGH boost converter.
6	LX	Switching node of PAVDD boost converter.
7	NC	No internal connection.
8	PAVDD	PAVDD boost converter output.
9	CX1	VGL charge pump flying cap node1.
10	PGND2	Power ground of VGL charge pump.
11	VGL	VGL charge pump output.
12	CX2	VGL charge pump flying cap node2.
13	CPP	VGL charge pump power input.
14	NAVDD	NAVDD inverting converter output.
15	NC	No internal connection.
16	LXN	Switching node of NAVDD inverting converter.
17	VIN2	NAVDD supply voltage input.
18	OPP	VCOM OP-AMP positive power supply.
19	VCOM	VCOM OP-AMP output
20	NEG	Inverting input of VCOM calibrator.
21	NC	No internal connection.
22	PGND	Power ground.
23	NTC	Thermistor network connection for temperature compensation.
24	VIN1	IC supply voltage input
25	EN	Enable control input
26	SCL	IIC clock input
27	SDA	IIC data input
28	WP	MTP write protection. When WP=1,MTP is protected, but register still can be written. WP=0, register and MTP can be written.
29	RESET	Output of voltage detection function
30	FAULT	Fault signal output.
31	AGND	Analog ground.
32	COMP	AVDD boost converter compensation input.
33	PGND	The exposed pad must be soldered to a large PCB and connected to PGND for maximum thermal dissipation.

Absolute Maximum Ratings (Note1)

VIN1,VIN2 to PGND ---------- -0.3V to +6V
CPGND,PGND1/2,AGND to GND ---------- -0.3V to +0.3V
COMP,RESET,FAULT,WP,SDA,SCL,EN,NTC to AGND ---------- -0.3V to +6V
LX,PAVDD to PGND ---------- -0.3V to +12V
VIN2 to LXN ---------- -0.3V to +16V
NAVDD to PGND ---------- -12V to +0.3V
PAVDD to CX1 ---------- -0.3V to +12V
CX1 to PGND ---------- -0.3V to +12V
CX2 to CPP ---------- -0.3V to +12V
CX2 to VGL ---------- -0.3V to +20V
CPP to PGND ---------- NAVDD to +0.3V
VGL to PGND ---------- -20V to +0.3V
LXP,VGHI,VGH to PGND ---------- -0.3V to +35V
OPP to VCOM,NEG ---------- -0.3V to +16V
VCOM,NEG to NAVDD ---------- -0.3V to +16V

Note1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings(Note2)

HBM (Human Body Model) ---------- 2KV
MM (Machine Model) ---------- 200V
CDM (Charge Discharge Model) ---------- 500V

Note2: Devices are ESD sensitive. Handling precaution is recommended.

Thermal Information

Junction Temperature (TJ) ---------- 150℃
Operating Junction Temperature Range (TJ) ---------- -40℃ to 125℃
Ambient Temperature Range ---------- -40℃ to 105℃
Storage Temperature Range ---------- -65℃ to 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃
θ_{JA} (Junction-to-Ambient Thermal Resistance) ---------- 27.5℃/W

Recommended Operating Conditions

Over Operating free-air temperature range (unless otherwise noted)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	VIN Supply Range		2.5	3.3	5.5	V
PAVDD	PAVDD output voltage Fosc=2.2MHz	Step:50mV	5.0 Vin+2.2		8.15	V
PAVDD	PAVDD output voltage Fosc<1MHz	Step:50mV	5.0 Vin+1.3		8.15	V
I_{PAVDD}	PAVDD output current ability	VIN=3.3V PAVDD=8.0V	400			mA
NAVDD	NAVDD output voltage	Step:50mV	-5		-8.15	V
I_{NAVDD}	NAVDD output current ability	VIN=3.3V NAVDD=-8.0V	400			mA
VGH_N	VGH output voltage	Step:500mV	7 PAVDD+2		30	V
VGH_LT	VGH low temperature	Step:1V	2		9	V
I_{GH}	VGH output current ability	V_{IN}=3.3V,V_{PAVDD}=6.7V VGH=30V	60			mA
VGL	VGL output voltage	Step:250mV	-18		-6	V
I_{GL}	VGL output current ability	V_{IN}=3.3V,V_{PAVDD}=6.7V V_{NAVDD}=-6.7V VGL=-8V	60			mA
VCOM_C	VCOM_C output voltage	Step:20mV	-3		2	V
VLDO	VLDO output voltage	Step:20mV	0.8		2	V
VCOM_F	VCOM_F	Step:10mV	VCOM_C -1.27V		VCOM_C +1.28V	V

Electrical Characteristics

(VIN = 2.5V to 5.5V, TA=-40℃ to 105℃，unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
GENERAL						
VIN_{OVP}	VIN over voltage protection		6.00	6.25	6.50	V
VIN_{OVP_HYS}	VIN over voltage protection hysteresis		5.75	6.0	6.25	V
VIN	Input Voltage Range		2.5	3.3	5.5	V
$VIN1_{UVLO\_R}$	VIN1 UVLO Rising	VIN1 rising, turn-on IC	2.16	2.33	2.5	V
$VIN1_{UVLO\_F}$	VIN1 UVLO Falling		2.01	2.18	2.35	V
VIN_{Write}	Write to MTP minimum Input voltage		2.8			V
VIN_{IQ}	VIN Total Quiescent Current	VIN=3.3V All output turn on		15	18	mA
$VIN1_{IQ}$	VIN1 Quiescent Current	SW not switching.	0	2	4.5	mA
$VIN1_{IQ}$	VIN1 Quiescent Current	SW switching.		2.35	5	mA
	VIN1 Shutdown Current	EN = Low, VIN1 = 3.3V	0	200	400	uA
VIH	EN/WP input threshold		1.5			V
VIL	EN/WP input threshold				0.8	V
F_{OSC}	Switch Frequency Range		600		2200	KHz
	Switch Frequency Accuracy		-15		+15	%
T_{D_POFF}	Power off delay time	3ms/step,16 steps	0		45	ms
T_{SD}	Thermal shutdown temperature rising		145	155	165	℃
DT_{SD}	Temperature Hysteresis			20		℃
R_{UP}	WP pull up resistor to VIN		80	100	120	KΩ
R_{PD}	EN pull down resistor		320	400	480	KΩ

Electrical Characteristics

(VIN = 2.5V to 5.5V, TA=-40℃ to 105℃，unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PAVDD Sync. Boost Converter						
V_{PAVDD}	PAVDD output voltage range	0.05V/step fosc=2.2MHz	5.0 VIN+2.2		8.15	V
V_{PAVDD}	PAVDD output voltage range	0.05V/step Fosc<1MHz	5.0 or VIN+1.3		8.15	V
	PAVDD output voltage tolerance	TA=25℃, no load	-1		+1	%
	PAVDD output voltage tolerance	TA=-40℃ to 105℃ No load	-2		+2	%
	PAVDD Load Regulation	I_{PAVDD}=0mA to 300mA		100		mV/A
T_{D_PAVDD}	PAVDD on delay time	5ms/step,16 steps	0		75	ms
T_{SS_PAVDD}	PAVDD soft-start time	5ms/step, 8 steps	5		40	ms
	PAVDD Delay/Soft-start time Tolerance		-15		+15	%
$PAVDD_{OFF}$	PAVDD power off delay time	2ms/step,7 steps	0		14	ms
D_{MAX_PAVDD}	PAVDD Maximum Duty		83	90	97	%
I_{LIM_PAVDD}	PAVDD current limit		2.0	2.4	2.8	A
R_{DSON_L}	PAVDD RON Low-side			0.15	0.35	Ω
R_{DSON_H}	PAVDD RON High-side			0.2	0.45	Ω
R_{DIS}	PAVDD power on/off discharge Res			5		Ω
$PAVDD_{SCP}$	PAVDD SCP level		23	30	37	%
$PAVDD_{UVP}$	PAVDD UVP level		62	70	78	%
$PAVDD\_T_{UVP}$	PAVDD UVP Fault Delay Duration to IC shutdown		30	50	70	ms
V_{OVP_PAVDD}	PAVDD OVP voltage percentage	PAVDD rising	110	120	130	%

Electrical Characteristics

(VIN = 2.5V to 5.5V, TA=-40℃ to 105℃，unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
NAVDD Sync. Buck-Boost Converter						
V_{NAVDD}	NAVDD output voltage range	0.05V/step	-5		-8.15	V
	NAVDD output voltage tolerance	TA=25℃, no load	-1		+1	%
	NAVDD output voltage tolerance	TA=-40℃ to 105℃ No load	-2		+2	%
	NAVDD Load Regulation	I_{NAVDD}=0mA to 300mA		100		mV/A
T_{D_NAVDD}	NAVDD on delay time	5ms/step, 16 steps	0		75	ms
T_{SS_NAVDD}	NAVDD soft-start time	5ms/step, 8 steps	5		40	ms
	NAVDD delay/soft-satrt time tolerance		-15		+15	%
$NAVDD_{OFF}$	NAVDD power off delay time	2ms/step,7 steps	0		14	ms
D_{MAX_NAVDD}	NAVDD maximum duty		83	90	97	%
V_{OVP_NAVDD}	NAVDD OVP voltage percentage	NAVDD falling	110	120	130	%
R_{DSON_H}	NAVDD RDSON high-side			0.14	0.35	Ω
R_{DSON_L}	NAVDD RDSON low-side			0.2	0.45	Ω
$NAVDD_{RDIS}$	NAVDD power on/off discharge Res			10		Ω
I_{LIM_NAVDD}	NAVDD current limit		2.0	2.4	2.8	A
$NAVDD_{SCP}$	NAVDD SCP level		23	30	37	%
$NAVDD_{UVP}$	NAVDD UVP level		62	70	78	%
$NAVDD\_T_{UVP}$	NAVDD UVP Fault Delay Duration to IC shutdown		30	50	70	ms

Electrical Characteristics

(VIN = 2.5V to 5.5V, TA=-40℃ to 105℃，unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGL Charge-pump Regulator						
VGL	VGL output voltage range	0.25V/step	-6		-18	V
	VGL output voltage tolerance	TA=25℃,No load	-2		+2	%
	VGL Load Regulation	I_{VGL}=0mA to 60mA			0.6	%
T_{D_VGL}	VGL on delay time	5ms/step, 16 steps	0		75	ms
T_{SS_VGL}	VGL soft-start time	3ms/step, 8 steps	3		24	ms
	VGL delay/soft-start time tolerance		-15		+15	%
VGL_{OFF}	VGL power off delay time	2ms/step,7 steps	0		14	ms
VGL_{RDIS}	VGL power on/off discharge Res.			175		Ω
VGL_{RON_P}	VGL PMOS RON		0.15	0.5	1.5	Ω
VGL_{RON_N1}	VGL NMOS_1 RON		0.15	0.32	1.5	Ω
VGL_{RON_N2}	VGL NMOS_2 RON		0.15	0.9	1.5	Ω
VGL_{RON_N3}	VGL NMOS_3 RON		0.15	0.4	1.5	Ω
VGL_{SCP}	VGL SCP level		23	30	37	%
VGL_{UVP}	VGL UVP level		62	70	78	%
VGL_T_{UVP}	VGL UVP Fault Delay Duration to IC shutdown		30	50	70	ms

Electrical Characteristics

(VIN = 2.5V to 5.5V, TA=-40℃ to 105℃，unless otherwise specified.)

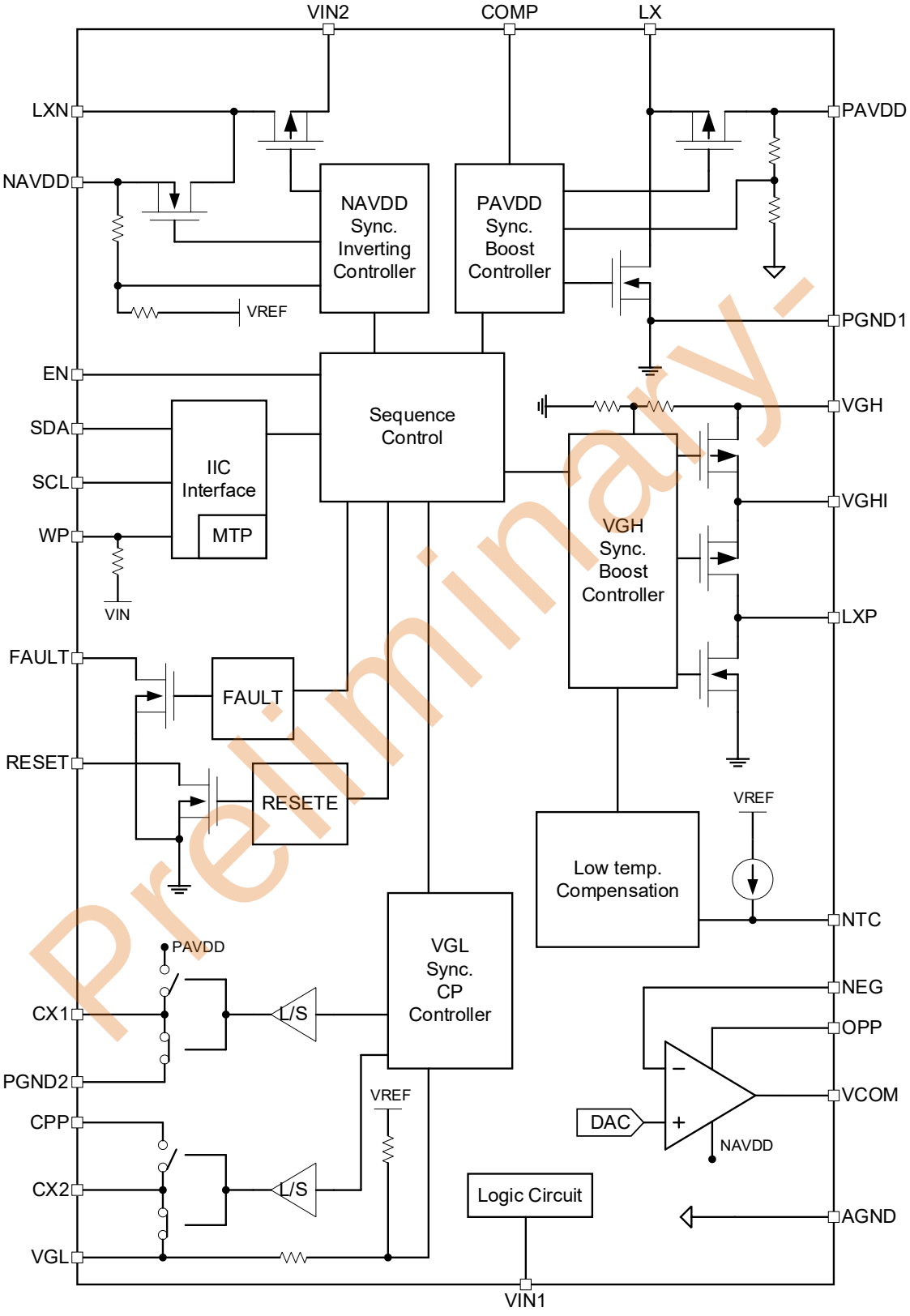
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VGH Sync. Boost Converter						
VGH_LT	VGH low temperature compensation Output Voltage range	1V/step, 8 steps VGH=VGH+VGH_LT >30V, Keep at 30V	2		9	V
VGH	VGH output voltage		7 or PAVDD+2		30	V
	VGH output voltage tolerance	TA=25℃, no load	-3		+3	%
	VGH output voltage tolerance	TA= -40℃ to 105℃ No load	-4.5		+4.5	%
	VGH Load Regulation	I_{VGL}=0mA to 60mA			0.6	%
T_{D_VGH}	VGH on delay time	5ms/step, 16 steps	0		75	ms
T_{SS_VGH}	VGH soft-start time	5ms/step, 4 steps	5		20	ms
	VGH delay/soft-start time tolerance		-15		+15	%
VGH_{OFF}	VGH power off delay time	2ms/step,7 steps	0		14	ms
D_{MAX_VGH}	VGH maximum duty		83	90	97	%
V_{OVP_VGH}	VGH OVP voltage percentage	(VGH+VGH_LT)*120%	110	120	130	%
V_{OVP_MAX}	VGHI max. OVP voltage threshold	(VGH+VGH_LT)>28.5	32	33	34	V
R_{DS_LS}	VGH RDSON low-side		0.2	0.36	0.6	Ω
R_{DS_HS}	VGH RDSON high-side		0.3	0.6	1	Ω
$R_{DS\_HS\_GD}$	VGH RDSON high-side GDMOS		0.3	0.65	1	Ω
VGH_{RDIS}	VGH power on/off discharge Res.			200		Ω
I_{LIM_VGH}	VGH Current Limit		0.56	0.7	0.88	A
I_NTC	VNTC source current		19.6	20	20.4	uA
VNTC1	VGH Terminal compensation voltage1		0.51	0.53	0.55	V
VNTC2	VGH Terminal compensation voltage2		0.57	0.59	0.61	V
VGH_{SCP}	VGH SCP level		23	30	37	%
VGH_{UVP}	VGH UVP level		62	70	78	%
VGH_T_{UVP}	VGH UVP Fault Delay Duration to IC shutdown		30	50	70	ms

Electrical Characteristics

(VIN = 2.5V to 5.5V, TA=-40℃ to 105℃，unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VLDO Linear Regurator						
VLDO	VLDO output voltage range	20mV/step	0.8		2	V
	VLDO output voltage tolerance	TA=25℃,No load	-2		+2	%
	VLDO output voltage tolerance	TA=-40℃ to 105℃ No load	-3		+3	%
	VLDO Load Regulation	I_{VGL}=0mA to 100mA			1	%
VCOM Operational Amplifier						
V_{VCOM_C}	VCOM_C output voltage range	20mV/step	-3		2	V
	VCOM_C Integral Non-Linearity			1		LSB
	VCOM_C Differential Non-Linearity			1		LSB
V_{VCOM_F}	VCOM_F output voltage range	10mV/step	VCOM_C -1.27		VCOM_C +1.28	V
	VCOM_F Integral Non-Linearity Error			1		LSB
	VCOM_F Differential Non-Linearity Error			1		LSB
T_{D_VCOM}	VCOM on delay time		0		75	ms
I_{VCOM_DC}	VCOM output current	Source	+150	+200	+250	mA
		Sink	-150	-200	-250	mA
I_{VCOM_SCP}	VCOM SCP current	Source	+50	+100		mA
		Sink	-50	-100		mA
$VCOM_{OFF}$	VCOM power off delay time	2ms/step, 7 steps	0		14	ms
$VCOM_{RDIS}$	VCOM power on/off discharge Res.			10		Ω
RESET Function						
T_{D_RESET}	RESET on delay time	5ms/step, 16 steps	0		75	ms
VIN_DET	RESET Detect VIN voltage	0x12h[6:5]=00 (UVLO_F)				V
VIN_DET	RESET Detect VIN voltage	0x12h[6:5]=01		2.1		V
VIN_DET	RESET Detect VIN voltage	0x12h[6:5]=10		2.4		V
VIN_DET	RESET Detect VIN voltage	0x12h[6:5]=11		2.7		V
	RESET Detect VIN voltage tolerance	TA=25℃, no load	-2		2	%
IIC Interface						
VIH	Logic input high	SDA,SCL	1.05			V
VIL	Logic input low	SDA,SCL			0.4	V
FSCL	SCL Clock frequency		15	400	1000	KHz

Functional Block Diagram



Typical Application Circuit_1

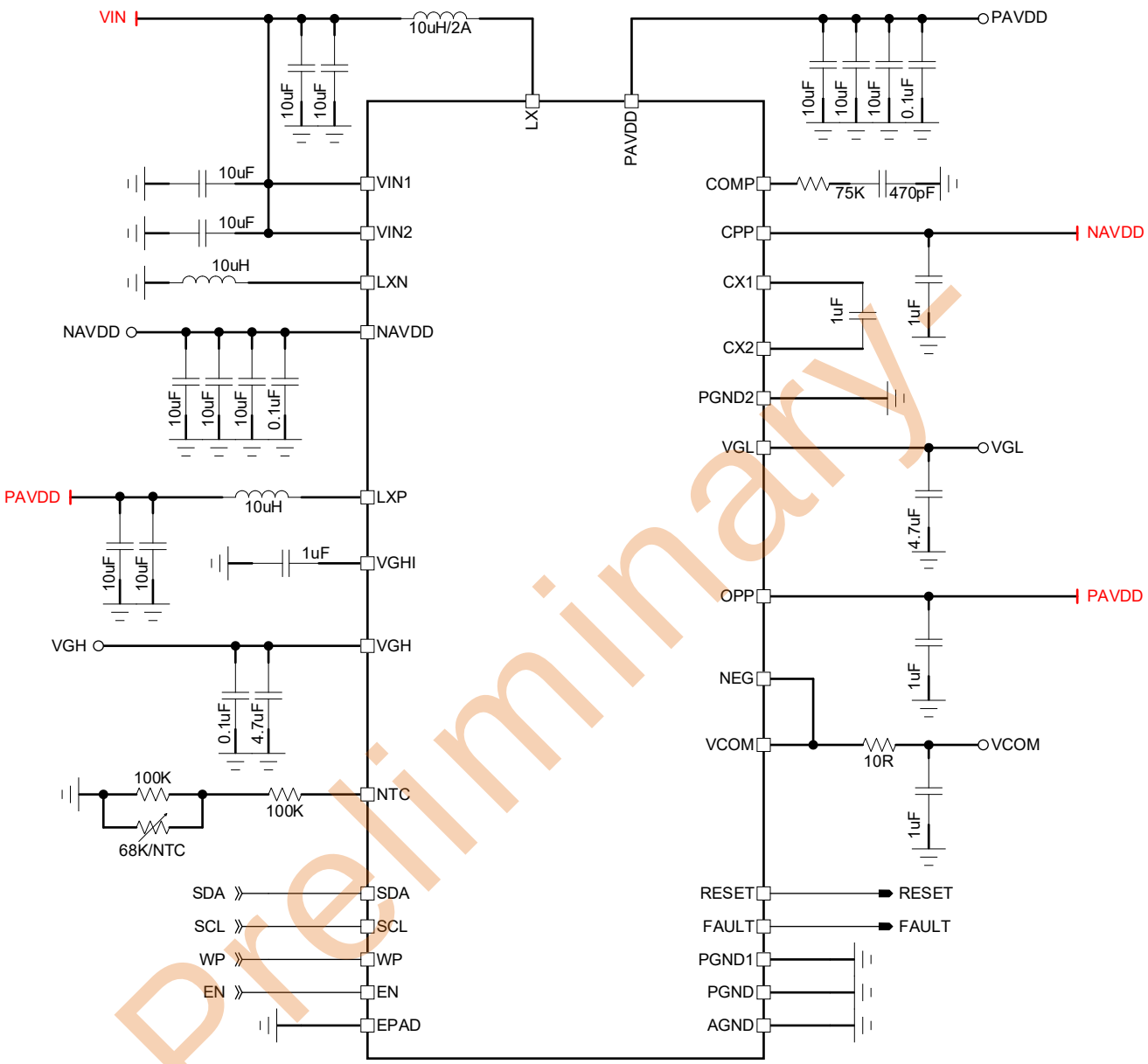


Figure 1. Typical Application Circuit with Internal Topology of VGL
PAVDD<|VGL|<(PAVDD+|NAVDD|)

Typical Application Circuit_2

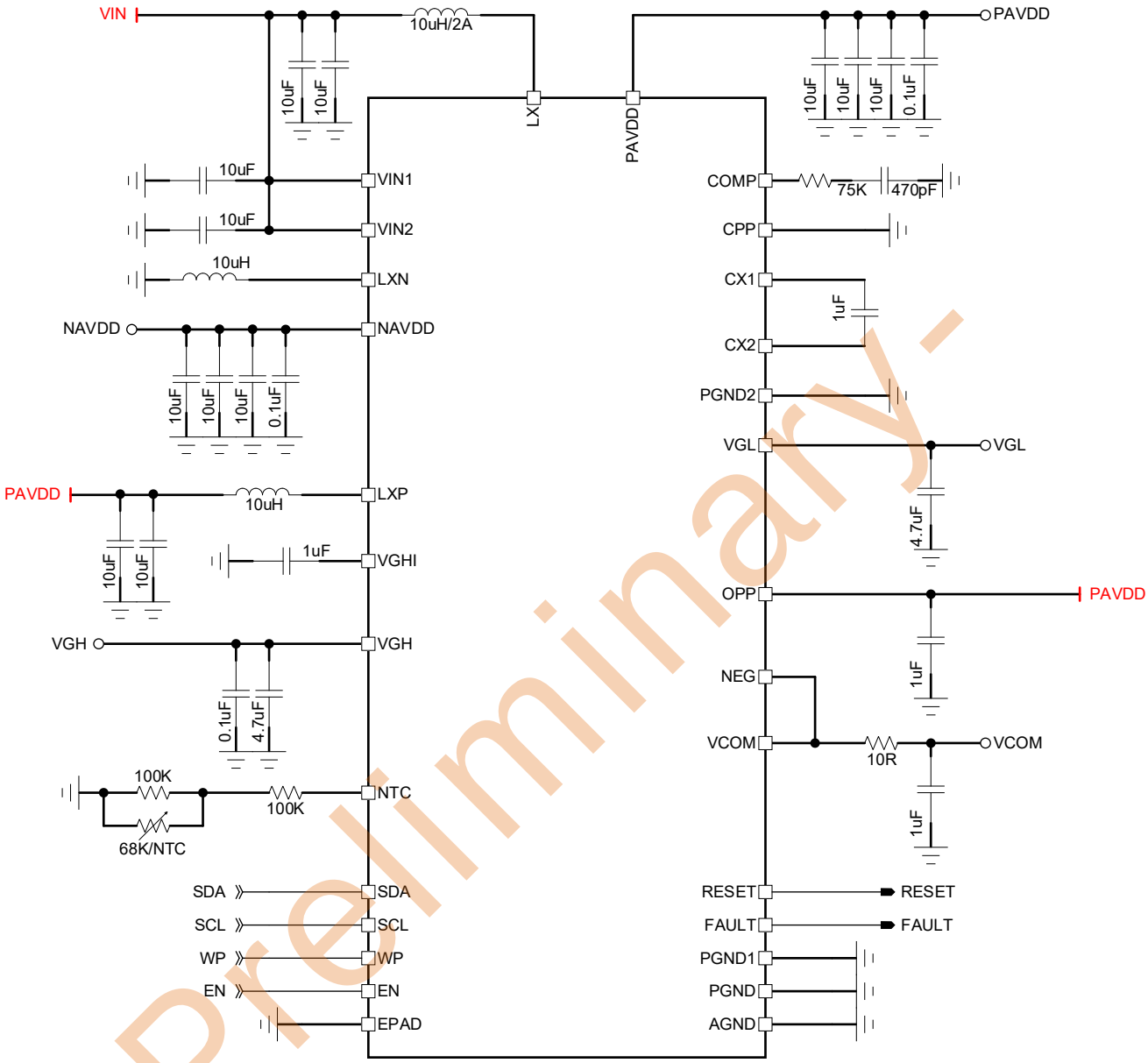


Figure 2. Typical Application Circuit with Internal Topology of VGL
|VGL|<PAVDD

Typical Application Circuit_3

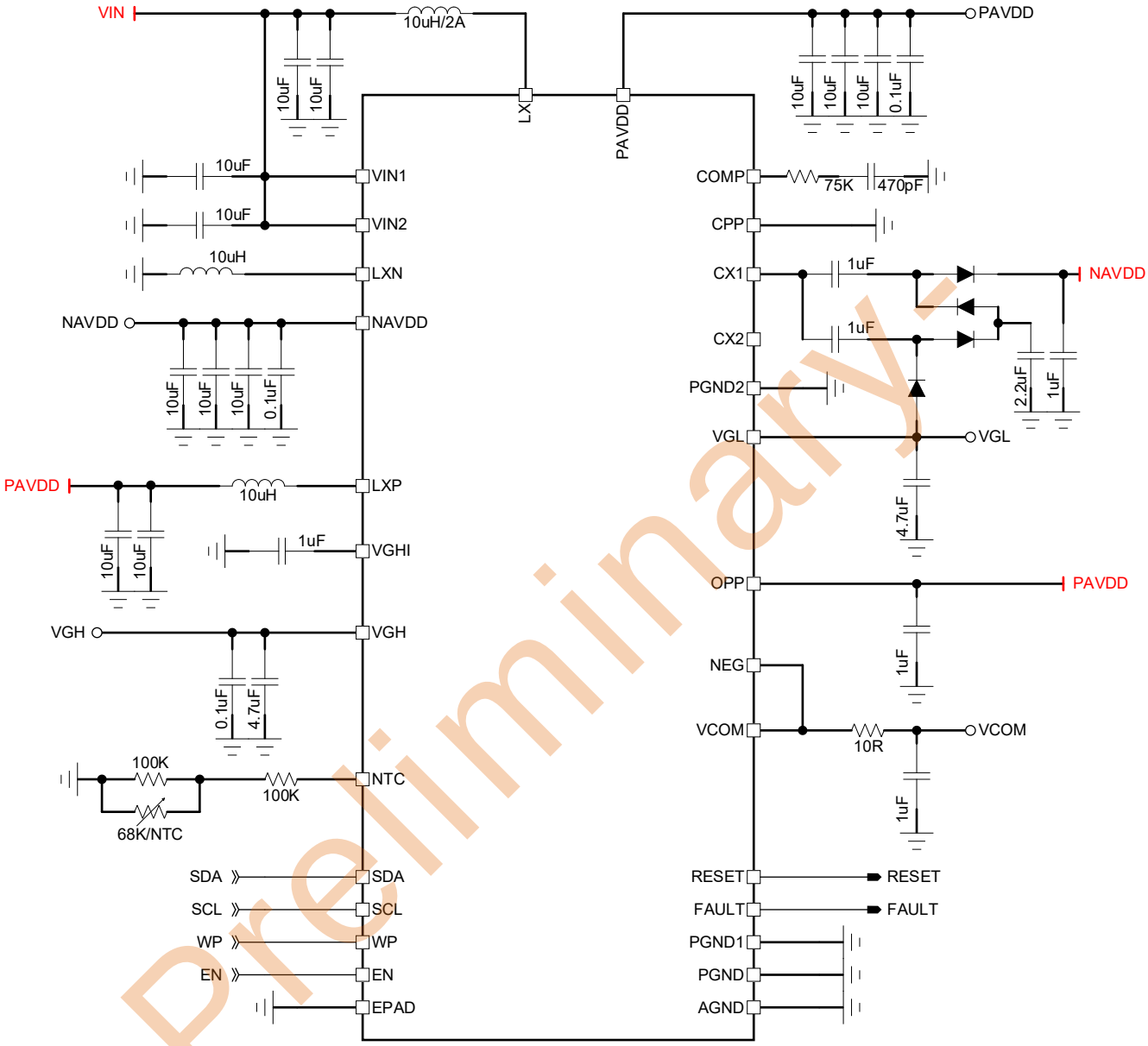


Figure 3. Typical Application Circuit with External Topology of VGL |VGL|>(PAVDD+|NAVDD|)

Typical Application Circuit_4

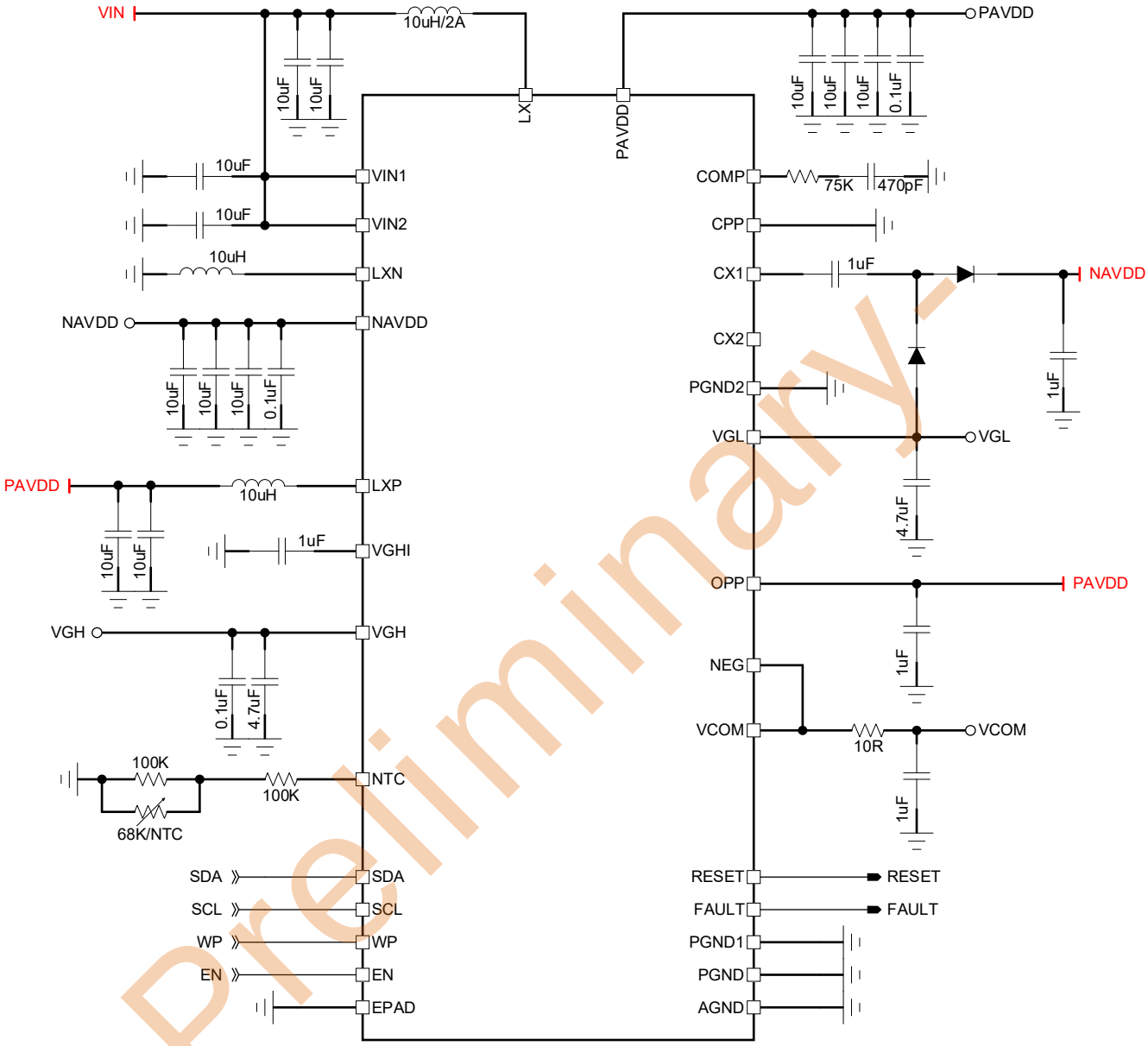


Figure 4. NAVDD Power Sequence Leading VGL Application Circuit with External Topology of VGL
PAVDD<|VGL|<(PAVDD+|NAVDD|)

Typical Application Circuit_5

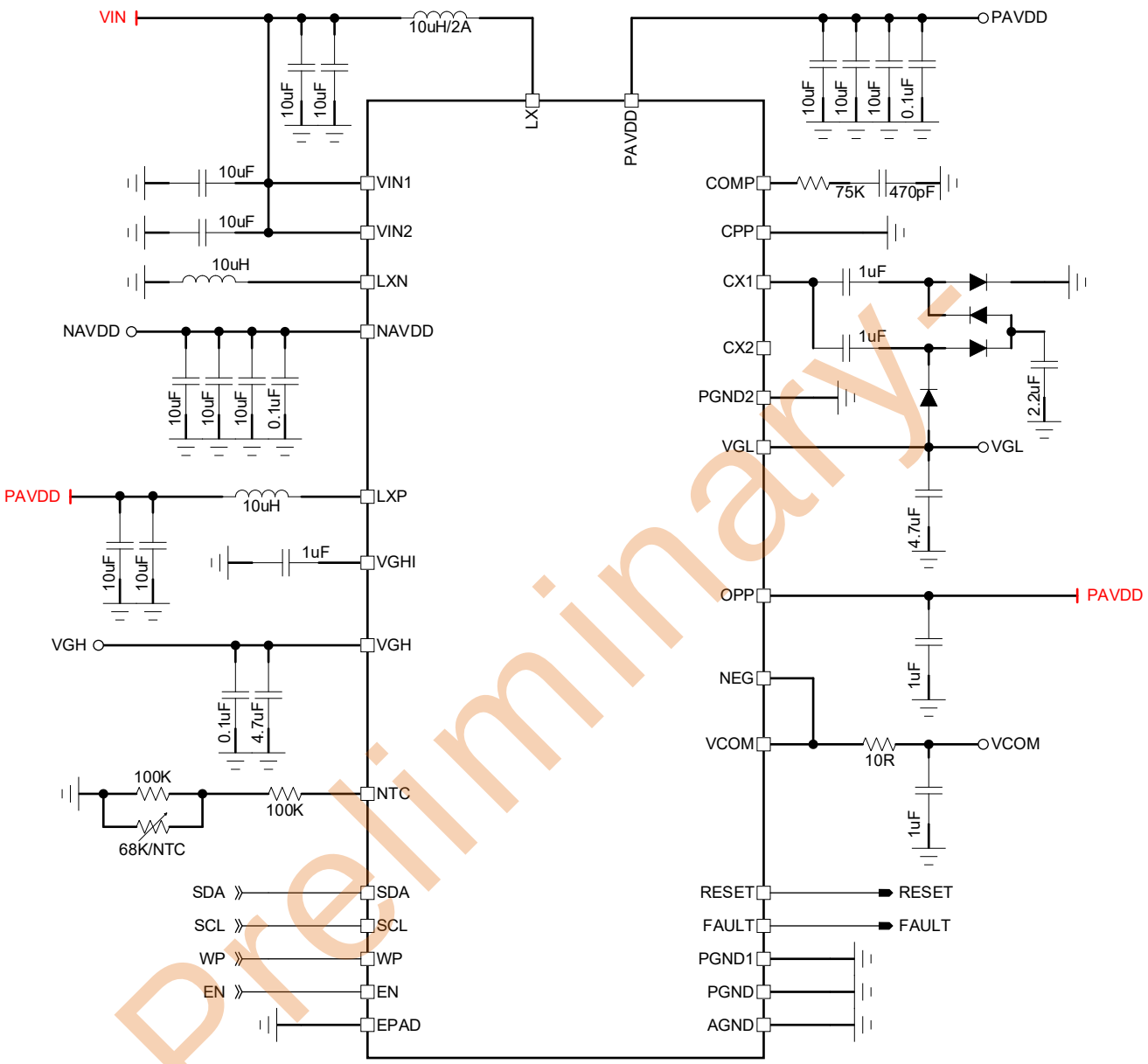


Figure 5. NAVDD Power Sequence Leading VGL and VGL Discharge Function Enabling Application Circuit with External Topology of VGL PAVDD<|VGL|<2 x PAVDD

Typical Application Circuit_6

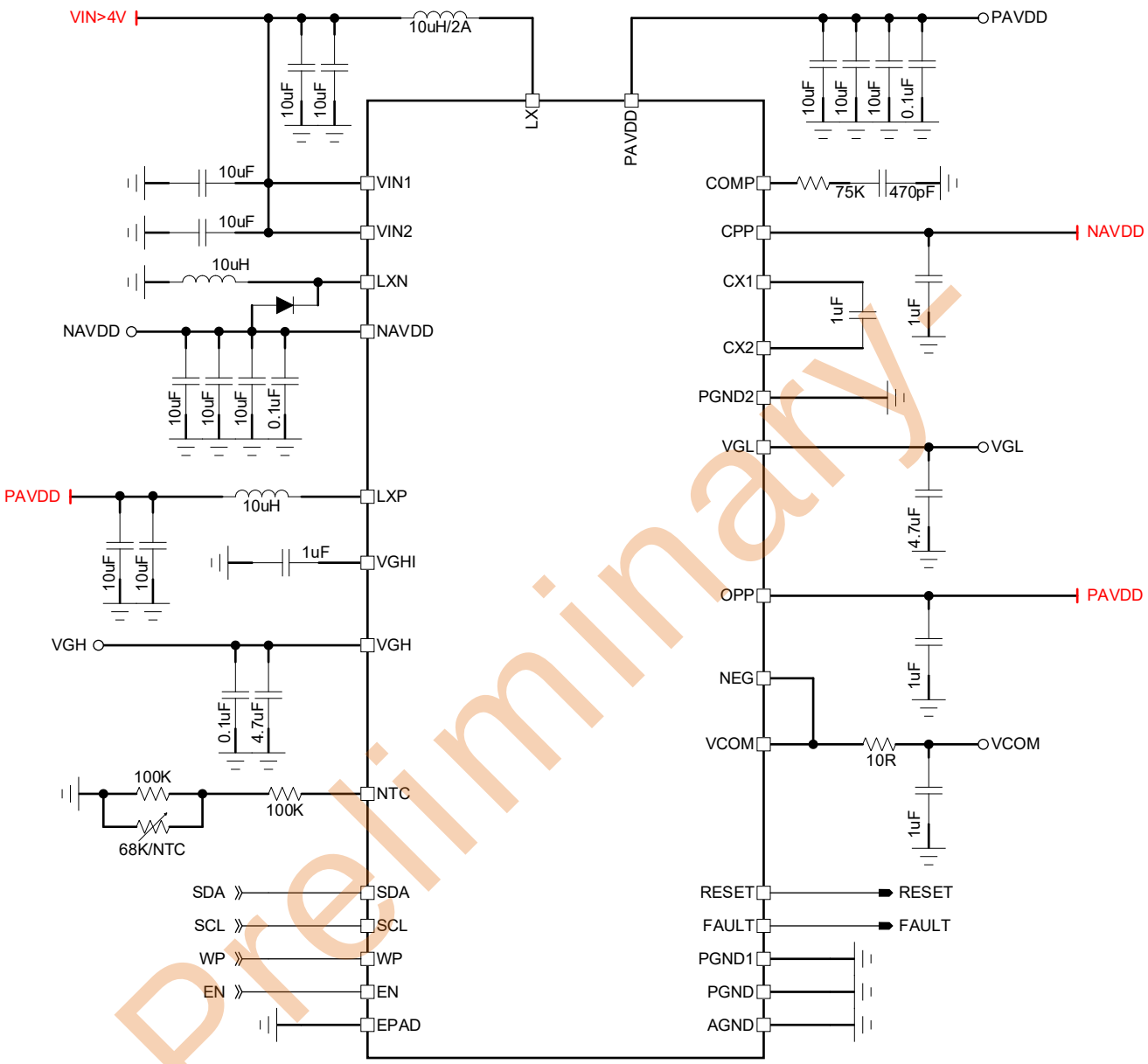


Figure 6. Typical Application Circuit with VIN>4V Application

VGL Application Condition with Circuit

VIN	VGL Conditions	Power Sequence	Circuit No.	LXN-NAVDD Schottky	0x14h[5]	VGL D/C	CPP Connection	VGL follow NAVDD at Power up
2.5V~4V (3.3V)	|VGL|<PAVDD	VGL→ NAVDD	Fig 2	X	0	V	GND	X
		NAVDD→ VGL			0	V	GND	X
	PAVDD<|VGL|<(PAVDD+|NAVDD|)	VGL→ NAVDD	Fig 1		0	V	NAVDD	X
			Fig 4		1	V	GND	X
		NAVDD→ VGL	Fig 4		1	X	GND	V
	PAVDD<|VGL|<2XPAVDD	VGL→ NAVDD	Fig 5		1	V	GND	X
		NAVDD→ VGL			1	V	GND	X
	|VGL|>(PAVDD+|NAVDD|)	VGL→ NAVDD	Fig 3		1	V	GND	X
		NAVDD→ VGL			1	X	GND	V
4V~5.5V (>4V)	|VGL|<PAVDD	VGL→ NAVDD	Fig 2 +Schotty	V	0	V	GND	X
		NAVDD→ VGL			0	V	GND	X
	PAVDD<|VGL|<(PAVDD+|NAVDD|)	VGL→ NAVDD	Fig 1 +Schotty		0	V	NAVDD	X
			Fig 4 +Schotty		1	V	GND	X
		NAVDD→ VGL	Fig 4 +Schotty		1	X	GND	V
	PAVDD<|VGL|<2XPAVDD	VGL→ NAVDD	Fig 5 +Schotty		1	V	GND	V
		NAVDD→ VGL			1	V	GND	V
	|VGL|>(PAVDD+|NAVDD|)	VGL→ NAVDD	Fig 6		1	V	GND	X
		NAVDD→ VGL			1	X	GND	V

Timing Diagram

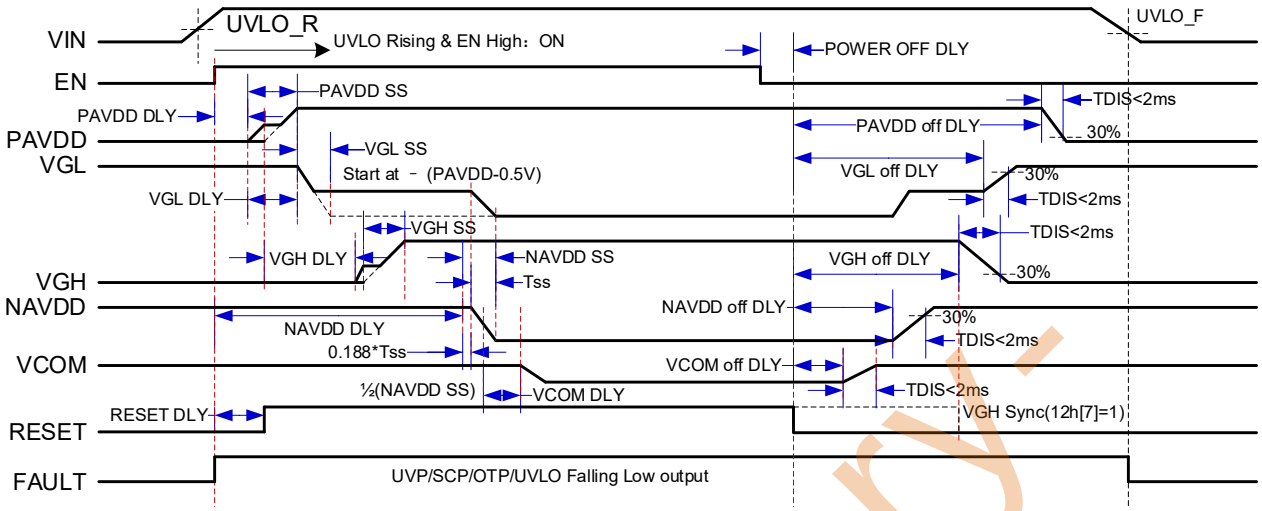


Figure 7. Power Sequence with Sequence Power-off

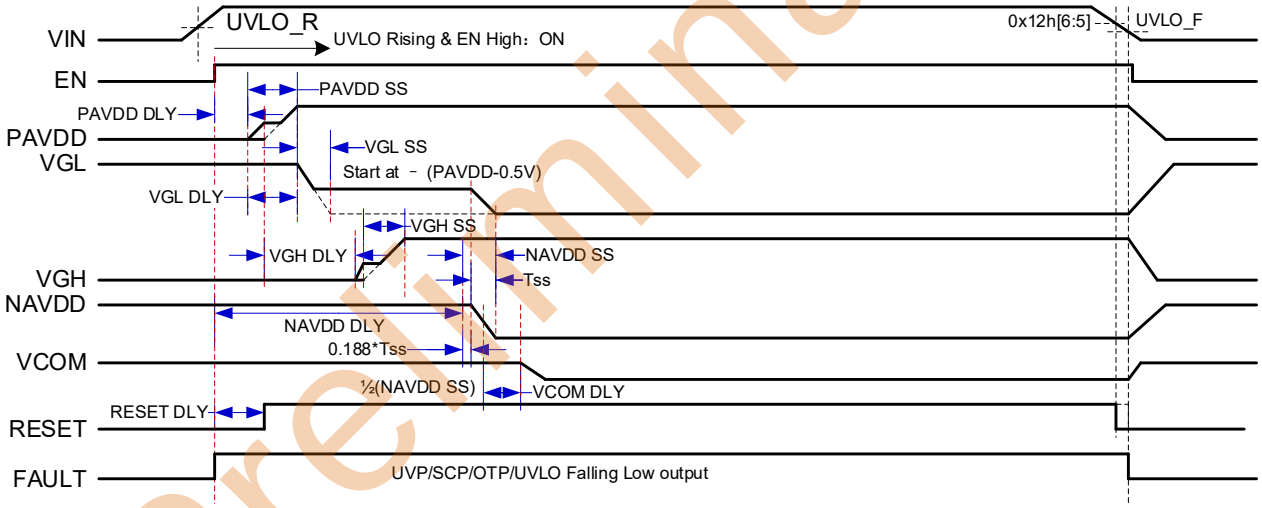


Figure 8. Power Sequence with Normal Power-off

Timing Diagram

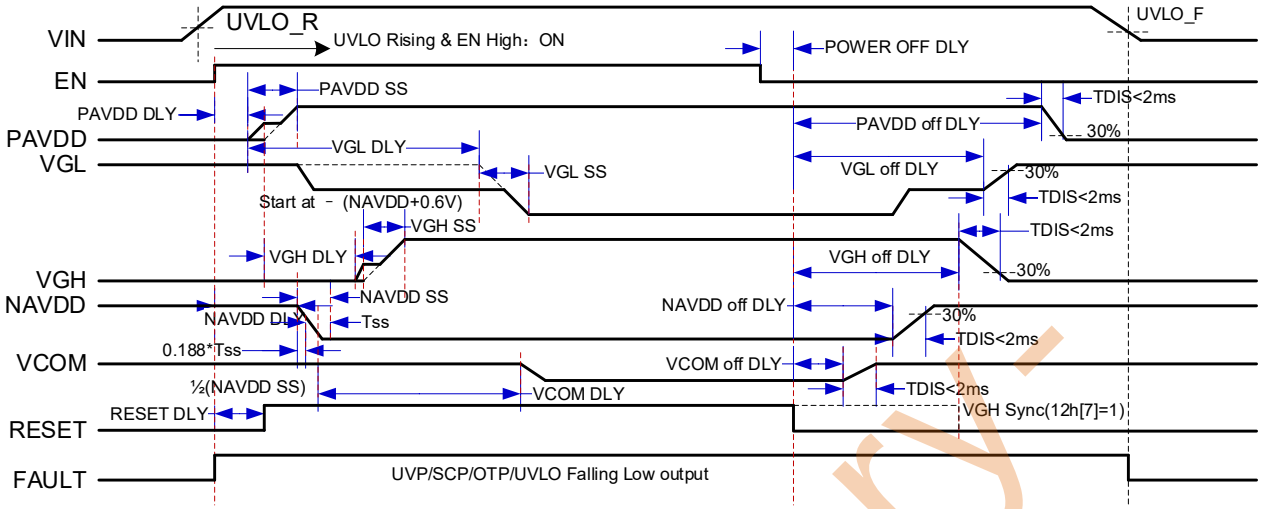


Figure 9. Power Sequence with NAVDD leading VGL (External Topology)

Note 1. Before IC power-up, the output voltage of each channel will be detected. If the one of outputs voltage is not below the SCP level, IC will wait the output voltage fall below the SCP level, then power up with sequence

APPLICATIONS INFORMATION

The LPQ6512 is an integrated solution for automotive TFT LCD panel, including PMIC and memory system. The LPQ6512 application mechanism is introduced in later sections. The LPQ6512's slave address is 1101110. PMIC – Power management system provides 2 sync. boost converters for PAVDD and VGH, one synchronous inverting converter for NAVDD, one negative charge-pump for VGL, and one operational amplifier for VCOM. Power-On and Power-Off sequences are control by EN input pin. Detail time sequence control is described in "Timing Diagram". The IIC interface can program each output channel as well as sequence control and voltage setting.

Swtiching Frequency Setting

The each channel switching frequency is set by the IIC interface. It has a 2-bit register as 4 steps, the setting options are 600kHz, 800kHz, 1MHz and 2.2MHz. The switching frequency default value is 600kHz (0x00). Please refer to the register map for details.

Under Voltage Protection(UVP)

The LPQ6512 equip a fault conditions to shut down IC. Once the output voltage is below the 70% output voltage, the internal timer starts counting and the fault condition continued about 50ms, the IC will shut down. After the UVLO or EN started again, the fault protection would be released. The protection start detecting at the soft-start finish of the outputs channel, the voltage of outputs has to large than the UVP level after soft-start finish and within 50ms. And an option is provided for user to enable or disable, the option can set by the register 14h[1].

Short Circuit Protection(SCP)

The LPQ6512 equip a fault conditions to shut down IC. In the power-on sequence, before the each channel power-up, the outputs voltage of each channel have to smaller than the SCP level of the channel. Or IC would wait the all of outputs voltage fall below the SCP level, then do the power-on sequence as the Figure 10 shown. The PAVDD_SCP_2 of PAVDD is 1.26V(typ) before PAVDD Soft-start, after soft-start finish the SCP will become 30% of voltage setting. the other channels are the 30% of voltage setting. The judgement point of the output voltage below SCP is from UVLO_R and plus 1ms.

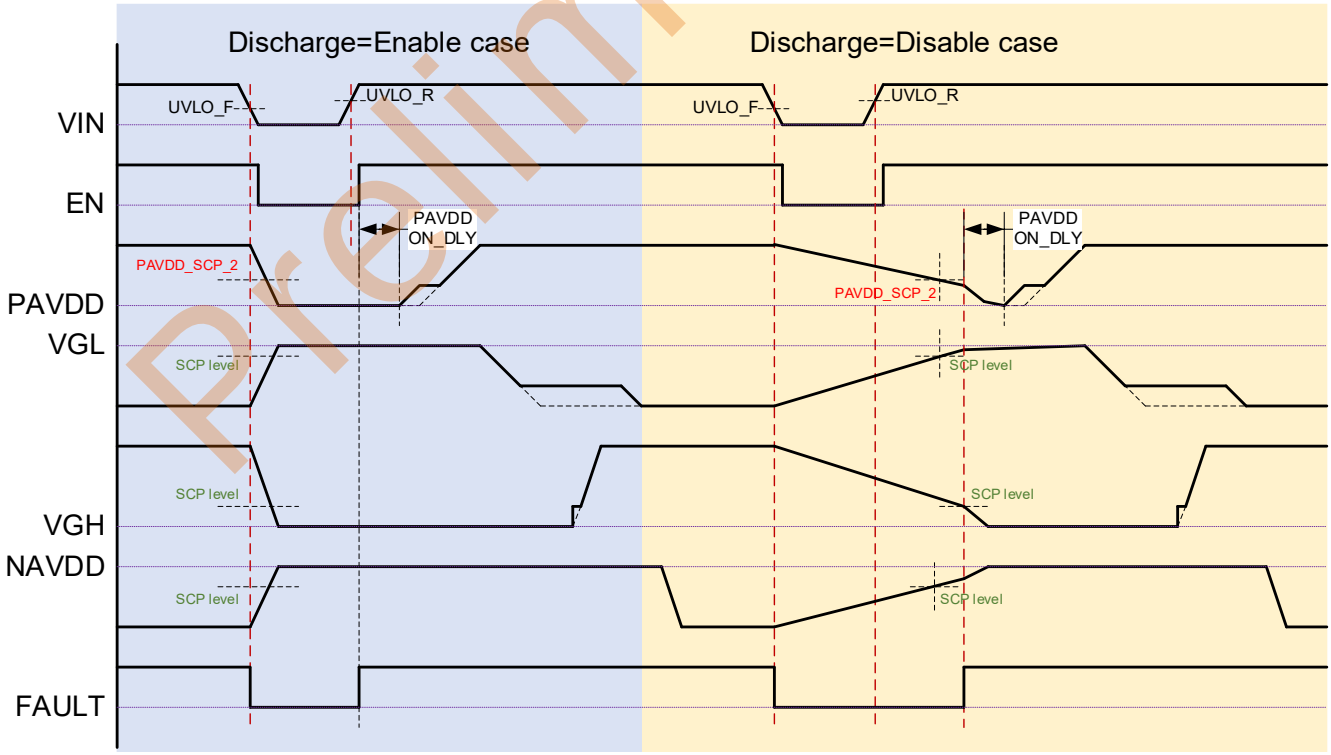


Figure 10 The Power-up Limitation of The Outputs Voltage must below the SCP level

In PAVDD pre-charge stage, the PAVDD SCP will be also checked after PAVDD power-on delay counting finish and plus 4ms. The SCP function also work during the soft-start period. If the PAVDD voltage is below the PAVDD_SCP_2 (1.26V_typ), IC will be protected at the delay counting finish and plus 4ms as the point “c” in the Figure 11 shown.
The pre-charging finish is going to judge the difference between PAVDD and VIN. When the difference is smaller than 0.2V(typ) that will be judged to pre-charge finished, and entry the soft-start stage. The SCP of the other channels is enabled after the soft-start of the channels is finished.

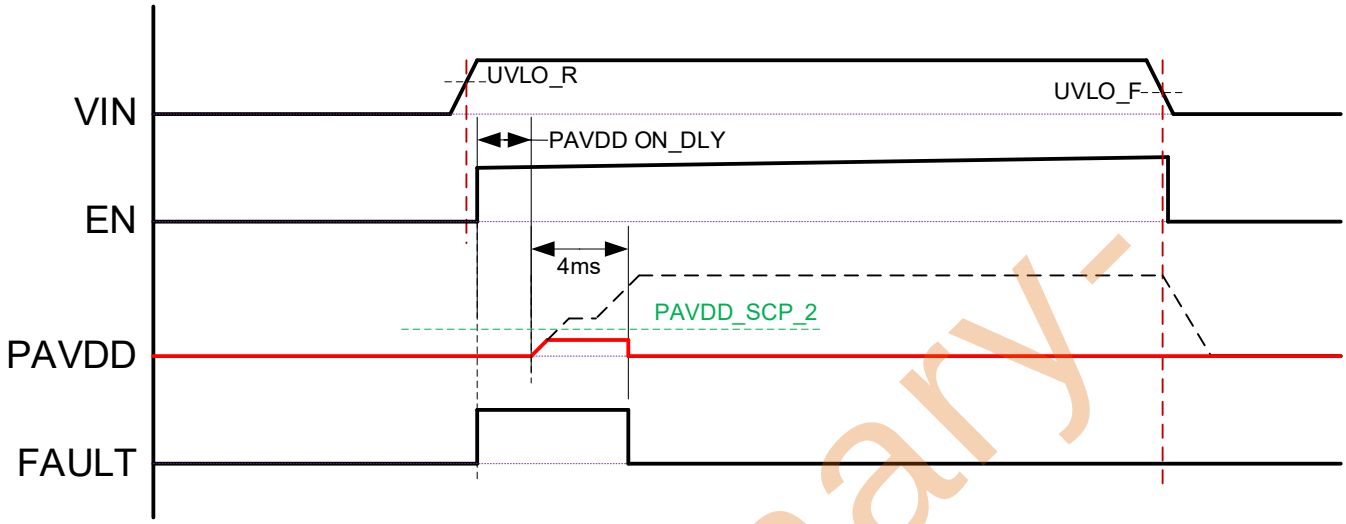


Figure 11 SCP Mechanism at PAVDD pre-charge when PAVDD with the Abnormal Heavy Load

In another one case, If the PAVDD voltage is above PAVDD_SCP_2, but not satisfy the condition of pre-charging finish. Then IC will keep in pre-charge stage, until the condition is satisfied and then to entry soft-start stage as the Figure 12 shown.

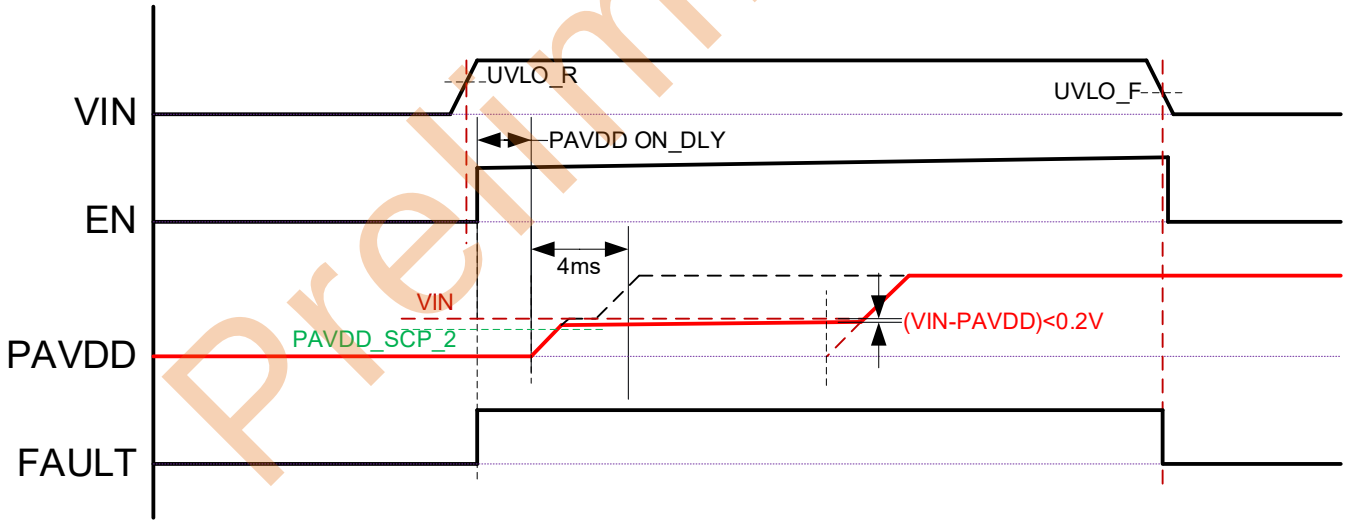


Figure 12 SCP Mechanism when PAVDD between SCP Level and Pre-charge Finish

Once the output voltage is below the 30% output voltage during operation stage, the high/low side MOSFET will stop switching immediately as the point “a” in the Figure 13 shown. The other channels will be stopped switching after 100us and the FAULT pin go low as the point “b”.

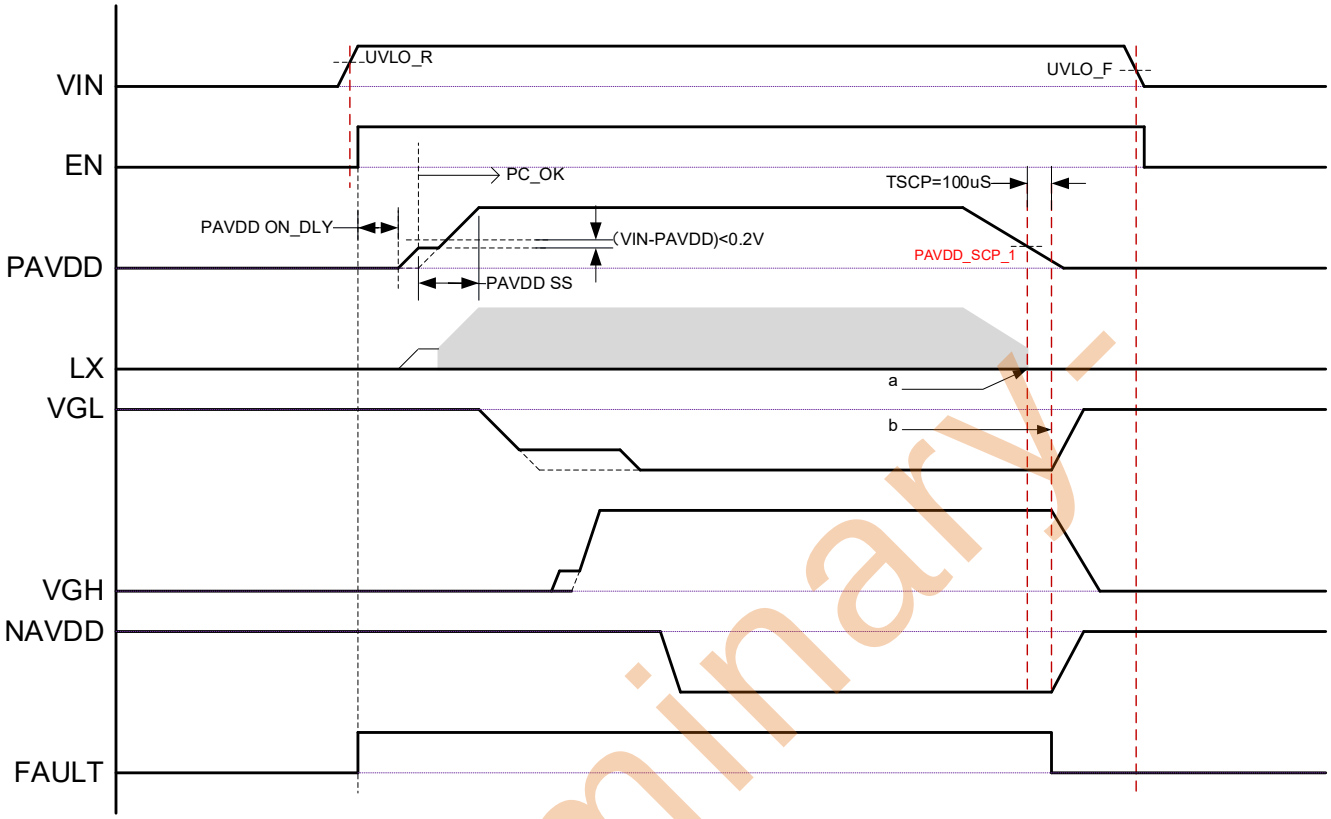


Figure 13 SCP Mechanism during Normal Operating

After the UVLO or EN started again, the protection would be released. There is an option as 14h[0] for user to disable or enable this function. the first PAVDD_SCP_2 detection during new power on in Figure 10 cannot be disable by 14h[0].

Over Temperature Protection(OTP)

The LPQ6512 equips an over temperature protection (OTP) to prevent the excessive power dissipation from overheating. The OTP will shut down switching operation while junction temperature exceeds approximately 150°C. All of output channel starting work while junction temperature is cooled by approximately 20°C. Prevent the maximum junction temperature over around 150°C and maintain continuous operation. The protection provided an option for user to enable or disable, the option can set by the register 14h[2].

PAVDD Syncchronous Boost Converter

The PAVDD synchronous Boost converter is high efficiency PWM architecture with programmable switching frequency. It performs fast transient responses to meet the requirement of source driver supplies for TFT-LCD display. The high operation frequency can prevent that switching frequency influence AM band range. The output voltage is controlled by a 6-bit register with 47 steps. The error amplifier varies the COMP voltage by sensing the PAVDD pin to regulate the output voltage.

PAVDD Slew Rate Setting

The PAVDD LX falling slew rate can be controlled by IIC interface, to optimize the efficiency and EMI performance. The adjustable options are slowest, slow, normal and fast. The default value is normal option. Please refer to the register map for details.

PAVDD Output Voltage Setting

The PAVDD output voltage is set by I2C interface. User can write the 00h[5:0] register to set PAVDD output voltage. It has 6 bits for output voltage adjustable, the setting range is from 5V to 7.3V, and each voltage step is about 50mV. The default voltage of PAVDD is 6.7V(0x22). Please refer the register map for detail on how to adjust the output voltage.

PAVDD Soft-start time Setting

The PAVDD soft-start time could be adjusted by the register 08h[2:0]. There are 3 bits and 8 steps. The soft-start time setting range is from 5ms to 40ms, and each step is about 5ms. The soft-start time default value is 10ms (0x01). The soft- start mechanism is following the reference voltage to soft-start, the soft-start starting point is from the slope of the soft-start down to the point of crosses 0V. The soft-start finish point is PAVDD output voltage ready. Please refer to Figure 7 and register map for details.

PAVDD Power-on Delay Time Setting

The PAVDD power-on delay time is adjustable by IIC interface. There are 16 steps within 3 bits register of 07h. The delay time setting range is from 0ms to 75ms, and each steps time is about 5ms. The delay time default value is 5ms (0x01). The delay time is from the MTP load data finish to PAVDD output voltage starting rising. Please refer the Figure 7, and register map for detail.

VGH Synchronous Boost Converter

The VGH synchronous boost converter is high efficiency PWM architecture with programmable switching frequency, output voltage, power-on delay time and soft-start time by IIC interface. The VGH integrate a GD MOSFET at output for sequence control.

VGH Soft-start Time Setting

The VGH sync-boost converter has an integrated soft-start function to reduce the input inrush current of power on. The soft-start time can be set through the 0Ch[1:0] register by the I2C interface. It has a 2-bit register with 4 steps. The soft-start time options as 5ms, 10ms, 15ms and 20ms, the each step is about 5ms. The soft- start mechanism is following the reference voltage to start up. The soft-start starting point is from the slope of the softstart down to the point of crosses 0V. The soft-start finish point is VGH output voltage ready. Please refer to Figure 7, and register map for details.

VGH Power-on Delay Time Setting

The VGH boost converter has integrated a power-on delay function. The delay time can be adjusted by I 2C interface, to write data into the 0Bh[3:0] register. There are 16 options within 3 bits. The delay time setting range is from 0ms to 75ms, and each step is about 5ms and the default value is 25ms (0x05). The delay time period is from the start point of PAVDD soft-start to VGH output voltage starts rising. If the VGH delay time set 0ms, the VGH need to wait PAVDD pre-charge finish, then go do pre-charge. Please refer the Figure 7 and register map for detail

VGH Voltage Setting

The VGH voltage is programmable by IIC interface. User can write data into 02h[5:0] register to set VGH voltage. The 02h register is for the VGH voltage of TH. The TH is the temperature point of started compensated temperature.Please refer the Figure 11 for clarity.

The voltage setting range is from 7V to 30V. The default value of VGH is 10V (0x06). The each voltage step is about 0.5V. It is integrated a protection when VGH too close PAVDD, VGH will automatically adjust the output voltage to keep the difference equal or large than 2V between PAVDD and VGH. Please refer the register map for detail.

VGH_LT Voltage Setting

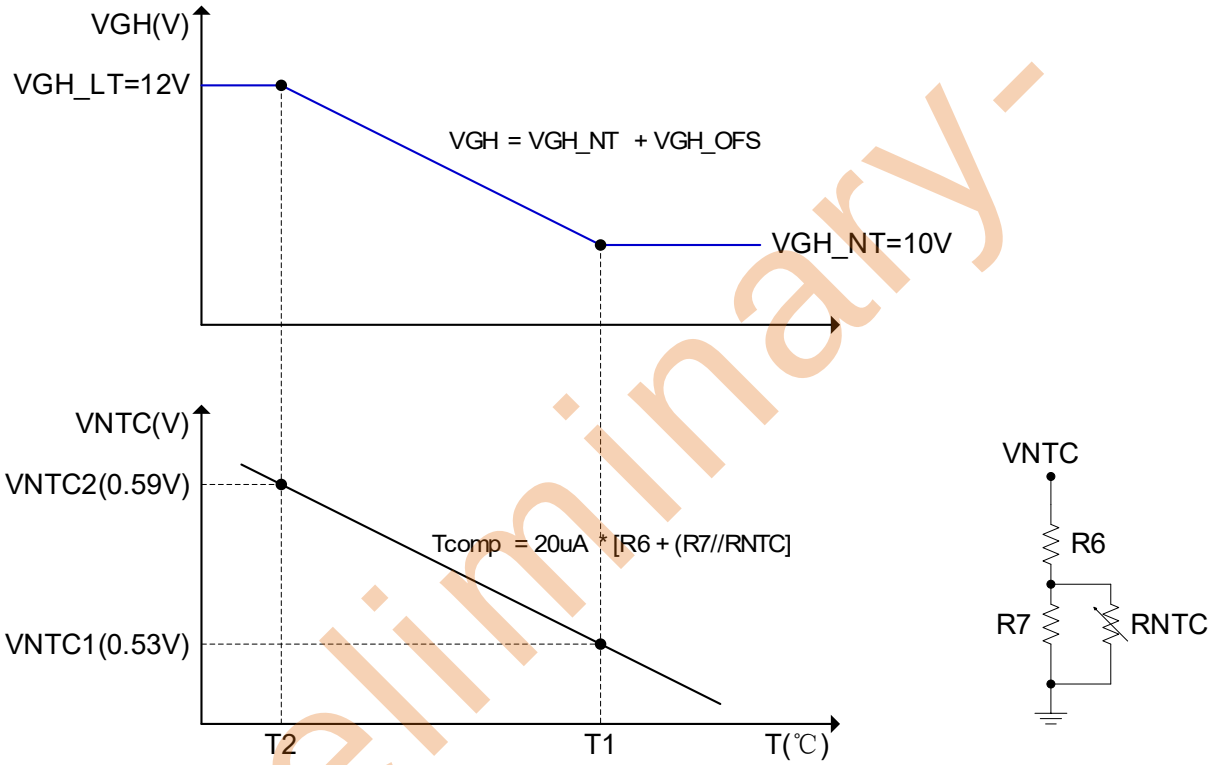
The VGH_LT voltage is programmable by IIC interface. User can write the 05h[2:0] register to set VGH_LT voltage. The 05h register is for VGH voltage of TL. TL is the temperature point of stopped compensated temperature. The VGH voltage of TL is equal to VGH+VGH_LT, the VGH_LT setting is only for difference. The setting range is from 2V to 9V. The default value of VGH_LT is 1V (0x00). The each voltage step is about 1V. Please refer register map for detail.

VGH Temperature Compensation

There is a temperature compensation feature in the LPQ6512. The VGH output voltage of TH will be change slowly from VGH of TH to VGH of TL if temperature is below TH, until the temperature is equal to TL, the VGH output voltage will be equal to VGH of TL.

The compensation is achieved by controlling the feedback voltage .The feedback voltage (VFBP) of VGH is sensed by VGH pin, from the VGH output voltage through the internal divider to get the feedback voltage. The VFBP can be compensated by external thermal sensing element (RNTC) and resistors (R6, R7), which set at what temperature the compensation starts and the slope of the compensation. The RNTC, R6 and R7 are shown in the "Typical Application Circuit", and temperature compensation curve is shown in Figure 16 :

Figure 16. VGH Temperature Compensation Curve



Where VFBPH is the feedback voltage at TL, the TH is the temperature point of started compensated temperature; TL is the temperature point of stopped compensated temperature.

The NTC pin will provide a current about 20uA(INTC), from IC internal constant current source. Then the RENTC can be calculated by the 20μA. The RENTC is equivalent resistance of RNTC, R6 and R7.

(1)$V_{NTC1} = I_{NTC} * R_{ENTC\_H}$ (1)

(2)$V_{NTC2} = I_{NTC} * R_{ENTC\_L}$ (2)

When the NTC function is not in use, the NTC PIN should be connected to GND.

VGL Negative Charge Pump Regulator

The negative charge pump regulator is programmable for soft-start time, the output voltage, switching frequency and power-on delay time by IIC interface. Moreover, it also equips a fault protection to prevent the output sudden overload.

VGL Output Voltage Setting

The VGL output voltage is adjusted by IIC interface. User can write a data into the 03h[5:0] register for setting VGL output voltage. There are 7 bits for output voltage adjustable, the setting range is from -6V to -18V, and each voltage step is about -250mV. The default output voltage is about -10V(0x10). Please refer the register map for detail.

Because the VGL voltage is supplied by PAVDD and NAVDD, the VGL maximum output voltage is limited by PAVDD + |NAVDD|, the VGL provides 3 options for user. If |VGL| < PAVDD, it is recommended that the CPP should be connected to GND as Figure 2 shown. But if the NAVDD power-on sequence lead VGL, the VGL topology should be used external mode (14h[5] = 1). The CPP should be connected to GND as the Figure 4. The definition of NAVDD leading VGL is (VGL – NAVDD) ≥ 0.3V during soft-start stage. If PAVDD < |VGL| < (PAVDD + |NAVDD|), the CPP should be connected to NAVDD as Figure 1 shown. If |VGL| > (PAVDD + |NAVDD|), changing internal mode to be external mode and using external diode structure as Figure 3 shown. In addition, if VGL uses internal mode, it needs enough headroom to regulate the output voltage. The headroom could be calculated by below equation :

Headroom ≥ I_{OUT_MAX}*12mV

$|V_{GL}|<V_{PAVDD}+|V_{NAVDD}|$-Headroom

Where the V_{PAVDD} is PAVDD output voltage, the V_{NAVDD} is NAVDD output voltage. If |VGL| voltage is higher than PAVDD + |NAVDD|, it is recommended to use external mode. The register 14h[5] should be changed from 0 to 1. The VGL output voltage is also limited by PAVDD, NAVDD and VF of external diode. The VF of external diode is not a constant, the forward current and ambient temperature will influence the VF, it is recommended to choose a maximum VF value to calculate. Therefore, the VGL voltage setting should be met the below equation :

Headroom ≥ I_{OUT_MAX} x 12mV

$|VGL|<2 \times V_{PAVDD}+|V_{NAVDD}|$-Headroom-($V_{FMAX}$ x 4) Where the VF_max is maximum forward voltage of diode.

VGL Soft-start Time Setting

The VGL negative charge pump regulator has integrated soft-start function to reduce the input inrush current at power on. The soft-start time cab be adjusted by register 0Ah[2:0]. There are 8 steps for setting. The soft-start time setting range is from 3ms to 24ms and each step is about 3ms. The soft-start time default value is 9ms (0x02). The soft-start time start from the VGL voltage starting falling to the slope of soft-start cross the setting level, the period is the VGL soft-start time. Please refer to Figure 7, and register map for details.

VGL Power-on Delay Time Setting

The negative charge pump regulator has integrated a power-on sequence control. The VGL power-on delay time is adjustable by IIC interface, there are 4 bits within register 0Ah[3:0] for setting. The setting range is from 0ms to 75ms and each step is about 5ms. The default setting is 25ms (0x05). The delay time start from the start point of PAVDD soft-start to VGL output voltage starting falling. If the VGL delay time set 0ms, the VGL soft-start need to wait PAVDD pre-charge finish, then go do soft-start. Please refer the Figure 7, and register map for detail.

VGL Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. One 4.7μF/X7R/1206 capacitors in parallel and the effective capacitance needs 4uF at least that are afford most applications. Additional capacitors can be added to improve output voltage ripple.

NAVDD Synchronous Buck-Boost Converter

The NAVDD synchronous Buck-Boost converter is high efficiency PWM architecture with programmable switching frequency. It performs fast transient responses to meet the requirement of source driver supplies for TFT-LCD display. The high operation frequency can prevent that switching frequency influence AM band range. The output voltage is controlled by a 6-bit register with 47 steps. For VIN > 4V application, the an-synchronous topology should be applied as the Figure 6 shown. To get a better performance.

NAVDD Powre on Delay Time Setting

The NAVDD power-on delay time is adjustable by IIC interface. There are 16 steps within 4 bits register of 0Dh. The power-on delay time setting range is from 0ms to 75ms, and each steps time is about 5ms. The delay time default value is 15ms (0x03). The delay time is from the MTP load data finish to NAVDD output voltage starting falling. Please refer the Figure 7, and register map for detail.

NAVDD Soft start Time Setting

The NAVDD has an internal soft-start mechanism to reduce the input inrush current. The NAVDD soft-start time can be adjusted by the register 0Eh[2:0]. There are 3 bits and 8 steps for setting. The soft-start time setting range is from 5ms to 40ms, and each step is about 5ms. The soft-start time default value is 10ms (0x01). The soft-start time starts from the NAVDD delay time counting finish. The stop point of soft-start time is NAVDD output voltage ready. Please refer to Figure 3 and register map for details.

NAVDD Output Voltage Setting

The NAVDD output voltage is adjusted by IIC interface. User can write data into the register 01h[5:0]. There are 6 bits for output voltage adjustable, the setting range is from -5V to -7.3V, and each voltage step is about -50mV. The default value is -6.7V(0x22). Please refer the register map for detail on how to adjust the output voltage.

NAVDD Output Capacitor Selection

For the best output voltage filtering, low ESR ceramic capacitors are recommended. Three 10uF/X7R/1206 capacitors in parallel and the effective capacitance needs 13uF at least that are afford most applications. Additional capacitors can be added to improve output voltage ripple.

NAVDD Current Limitation

The LPQ6512 can limit the peak current to achieve over current protection. The IC senses the inductor current during an on period. The internal P-MOSFET will be turned off if the peak inductor current reaches 2.0A (min.)

Programmable VCOM

The LPQ6512 provides the ability to reduce the flicker of an LCD Panel by adjusting the VCOM voltage during production test and alignment. The output voltage is adjusted by the I2C interface. There are two registers to adjust the VCOM voltage, one is VCOM_C for coarse tune, and another one is VCOM_F for fine tune. It is suggested to connect a resistor 10 ohm between output pin and output capacitor for better stability.
In general application, VCOM should not be set 0V. If user don't want to use this channel, please disable it.

VCOM Power on Delay Time Setting

The VCOM is integrated power-on sequence control. The delay time is adjustable by IIC interface, there are 4 bits within register 0Fh[3:0]. The delay time setting range is from 0ms to 75ms, and each step is about 5ms. The default value is 25ms (0x05). The delay time start from half of PAVDD and NAVDD soft-start to VCOM output voltage starting falling. Please refer the Figure 7, and register map for detail.

VCOM_C Voltage Setting

The VCOM_C voltage is adjusted by the register 04h[7:0], it is provided 8bits resolution and 256 steps for user setting. The setting range is from 2V to -3V, each step is about 20mV. The default value is -1V (0x64). Please refer the register map for detail.

VCOM_F Voltage Setting

The VCOM_F voltage is programmable by IIC interface, but the slave ID is different to VCOM_C, the slave ID is 0x60 and user can adjust it with “VCOM_F IIC Write Timing Sequence”. The VCOM_F is also provided 256 steps and 8 bits resolution. The default value is equal to VCOM_C setting (0x7F). From the 0x7F of VCOM_F to go up means VCOM_F voltage will be from VCOM_C voltage setting to increase with steps and each step is about 10mV. On the contrary, from the 0x7F to go down means VCOM_F voltage will be from VCOM_C voltage setting to decrease with steps. The setting range is from (VCOM_C + 1.28V) to (VCOM_C – 1.27V). Please refer the register map for detail.

RESET Voltage Detector

The voltage detector monitors the VIN voltage to generate a RESET signal from RESET pin while VIN is lower than the detecting level and not latched. Both detecting level and power-on delay time could be set by IIC interface. The detecting level could be adjusted by the register (0x12 [6:5]), it provided 4 options such as UVLO falling, 2.1V, 2.4V and 2.7V. The delay time could be set by register (0x10[3:0]), the setting range is from 0ms to 75ms, the each step is about 5ms. The delay time start from that the two conditions are achieved, one is VIN over UVLO threshold, and another one is the EN over VIH threshold, the stop point is that RESET signal goes to high.

In addition, the voltage detector also provided an option, user can chose which RESET goes low following power-off delay time or VGH channel turn off. The options can be set by the register 12h[7].

Discharge Function

The PAVDD, NAVDD, VGH, VGL and VCOM outputs voltage is integrated a discharge function. The each output voltage discharged from 100% to 30% rapidly within 2ms at power-off, preventing phenomena such as residual image on the display at power-off. If user want to make the outputs voltage were discharged to GND level, user should add discharging resistances on the outputs. The discharge function also provided an option for user to enable or disable, the option can set by the register 12h[4:0] individually for each channel.

If the discharge function is enabled, except discharge is worked at power-off, it also be discharge at power-on. The power-on discharge start to work from UVLO and plus 1ms, until the delay time of the channel be counting finish. If the discharge function is disabled, except the power-off without discharge function, the power-on also does not have. However, the period still has discharge function from UVLO_R to MTP_LOAD_OK. The mechanism is shown in Figure 18. Beside the discharging function should be turned off at same time if the channels are unused.

In addition, the VGL discharge function is related to the VGL topology and power-off sequence. Once VGL discharge enable, the VGL topology is recommended to use external mode as Figure 5, or the power sequence of VGL must be leading NAVDD.

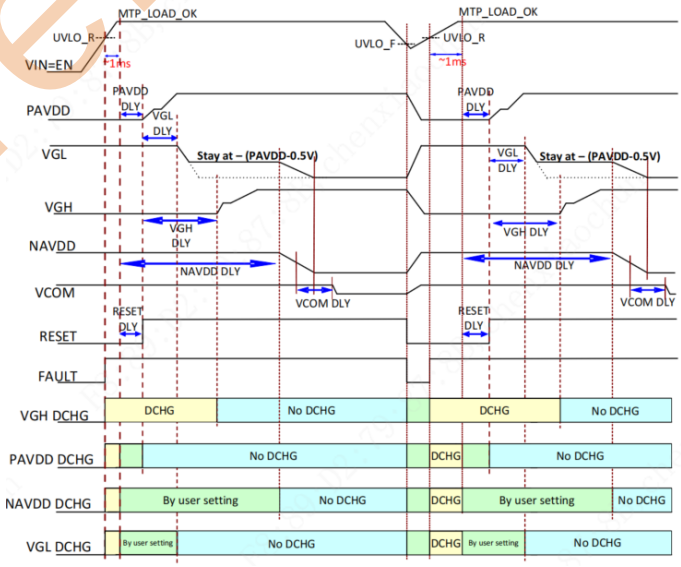


Figure 18. Discharge Function Enable Operation Mechanism

Slew Rate Control

The LPQ6512 provided options for switching node slew rate adjustment with IIC interface. The slew rate can be adjusted by the register 13h[7:0]. The register 13h[7:6] is for PAVDD LX falling slew rate control and there are 4 options for setting such as fast, normal, slow and slowest. The register 13h[5:4] is for NAVDD LXN rising slew rate control, the options are same as PAVDD. The register 13h[3:2] is for VGL CX1 slew rate control. The register 13h[1:0] is for VGH LXP falling slew rate control.

Power off Delay Time Setting

The PAVDD (18h[2:0]), NAVDD (19h[2:0]), VGH (1Ah[2:0]), VGL (1Bh[2:0]) and VCOM (1Ch[2:0]) power-off delay time are adjustable by I2C interface. The each output channels 8 steps within 3 bits register. The delay time setting range is from 0ms to 14ms, and each steps time is about 2ms. The each output power-off delay time default value is 0ms. The power-off delay time is from the RESET goes low to the delay counting finish. Please refer the Figure 7, and register map for detail.

Frequency Spread

The LPQ6512 is integrated a frequency spread of switching frequency function, it can reduce the noise level of the switching frequency point, it is good for EMI performance. There are 3 options for adjustment such as disabled, 3% and 6%. User can write data into the register 14h[4:3] to control the frequency spread.

FAULT Analysis Function

The LPQ6512 has provided a fault recording register that can help quickly user to know which output channel is UVP fault. If one of the output channels triggered UVP, the fault record will be saved into register 1Dh[3:0]. Then user can use IIC interface to read the data of 1Dh register during the UVP is triggered. The 1Dh register will show which channel is fault.

In addition, there is an option (1Ch[3]) for clearing the record of the fault register. Users can choice that the fault record be cleared by EN going low, or VIN fall below the VIN1 UVLO_F that also can be cleared fault record.

Control Register(FFh)

The LPQ6512 provides a register for user choosing that write/read data into MTP or register. User can set the MSB of the register FFH goes to high, it means the data is written into MTP. But writing data into register don't need to set the register FFH. In addition, reading data from MTP need to set the LSB of register FFH to high. On the contrary, reading data from register need to set LSB to low. Please refer the "IIC Write/Read Timing Sequence" for detail.

Device Address Setting

PMIC Device Slave Address (0XD6h)

MSB LSB

1	1	0	1	0	1	1	R/W

Read Address	Write Address
11010111(D7h)	11010110(D6h)

VCOM_F Device Slave Address (0x60h)

MSB LSB

0	1	1	0	0	0	0	R/W

Read Address	Write Address
01100001(61h)	01100000(60h)

PMIC IIC Write Timming Sequence(To DAC Register)

1. Write single Data(00h)

Start	11010110(Slave ID)	Slave ACK	00000000(Register)	Slave ACK	00101001(Data 29h)	Slave ACK	Stop

2. Write multiple Data(00h~1Ch)

Start	11010110(Slave ID)	Slave ACK	00000000(Register)	Slave ACK	LPQ6512 Data 00h	Slave ACK

LPQ6512 Data 01h	Slave ACK	……	Slave ACK	LPQ6512 Data 1Ch	Slave ACK	Stop

PMIC IIC Write Timming Sequence(To MTP)

3. Write Multiple Data (00h~1Ch)

Start	11010110(Slave ID)	Slave ACK	00000000(Register)	Slave ACK	LPQ6512 Data 00h	Slave ACK

LPQ6512 Data 01h	Slave ACK	……	Slave ACK	LPQ6512 Data 1Ch	Slave ACK	Stop

Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	10000000(Control Data)	Slave ACK	Stop

4. Write Single Data (00h)

Start	11010110(Slave ID)	Slave ACK	00000000(Register)	Slave ACK	00101001(Data 29h)	Slave ACK	Stop

Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	10000000(Control Data)	Slave ACK	Stop

PMIC IIC Read Timming Sequence(From DAC Register)

5. Read Mulitple Data (00h~1Ch)

Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000000(Control Data)	Slave ACK	Stop

Start	11010110(Slave ID)	Slave ACK	00000000(Data Address)	Slave ACK

Start	11010111(Slave ID)	Slave ACK	LPQ6512 Data 00h	Master ACK	LPQ6512 Data 01h	Master ACK

……	Master ACK	LPQ6512 Data 1Ch	Master N-ACK	Stop

6. Read Single Data (00h)

Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000000(Control Data)	Slave ACK	Stop

Start	11010110 (Slave ID)	Slave ACK	00000000 (Data Address)	Slave ACK	Start	11010111 (Slave ID)	Slave ACK	LPQ6512 Data	Master ACK	Stop

PMIC IIC Read Timming Sequence(From MTP)

7. Read Multiple Data (00h~1Ch)

Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000001(Control Data)	Slave ACK	Stop

Start	11010110(Slave ID)	Slave ACK	00000000(Data Address)	Slave ACK

Start	11010111(Slave ID)	Slave ACK	LPQ6512 Data 00h	Master ACK	LPQ6512 Data 01h	Master ACK

……	Master ACK	LPQ6512 Data 1Ch	Master NACK	Stop

8. Read Single Data (00h)

Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000001(Control Data)	Slave ACK	Stop

Start	11010110 (Slave ID)	Slave ACK	00000000 (Data Address)	Slave ACK	Start	11010111 (Slave ID)	Slave ACK	LPQ6512 Data	Master ACK	Stop

VCOM_F IIC Write Timing Sequence (To DAC Register)

Start	01100000(Slave ID)	Slave ACK	00000010(Control REG)	Slave ACK	10000000(Control Data)	Slave ACK	Stop

Start	01100000(Slave ID)	Slave ACK	00000000(Data Address)	Slave ACK	VCOM_F(Data)	Slave ACK	Stop

VCOM_F IIC Write Timing Sequence (To MTP&DAC Register)

Start	01100000(Slave ID)	Slave ACK	00000010(Control REG)	Slave ACK	00000000(Control Data)	Slave ACK	Stop

Start	01100000(Slave ID)	Slave ACK	00000000(Data Address)	Slave ACK	VCOM_F(Data)	Slave ACK	Stop

VCOM_F IIC Read Timing Sequence (From DAC Register)

Start	01100000(Slave ID)	Slave ACK	00000010(Control REG)	Slave ACK	10000000(Control Data)	Slave ACK	Stop

Start	01100000 (Slave ID)	Slave ACK	00000000 (Data Address)	Slave ACK	Start	01100001 (Slave ID)	Slave ACK	VCOM_F Data	Master NACK	Stop

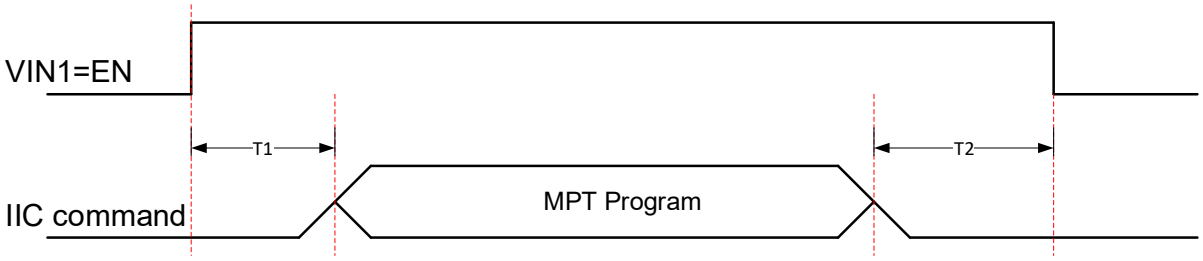
VCOM_F IIC Read Timing Sequence (From MTP)

Start	01100000(Slave ID)	Slave ACK	00000010(Control REG)	Slave ACK	00000000(Control Data)	Slave ACK	Stop

Start	01100000 (Slave ID)	Slave ACK	00000000 (Data Address)	Slave ACK	Start	01100001 (Slave ID)	Slave ACK	VCOM_F Data	Master NACK	Stop

MTP Program Sequence for Single Chip

MTP program timing sequence



Write Timing:
T1 = 50ms, T2 = 500ms
Read Timing:
T1 = 50ms, T2 = 10ms
F_{SCL} = 400KHz

IIC Protocol for MTP Program

IIC Write Timing Sequence

Start	11010110(Slave ID)	Slave ACK	00000000(Register)	Slave ACK	LPQ6512 Data 00h	Slave ACK

LPQ6512 Data 01h	Slave ACK	……	Slave ACK	LPQ6512 Data 1Ch	Slave ACK	Stop

Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	10000000(Control Data)	Slave ACK	Stop

IIC Read Timing Sequence

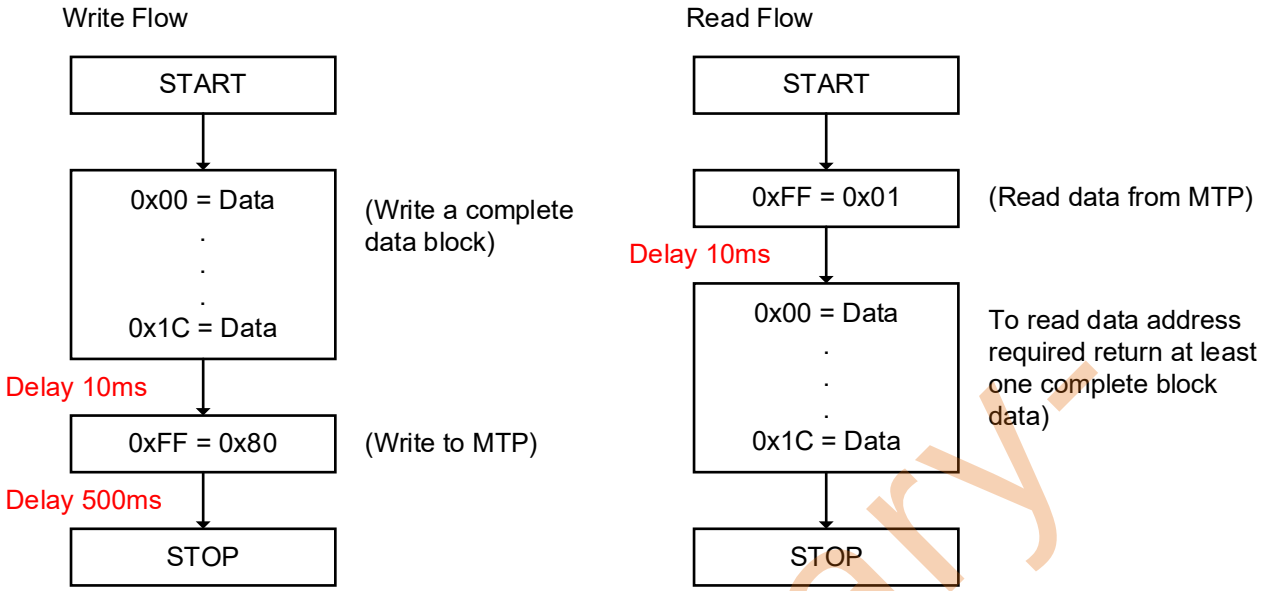
Start	11010110(Slave ID)	Slave ACK	11111111(Control REG)	Slave ACK	00000001(Control Data)	Slave ACK	Stop

Start	11010110(Slave ID)	Slave ACK	00000000(Data Address)	Slave ACK

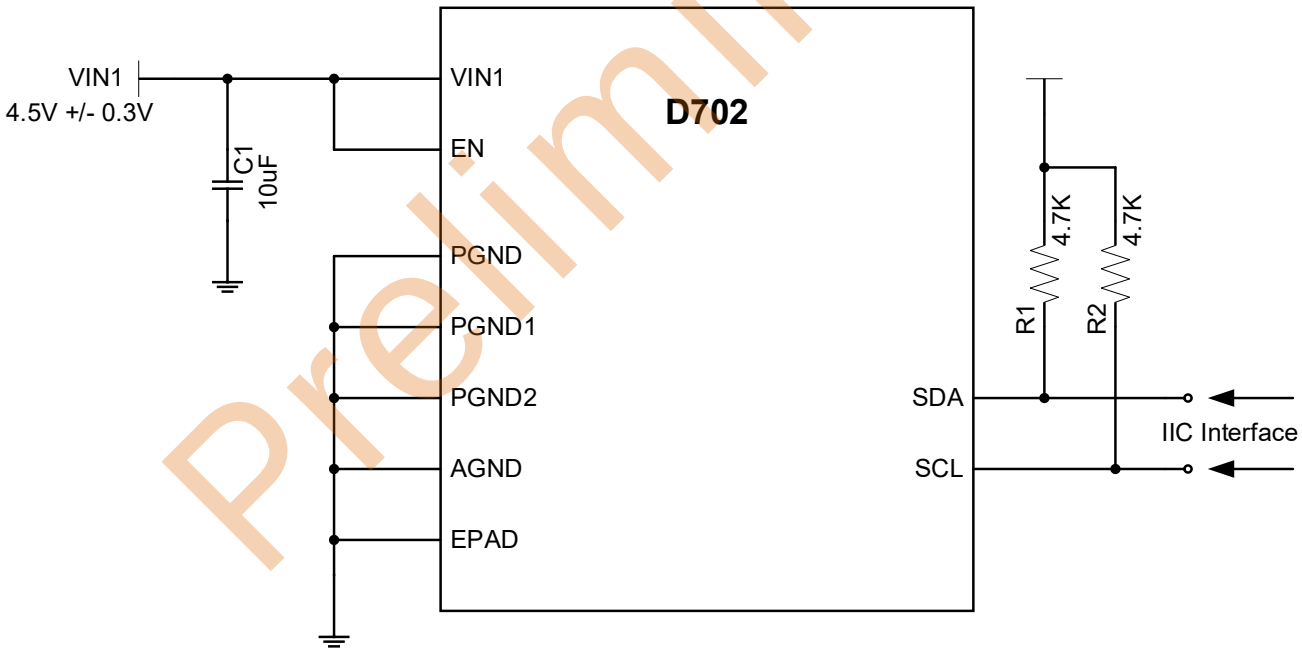
Start	11010111(Slave ID)	Slave ACK	LPQ6512 Data 00h	Master ACK	LPQ6512 Data 01h	Master ACK

……	Master ACK	LPQ6512 Data 1Ch	Master NACK	Stop

IIC Read / Write Flow Chat

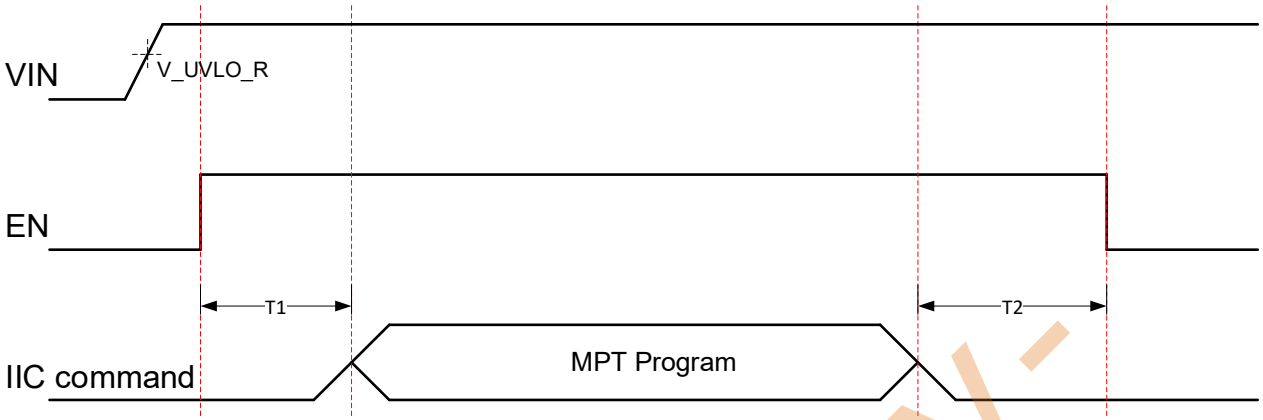


MTP Program Application Circuit for Single Chip



MTP Program Sequence on Board

MTP program timing sequence



IIC Write Conditions : (Note 2)

1. VIN = 3.3V ± 0.3V
2. EN = H
3. WP = L
4. All of output power ready (Note.6)

Write Timing:
VCOM_F : T1 = 60ms(Default code), T2 = 15ms (15ms wait time is required regardless of the munber of rewrite bits.) (Note. 1)
00h~1Ch : T1 = 60ms(Default code), T2 > 150ms(150ms wait time is required regardless of the munber of rewrite bits.) (Note. 1)
Read Timing:
T1 = 60ms, T2 = 10ms

MTP Program function (Note. 4)
Program time : 1 page = 4 bytes
MTP page program = 1*ERASE(4 bytes) + 2*PROGRAM(2 bytes) = 5ms +2*5ms = 15ms
VCOM_F = 1 page : 1*15ms = 15ms
0x00~0x1C = 10 pages : 10*15ms = 150ms

Note. 1 : T2:Add a margin according to the writing environment.
Note. 2 : LPQ6512 reads default data from internal memory(MTP) at startup, and run. The customer can change the data in the internal memory via external IIC communication, but IIC communication is not possible until VIN over UVLO_R and EN = H are satisfied.
When VIN over UVLO_R,EN = H ,All of output power ready, and T1 are satisfied, settings such as output voltage and delay time can be changed.
Note. 3 : All data in the DAC register (Existing data and rewritten data) is written to the MTP by the control register(FFh) Command, so a 150ms wait time is required.
Note. 4 : If the setting conditions are fixed, an IC with the setting conditions written to the MTP can be provided.
Note. 5 : UVLO_R = UVLO_F + UVLO_H
Note. 6 : Once the power on sequence is changed, the T1 waiting time should be changed to be PAVDD_DLY+PAVDD_SS+VGL_DLY+VGL_SS+VGH_DLY+VGH_SS+NAVDD_DLY+NAVDD_SS+VCOM_DLY+VCOM_SS(5ms)

PMIC Register Map:

PMIC Device Address: 0XD6h DVCOM Device Address: 0x60h

Register Address	Items	Resolution	Range	Default value	Step	Bit
0x00 (22h)	PAVDD[5:0]	0.05V	5.0V~8.15V	6.7V	64 step	6 bit
0x01 (22h)	NAVDD[5:0]	0.05V	-5.0V~-8.15V	-6.7V	64 step	6 bit
0x02 (06h)	VGH[5:0]	0.5V	7V~30V	10V	31 step	6 bit
0x03 (10h)	VGL[5:0]	0.25V	-6V~-18V	-10V	49 step	6 bit
0x04 (64h)	VCOM_C[7:0]	20mV	2V~-3V	-1V	251 step	8 bit
0x05 (00h)	VGH_LT_OFS[2]	+1V	0: Even 1: Odd	Even	2 step	1 bit
	VGH_LT[1:0]	2V	Even: 2V/4V/6V/8V Odd: 3V/5V/7V/9V	2V	4 step	2 bit
0x06 (00h)	SW Freq.[1:0]	--	600K/800K/1M/2.2M	600KHz	4 step	2 bit
0x07 (01h)	PAVDD ON DELAY[3:0]	5ms	0ms~75ms	5ms	16 step	4 bit
0x08 (01h)	PAVDD Soft-start[2:0]	5ms	5ms~40ms	10ms	8 step	3 bit
0x09 (05h)	VGL ON DELAY[3:0]	5ms	0ms~75ms	25ms	16 step	4 bit
0x0A (02h)	VGL Soft-start[2:0]	3ms	3ms~24ms	9ms	8 step	3 bit
0x0B (05h)	VGH ON DELAY[3:0]	5ms	0ms~75ms	25ms	16 step	4 bit
0x0C (01h)	VGH Soft-start[1:0]	5ms	5/10/15/20ms	10ms	4 step	2 bit
0x0D (03h)	NAVDD ON DELAY[3:0]	5ms	0ms~75ms	15ms	16 step	4 bit
0x0E (01h)	NAVDD Soft-start[2:0]	5ms	5ms~40ms	10ms	8 step	3 bit
0x0F (05h)	VCOM ON DELAY[3:0]	5ms	0ms~75ms	25ms	16 step	4 bit
0x10 (01h)	RESET ON DELAY[3:0]	5ms	0ms~75ms	5ms	16 step	4 bit
0x11 (06h)	POWER OFF DELAY[3:0]	3ms	0ms~45ms	18ms	16 step	4 bit

PMIC Register Map:

Register Address	Items	Resolution	Range	Default value	Step	Bit
0x12 (06h)	RESET Sync. Option[7]	--	Power off delay VGH sync.	Power off delay	2 step	1 bit
	VIN Detection[6:5]	--	UVLO_F/2.1V 2.4V/2.7V	UVLO falling	4 step	2 bit
	PAVDD D/C Function[4]	--	ON(0)/OFF(1)	ON	2 step	1 bit
	NAVDD D/C Function[3]	--	ON(0)/OFF(1)	ON	2 step	1 bit
	VGH D/C Function[2]	--	ON(0)/OFF(1)	OFF	2 step	1 bit
	VGL D/C Function[1]	--	ON(0)/OFF(1)	OFF	2 step	1 bit
	VCOM D/C Function[0]	--	ON(0)/OFF(1)	ON	2 step	1 bit
0x13 (55h)	PAVDD SR [7:6]	--	Fast/normal/Slow/Slowest	Normal	4 step	2 bit
	NAVDD SR [5:4]	--	Fast/normal/Slow/Slowest	Normal	4 step	2 bit
	VGL SR [3:2]	--	Fast/normal/Slow/Slowest	Normal	4 step	2 bit
	VGH SR [1:0]	--	Fast/normal/Slow/Slowest	Normal	4 step	2 bit
0x14 (00h)	VGL Internal/External[5]	--	Internal/External	Internal	2 step	1 bit
	Freq. Spread Option(EMI)[4:3]	--	OFF/+3%/+6%	OFF	3 step	2 bit
	OTP ON/OFF[2]	--	ON(0) / OFF(1)	ON	2 step	1 bit
	UVP ON/OFF[1]	--	ON(0) / OFF(1)	ON	2 step	1 bit
	SCP ON/OFF[0]	--	ON(0) / OFF(1)	ON	2 step	1 bit
X (7Fh)	VCOM_F[7:0]	10mV	VCOM_C-1.27V~ VCOM_C+1.28V	VCOM_C	256 step	8 bit
0x16 (3F)	VCOM/LDO_SEL[7]	---	VCOM(0)/LDO(1)	VCOM	2 step	1 bit
	VGH_IN_SEL[6]	---	PAVDD(0)/VIN(1)	PAVDD	2 step	1 bit
	RESET EN[5]	--	ON(1) / OFF(0)	ON	2 step	1 bit
	VCOM EN[4]	--	ON(1) / OFF(0)	ON	2 step	1 bit
	NAVDD EN[3]	--	ON(1) / OFF(0)	ON	2 step	1 bit
	VGH EN[2]	--	ON(1) / OFF(0)	ON	2 step	1 bit
	VGL EN[1]	--	ON(1) / OFF(0)	ON	2 step	1 bit
	PAVDD EN[0]	--	ON(1) / OFF(0)	ON	2 step	1 bit
0x17 (0Ah)	FAULT Behavior[3]		Not Pull Low(0) / Pull Low(1)	Pull Low	2 step	1 bit
	Refreshing Time[2:1]		0.25s/0.5s/1s/2s	0.5s	4 step	2 bit
	AR EN[0]	--	OFF(0) / ON(1)	OFF	2 step	1 bit
0x18 (00h)	PAVDD OFF DELAY[2:0]	2ms	0ms~14ms	0ms	7 step	3 bit
0x19 (00h)	NAVDD OFF DELAY[2:0]	2ms	0ms~14ms	0ms	7 step	3 bit
0x1A (00h)	VGH OFF DELAY[2:0]	2ms	0ms~14ms	0ms	7 step	3 bit
0x1B (00h)	VGL OFF DELAY[2:0]	2ms	0ms~14ms	0ms	7 step	3 bit

PMIC Register Map:

Register Address	Items	Resolution	Range	Default value	Step	Bit
0x1C (00h)	FAULT Analysis Clear Option[3]	--	Not clear by EN go low(0) /Clear by EN go low(1)	Not Clear	2 step	1 bit
	VCOM OFF DELAY[2:0]	2ms	0ms~14ms	0ms	7 step	3 bit
0x1D (00h)	PAVDD FAULT[3]	--	No fault(0) / Fault Happen(1)	No Fault	2 step	1 bit
	VGL FAULT[2]	--	No fault(0) / Fault Happen(1)	No Fault	2 step	1 bit
	VGH FAULT[1]	--	No fault(0) / Fault Happen(1)	No Fault	2 step	1 bit
	NAVDD FAULT[0]	--	No fault(0) / Fault Happen(1)	No Fault	2 step	1 bit
0xFF (00h)	Control Byte	00h: Read from DAC register 01h: Read from MTP 80h:Write to MTP				

Registers and DAC settings

PAVDD Voltage Set (0x00h) --- Default Code 22h

Name	# of Bits	Access	Default	Description
---	7-6	W/R	**00**	Reserved.
PAVDD	5	W/R	**1**	PAVDD voltage adjustment from 5.0V to 8.15V step=0.05V. Refer to table below for details.
	4	W/R	**0**	
	3	W/R	**0**	
	2	W/R	**0**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	PAVDD Voltage(V)	DAC Value	PAVDD Voltage(V)	DAC Value	PAVDD Voltage(V)	DAC Value	PAVDD Voltage(V)
00h	5.00	10h	5.80	20h	6.60	30h	7.40
01h	5.05	11h	5.85	21h	6.65	31h	7.45
02h	5.10	12h	5.90	22h	6.70	32h	7.50
03h	5.15	13h	5.95	23h	6.75	33h	7.55
04h	5.20	14h	6.00	24h	6.80	34h	7.60
05h	5.25	15h	6.05	25h	6.85	35h	7.65
06h	5.30	16h	6.10	26h	6.90	36h	7.70
07h	5.35	17h	6.15	27h	6.95	37h	7.75
08h	5.40	18h	6.20	28h	7.00	38h	7.80
09h	5.45	19h	6.25	29h	7.05	39h	7.85
0Ah	5.50	1Ah	6.30	2Ah	7.10	3Ah	7.90
0Bh	5.55	1Bh	6.35	2Bh	7.15	3Bh	7.95
0Ch	5.60	1Ch	6.40	2Ch	7.20	3Ch	8.00
0Dh	5.65	1Dh	6.45	2Dh	7.25	3Dh	8.05
0Eh	5.70	1Eh	6.50	2Eh	7.30	3Eh	8.10
0Fh	5.75	1Fh	6.55	2Fh	7.35	3Fh	8.15

NAVDD Voltage Set (0x01h) --- Default Code 22h

Name	# of Bits	Access	Default	Description
---	7-6	W/R	**00**	Reserved.
NAVDD	5	W/R	**1**	NAVDD voltage adjustment from -5.0V to -8.15V step=0.05V. Refer to table below for details.
	4	W/R	**0**	
	3	W/R	**0**	
	2	W/R	**0**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	NAVDD Voltage(V)	DAC Value	NAVDD Voltage(V)	DAC Value	NAVDD Voltage(V)	DAC Value	NAVDD Voltage(V)
00h	-5.00	10h	-5.80	20h	-6.60	30h	-7.40
01h	-5.05	11h	-5.85	21h	-6.65	31h	-7.45
02h	-5.10	12h	-5.90	22h	-6.70	32h	-7.50
03h	-5.15	13h	-5.95	23h	-6.75	33h	-7.55
04h	-5.20	14h	-6.00	24h	-6.80	34h	-7.60
05h	-5.25	15h	-6.05	25h	-6.85	35h	-7.65
06h	-5.30	16h	-6.10	26h	-6.90	36h	-7.70
07h	-5.35	17h	-6.15	27h	-6.95	37h	-7.75
08h	-5.40	18h	-6.20	28h	-7.00	38h	-7.80
09h	-5.45	19h	-6.25	29h	-7.05	39h	-7.85
0Ah	-5.50	1Ah	-6.30	2Ah	-7.10	3Ah	-7.90
0Bh	-5.55	1Bh	-6.35	2Bh	-7.15	3Bh	-7.95
0Ch	-5.60	1Ch	-6.40	2Ch	-7.20	3Ch	-8.00
0Dh	-5.65	1Dh	-6.45	2Dh	-7.25	3Dh	-8.05
0Eh	-5.70	1Eh	-6.50	2Eh	-7.30	3Eh	-8.10
0Fh	-5.75	1Fh	-6.55	2Fh	-7.35	3Fh	-8.15

VGH Voltage Set (0x02h) --- Default Code 06h

Name	# of Bits	Access	Default	Description
---	7-6	W/R	**00**	Reserved.
VGH	5	W/R	**0**	VGH voltage adjustment from 7.0V to 30V step=0.5V. Refer to table below for details.
	4	W/R	**0**	
	3	W/R	**0**	
	2	W/R	**1**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	VGH Voltage(V)	DAC Value	VGH Voltage(V)	DAC Value	VGH Voltage(V)	DAC Value	VGH Voltage(V)
00h	7.0	10h	15.0	20h	23.0	30h	30.0
01h	7.5	11h	15.5	21h	23.5	31h	30.0
02h	8.0	12h	16.0	22h	24.0	32h	30.0
03h	8.5	13h	16.5	23h	24.5	33h	30.0
04h	9.0	14h	17.0	24h	25.0	34h	30.0
05h	9.5	15h	17.5	25h	25.5	35h	30.0
06h	10.0	16h	18.0	26h	26.0	36h	30.0
07h	10.5	17h	18.5	27h	26.5	37h	30.0
08h	11.0	18h	19.0	28h	27.0	38h	30.0
09h	11.5	19h	19.5	29h	27.5	39h	30.0
0Ah	12.0	1Ah	20.0	2Ah	28.0	3Ah	30.0
0Bh	12.5	1Bh	20.5	2Bh	28.5	3Bh	30.0
0Ch	13.0	1Ch	21.0	2Ch	29.0	3Ch	30.0
0Dh	13.5	1Dh	21.5	2Dh	29.5	3Dh	30.0
0Eh	14.0	1Eh	22.0	2Eh	30.0	3Eh	30.0
0Fh	14.5	1Fh	22.5	2Fh	30.0	3Fh	30.0

VGL Voltage Set (0x03h) --- Default Code 10h

Name	# of Bits	Access	Default	Description
---	7-6	W/R	**00**	Reserved.
VGL	5	W/R	**0**	VGL voltage adjustment from -6.0V to -18V step=0.25V. Refer to table below for details.
	4	W/R	**1**	
	3	W/R	**0**	
	2	W/R	**0**	
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VGL Voltage(V)	DAC Value	VGL Voltage(V)	DAC Value	VGL Voltage(V)	DAC Value	VGL Voltage(V)
00h	-6.00	10h	-10.00	20h	-14.00	30h	-18.00
01h	-6.25	11h	-10.25	21h	-14.25	31h	-18.00
02h	-6.50	12h	-10.50	22h	-14.50	32h	-18.00
03h	-6.75	13h	-10.75	23h	-14.75	33h	-18.00
04h	-7.00	14h	-11.00	24h	-15.00	34h	-18.00
05h	-7.25	15h	-11.25	25h	-15.25	35h	-18.00
06h	-7.50	16h	-11.50	26h	-15.50	36h	-18.00
07h	-7.75	17h	-11.75	27h	-15.75	37h	-18.00
08h	-8.00	18h	-12.00	28h	-16.00	38h	-18.00
09h	-8.25	19h	-12.25	29h	-16.25	39h	-18.00
0Ah	-8.50	1Ah	-12.50	2Ah	-16.50	3Ah	-18.00
0Bh	-8.75	1Bh	-12.75	2Bh	-16.75	3Bh	-18.00
0Ch	-9.00	1Ch	-13.00	2Ch	-17.00	3Ch	-18.00
0Dh	-9.25	1Dh	-13.25	2Dh	-17.25	3Dh	-18.00
0Eh	-9.50	1Eh	-13.50	2Eh	-17.50	3Eh	-18.00
0Fh	-9.75	1Fh	-13.75	2Fh	-17.75	3Fh	-18.00

VCOM_C Voltage Set (0x04h) --- Default Code 64h

Name	# of Bits	Access	Default	Description
VCOM_C	7	W/R	**0**	VCOM_C voltage adjustment from -3V to 2V step=0.02V. Refer to table below for details.
	6	W/R	**1**	
	5	W/R	**1**	
	4	W/R	**0**	
	3	W/R	**0**	
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VCOM_C Voltage(V)	DAC Value	VCOM_C Voltage(V)	DAC Value	VCOM_C Voltage(V)	DAC Value	VCOM_C Voltage(V)
00h	-3.00	1Ch	-2.44	38h	-1.88	54h	-1.32
01h	-2.98	1Dh	-2.42	39h	-1.86	55h	-1.30
02h	-2.96	1Eh	-2.40	3Ah	-1.84	56h	-1.28
03h	-2.94	1Fh	-2.38	3Bh	-1.82	57h	-1.26
04h	--2.92	20h	-2.36	3Ch	-1.80	58h	-1.24
05h	-2.90	21h	-2.34	3Dh	-1.78	59h	-1.22
06h	-2.88	22h	-2.32	3Eh	-1.76	5Ah	-1.20
07h	-2.86	23h	-2.30	3Fh	-1.74	5Bh	-1.18
08h	-2.84	24h	-2.28	40h	-1.72	5Ch	-1.16
09h	-2.82	25h	-2.26	41h	-1.70	5Dh	-1.14
0Ah	-2.80	26h	-2.24	42h	-1.68	5Eh	-1.12
0Bh	-2.78	27h	-2.22	43h	-1.66	5Fh	-1.10
0Ch	-2.76	28h	-2.20	44h	-1.64	60h	-1.08
0Dh	-2.74	29h	-2.18	45h	-1.62	61h	-1.06
0Eh	-2.72	2Ah	-2.16	46h	-1.60	62h	-1.04
0Fh	-2.70	2Bh	-2.14	47h	-1.58	63h	-1.02
10h	-2.68	2Ch	-2.12	48h	-1.56	64h	-1.00
11h	-2.66	2Dh	-2.10	49h	-1.54	65h	-0.98
12h	-2.64	2Eh	-2.08	4Ah	-1.52	66h	-0.96
13h	-2.62	2Fh	-2.06	4Bh	-1.50	67h	-0.94
14h	-2.60	30h	-2.04	4Ch	-1.48	68h	-0.92
15h	-2.58	31h	-2.02	4Dh	-1.46	69h	-0.90
16h	-2.56	32h	-2.00	4Eh	-1.44	6Ah	-0.88
17h	-2.54	33h	-1.98	4Fh	-1.42	6Bh	-0.86
18h	-2.52	34h	-1.96	50h	-1.40	6Ch	-0.84
19h	-2.50	35h	-1.94	51h	-1.38	6Dh	-0.82
1Ah	-2.48	36h	-1.92	52h	-1.36	6Eh	-0.80
1Bh	-2.46	37h	-1.90	53h	-1.34	6Fh	-0.78

DAC Value	VCOM_C Voltage(V)	DAC Value	VCOM_C Voltage(V)	DAC Value	VCOM_C Voltage(V)	DAC Value	VCOM_C Voltage(V)
70h	-0.76	94h	-0.04	B8h	0.68	DCh	1.40
71h	-0.74	95h	-0.02	B9h	0.70	DDh	1.42
72h	-0.72	96h	0.00	BAh	0.72	DEh	1.44
73h	-0.70	97h	0.02	BBh	0.74	DFh	1.46
74h	-0.68	98h	0.04	BCh	0.76	E0h	1.48
75h	-0.66	99h	0.06	BDh	0.78	E1h	1.50
76h	-0.64	9Ah	0.08	BEh	0.80	E2h	1.52
77h	-0.62	9Bh	0.10	BFh	0.82	E3h	1.54
78h	-0.60	9Ch	0.12	C0h	0.84	E4h	1.56
79h	-0.58	9Dh	0.14	C1h	0.86	E5h	1.58
7Ah	-0.56	9Eh	0.16	C2h	0.88	E6h	1.60
7Bh	-0.54	9Fh	0.18	C3h	0.90	E7h	1.62
7Ch	-0.52	A0h	0.20	C4h	0.92	E8h	1.64
7Dh	-0.50	A1h	0.22	C5h	0.94	E9h	1.66
7Eh	-0.48	A2h	0.24	C6h	0.96	EAh	1.68
7Fh	-0.46	A3h	0.26	C7h	0.98	EBh	1.70
80h	-0.44	A4h	0.28	C8h	1.00	ECh	1.72
81h	-0.42	A5h	0.30	C9h	1.02	EDh	1.74
82h	-0.40	A6h	0.32	CAh	1.04	EEh	1.76
83h	-0.38	A7h	0.34	CBh	1.06	EFh	1.78
84h	-0.36	A8h	0.36	CCh	1.08	F0h	1.80
85h	-0.34	A9h	0.38	CDh	1.10	F1h	1.82
86h	-0.32	AAh	0.40	CEh	1.12	F2h	1.84
87h	-0.30	ABh	0.42	CFh	1.14	F3h	1.86
88h	-0.28	ACh	0.44	D0h	1.16	F4h	1.88
89h	-0.26	ADh	0.46	D1h	1.18	F5h	1.90
8Ah	-0.24	AEh	0.48	D2h	1.20	F6h	1.92
8Bh	-0.22	AFh	0.50	D3h	1.22	F7h	1.94
8Ch	-0.20	B0h	0.52	D4h	1.24	F8h	1.96
8Dh	-0.18	B1h	0.54	D5h	1.26	F9h	1.98
8Eh	-0.16	B2h	0.56	D6h	1.28	FAh	2.00
8Fh	-0.14	B3h	0.58	D7h	1.30	FBh	2.00
90h	-0.12	B4h	0.60	D8h	1.32	FCh	2.00
91h	-0.10	B5h	0.62	D9h	1.34	FDh	2.00
92h	-0.08	B6h	0.64	DAh	1.36	FEh	2.00
93h	-0.06	B7h	0.66	DBh	1.38	FFh	2.00

VGH Low temperature compensation Set (0x05h) --- Default Code 00h

Name	# of Bits	Access	Default	Description
---	7-3	W/R	**00000**	Reserved.
VGH_LT_OFS	2	W/R	**0**	0: Even 1: Odd
VGH_LT	1	W/R	**0**	VGH Low Temperature compensation offset Even: 2V to 8Vstep=2V. Refer to table below for details Odd: 3V to 9Vstep=2V. Refer to table below for details
	0	W/R	**0**	

0x05h [1]	0x05h [0]	0x05h [2]	VGH_LT Voltage(V)	0x05h [1]	0x05h [0]	0x05h [2]	VGH_LT Voltage(V)
0	0	0	VGL_NT+2V	0	0	1	VGL_NT+3V
0	1	0	VGL_NT+4V	0	1	1	VGL_NT+5V
1	0	0	VGL_NT+6V	1	0	1	VGL_NT+7V
1	1	0	VGL_NT+8V	1	1	1	VGL_NT+9V

Switching Frequency Set (0x06h) --- Default Code 00h

Name	# of Bits	Access	Default	Description
---	7-2	W/R	**000000**	Reserved.
SW_Fosc	1	W/R	**0**	PAVDD, NAVDD, VGH,VGL Operation Frequency Refer to table below for details
	0	W/R	**0**	

DAC Value	SW Freq.(KHz)	DAC Value	SW Freq.(KHz)	DAC Value	SW Freq.(KHz)	DAC Value	SW Freq.(KHz)
00h	600	01h	800	10h	1000	11h	2200

PAVDD ON Delay Time Set (0x07h) --- Default Code 01h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
PAVDD ON DELAY	3	W/R	**0**	PAVDD ON Delay Time Refer to table below for details
	2	W/R	**0**	
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	PAVDD Delay(ms)	DAC Value	PAVDD Delay(ms)	DAC Value	PAVDD Delay(ms)	DAC Value	PAVDD Delay(ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

PAVDD Soft-start Time Set (0x08h) --- Default Code 01h

Name	# of Bits	Access	Default	Description
	7-3	W/R	**00000**	Reserved
PAVDD Soft-start	2	W/R	**0**	PAVDD Soft-start Time Refer to table below for details
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	PAVDD SS(ms)	DAC Value	PAVDD SS(ms)	DAC Value	PAVDD SS(ms)	DAC Value	PAVDD SS(ms)
00h	5	02h	15	04h	25	06h	35
01h	10	03h	20	05h	30	07h	40

VGL ON Delay Time Set (0x09h) --- Default Code 05h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
VGL ON DELAY	3	W/R	**0**	VGL ON Delay Time Refer to table below for details
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	VGL Delay(ms)	DAC Value	VGL Delay(ms)	DAC Value	VGL Delay(ms)	DAC Value	VGL Delay(ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

VGL Soft-start Time Set (0x0Ah) --- Default Code 02h

Name	# of Bits	Access	Default	Description
	7-3	W/R	**00000**	Reserved
VGL Soft-start	2	W/R	**0**	VGL Soft-start Time Refer to table below for details
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	VGL Soft-start(ms)	DAC Value	VGL Soft-start(ms)	DAC Value	VGL Soft-start(ms)	DAC Value	VGL Soft-start(ms)
00h	3	02h	9	04h	15	06h	21
01h	6	03h	12	05h	18	07h	24

VGH ON Delay Time Set (0x0Bh) --- Default Code 05h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
VGH ON DELAY	3	W/R	**0**	VGH ON Delay Time Refer to table below for details
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	VGH Delay(ms)	DAC Value	VGH Delay(ms)	DAC Value	VGH Delay(ms)	DAC Value	VGH Delay(ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

VGH Soft-start Time Set (0x0Ch) --- Default Code 01h

Name	# of Bits	Access	Default	Description
	7-2	W/R	**000000**	Reserved
VGH Soft-start	1	W/R	**0**	VGH Soft-start Time Refer to table below for details
	0	W/R	**1**	

DAC Value	VGH Soft-start(ms)	DAC Value	VGH Soft-start(ms)	DAC Value	VGH Soft-start(ms)	DAC Value	VGH Soft-start(ms)
00h	5	01h	10	10h	15	11h	20

NAVDD ON Delay Time Set (0x0Dh) --- Default Code 03h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
NAVDD ON DELAY	3	W/R	**0**	NAVDD ON Delay Time Refer to table below for details
	2	W/R	**0**	
	1	W/R	**1**	
	0	W/R	**1**	

DAC Value	NAVDD Delay(ms)	DAC Value	NAVDD Delay(ms)	DAC Value	NAVDD Delay(ms)	DAC Value	NAVDD Delay(ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

NAVDD Soft-start Time Set (0x0Eh) --- Default Code 01h

Name	# of Bits	Access	Default	Description
	7-3	W/R	**00000**	Reserved
NAVDD Soft-start	2	W/R	**0**	NAVDD Soft-start Time Refer to table below for details
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	NAVDD Soft-start(ms)	DAC Value	NAVDD Soft-start(ms)	DAC Value	NAVDD Soft-start(ms)	DAC Value	NAVDD Soft-start(ms)
00h	5	02h	15	04h	25	06h	35
01h	10	03h	20	05h	30	07h	40

VCOM ON Delay Time Set (0x0Fh) --- Default Code 05h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
VCOM ON DELAY	3	W/R	**0**	VCOM ON Delay Time Refer to table below for details
	2	W/R	**1**	
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	VCOM Delay(ms)	DAC Value	VCOM Delay(ms)	DAC Value	VCOM Delay(ms)	DAC Value	VCOM Delay(ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

RESET ON Delay Time Set (0x10h) --- Default Code 01h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
RESET ON DELAY	3	W/R	**0**	RESET ON Delay Time Refer to table below for details
	2	W/R	**0**	
	1	W/R	**0**	
	0	W/R	**1**	

DAC Value	RESET Delay(ms)	DAC Value	RESET Delay(ms)	DAC Value	RESET Delay(ms)	DAC Value	RESET Delay(ms)
00h	0	04h	20	08h	40	0Ch	60
01h	5	05h	25	09h	45	0Dh	65
02h	10	06h	30	0Ah	50	0Eh	70
03h	15	07h	35	0Bh	55	0Fh	75

POWER OFF Delay Time Set (0x11h) --- Default Code 06h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
POWER OFF DELAY	3	W/R	**0**	POWER OFF Delay Time Refer to table below for details
	2	W/R	**1**	
	1	W/R	**1**	
	0	W/R	**0**	

DAC Value	POWER OFF Delay(ms)	DAC Value	POWER OFF Delay(ms)	DAC Value	POWER OFF Delay(ms)	DAC Value	POWER OFF Delay(ms)
00h	0	04h	12	08h	24	0Ch	36
01h	3	05h	15	09h	27	0Dh	39
02h	6	06h	18	0Ah	30	0Eh	42
03h	9	07h	21	0Bh	33	0Fh	45

Option 1 (0x12h) --- Default Code 06h

Name	# of Bits	Access	Default	Description
RESET_SYNC	7	W/R	**0**	0: Power off Delay 1: VGH SYNC.
VIN_DET	6	W/R	**0**	00: UVLO falling 01: 2.1V 10: 2.4V 11: 2.7V
	5	W/R	**0**	
PAVDD_DIS	4	W/R	**0**	0: ON 1: OFF
NAVDD_DIS	3	W/R	**0**	0: ON 1: OFF
VGH_DIS	2	W/R	**1**	0: ON 1: OFF
VGL_DIS	1	W/R	**1**	0: ON 1: OFF
VCOM_DIS	0	W/R	**0**	0: ON 1: OFF

Option 2 (0x13h) --- Default Code 55h

Name	# of Bits	Access	Default	Description
PAVDD_SR	7	W/R	**0**	00: Fast 01: Normal 10: Slow 11: Slowest
	6	W/R	**1**	
NAVDD_SR	5	W/R	**0**	00: Fast 01: Normal 10: Slow 11: Slowest
	4	W/R	**1**	
VGL_SR	3	W/R	**0**	00: Fast 01: Normal 10: Slow 11: Slowest
	2	W/R	**1**	
VGH_SR	1	W/R	**0**	00: Fast 01: Normal 10: Slow 11: Slowest
	0	W/R	**1**	

Option 3 (0x14h) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	7-6	W/R	**00**	Reserved
VGL_INT/EXT	5	W/R	**0**	0: Internal 1: External
FREQ._SPR	4	W/R	**0**	00: OFF 01: 3% 10: 6% 11: N/A
	3	W/R	**0**	
OTP	2	W/R	**0**	0: ON 1: OFF
UVP	1	W/R	**0**	0: ON 1: OFF
SCP	0	W/R	**0**	0: ON 1: OFF

VCOM_F Voltage Set (XX) --- Default Code 7Fh

Name	# of Bits	Access	Default	Description
VCOM_F	7	W/R	**0**	VCOM_F voltage adjustment from (VCOM_C-1.27)V to (VCOM_C+1.28)V step=0.01V. Refer to table below for details.
	6	W/R	**1**	
	5	W/R	**1**	
	4	W/R	**1**	
	3	W/R	**1**	
	2	W/R	**1**	
	1	W/R	**1**	
	0	W/R	**1**	

DAC Value	VCOM_F Voltage(V)	DAC Value	VCOM_F Voltage(V)	DAC Value	VCOM_F Voltage(V)	DAC Value	VCOM_F Voltage(V)
00h	-1.27	1Ch	-0.99	38h	-0.71	54h	-0.43
01h	-1.26	1Dh	-0.98	39h	-0.70	55h	-0.42
02h	-1.25	1Eh	-0.97	3Ah	-0.69	56h	-0.41
03h	-1.24	1Fh	-0.96	3Bh	-0.68	57h	-0.40
04h	-1.23	20h	-0.95	3Ch	-0.67	58h	-0.39
05h	-1.22	21h	-0.94	3Dh	-.066	59h	-0.38
06h	-1.21	22h	-0.93	3Eh	-0.65	5Ah	-0.37
07h	-1.20	23h	-0.92	3Fh	-0.64	5Bh	-0.36
08h	-1.19	24h	-0.91	40h	-0.63	5Ch	-0.35
09h	-1.18	25h	-0.90	41h	-0.62	5Dh	-0.34
0Ah	-1.17	26h	-0.89	42h	-0.61	5Eh	-0.33
0Bh	-1.16	27h	-0.88	43h	-0.60	5Fh	-0.32
0Ch	-1.15	28h	-0.87	44h	-0.59	60h	-0.31
0Dh	-1.14	29h	-0.86	45h	-0.58	61h	-0.30
0Eh	-1.13	2Ah	-0.85	46h	-0.57	62h	-0.29
0Fh	-1.12	2Bh	-0.84	47h	-0.56	63h	-0.28
10h	-1.11	2Ch	-0.83	48h	-0.55	64h	-0.27
11h	-1.10	2Dh	-0.82	49h	-0.54	65h	-0.26
12h	-1.09	2Eh	-0.81	4Ah	-0.53	66h	-0.25
13h	-1.08	2Fh	-0.80	4Bh	-0.52	67h	-0.24
14h	-1.07	30h	-0.79	4Ch	-0.51	68h	-0.23
15h	-1.06	31h	-0.78	4Dh	-0.50	69h	-0.22
16h	-1.05	32h	-0.77	4Eh	-0.49	6Ah	-0.21
17h	-1.04	33h	-0.76	4Fh	-0.48	6Bh	-0.20
18h	-1.03	34h	-0.75	50h	-0.47	6Ch	-0.19
19h	-1.02	35h	-0.74	51h	-0.46	6Dh	-0.18
1Ah	-1.01	36h	-0.73	52h	-0.45	6Eh	-0.17
1Bh	-1.00	37h	-0.72	53h	-0.44	6Fh	-0.16

DAC Value	VCOM_F Voltage(V)	DAC Value	VCOM_F Voltage(V)	DAC Value	VCOM_F Voltage(V)	DAC Value	VCOM_F Voltage(V)
70h	-0.15	94h	0.21	B8h	0.57	DCh	0.93
71h	-0.14	95h	0.22	B9h	0.58	DDh	0.94
72h	-0.13	96h	0.23	BAh	0.59	DEh	0.95
73h	-0.12	97h	0.24	BBh	0.60	DFh	0.96
74h	-0.11	98h	0.25	BCh	0.61	E0h	0.97
75h	-0.10	99h	0.26	BDh	0.62	E1h	0.98
76h	-0.09	9Ah	0.27	BEh	0.63	E2h	0.99
77h	-0.08	9Bh	0.28	BFh	0.64	E3h	1.00
78h	-0.07	9Ch	0.29	C0h	0.65	E4h	1.01
79h	-0.06	9Dh	0.30	C1h	0.66	E5h	1.02
7Ah	-0.05	9Eh	0.31	C2h	0.67	E6h	1.03
7Bh	-0.04	9Fh	0.32	C3h	0.68	E7h	1.04
7Ch	-0.03	A0h	0.33	C4h	0.69	E8h	1.05
7Dh	-0.02	A1h	0.34	C5h	0.70	E9h	1.06
7Eh	-0.01	A2h	0.35	C6h	0.71	EAh	1.07
7Fh	VCOM_C	A3h	0.36	C7h	0.72	EBh	1.08
80h	0.01	A4h	0.37	C8h	0.73	ECh	1.09
81h	0.02	A5h	0.38	C9h	0.74	EDh	1.10
82h	0.03	A6h	0.39	CAh	0.75	EEh	1.11
83h	0.04	A7h	0.40	CBh	0.76	EFh	1.12
84h	0.05	A8h	0.41	CCh	0.77	F0h	1.13
85h	0.06	A9h	0.42	CDh	0.78	F1h	1.14
86h	0.07	AAh	0.43	CEh	0.79	F2h	1.15
87h	0.08	ABh	0.44	CFh	0.80	F3h	1.16
88h	0.09	ACh	0.45	D0h	0.81	F4h	1.17
89h	0.10	ADh	0.46	D1h	0.82	F5h	1.18
8Ah	0.11	AEh	0.47	D2h	0.83	F6h	1.19
8Bh	0.12	AFh	0.48	D3h	0.84	F7h	1.20
8Ch	0.13	B0h	0.49	D4h	0.85	F8h	1.21
8Dh	0.14	B1h	0.50	D5h	0.86	F9h	1.22
8Eh	0.15	B2h	0.51	D6h	0.87	FAh	1.23
8Fh	0.16	B3h	0.52	D7h	0.88	FBh	1.24
90h	0.17	B4h	0.53	D8h	0.89	FCh	1.25
91h	0.18	B5h	0.54	D9h	0.90	FDh	1.26
92h	0.19	B6h	0.55	DAh	0.91	FEh	1.27
93h	0.20	B7h	0.56	DBh	0.92	FFh	1.28

Channel ON/OFF set (0x16h) --- Default Code 3Fh

Name	# of Bits	Access	Default	Description
VCOM/LDO_SEL	7	W/R	**0**	0: VCOM 1: LDO
VGH_IN_SEL	6	W/R	**0**	0: VGH Input Power is PAVDD 1: VGH Input Power is VIN
RESET_EN	5	W/R	**1**	0: OFF 1: ON
VCOM_EN	4	W/R	**1**	0: OFF 1: ON
NAVDD_EN	3	W/R	**1**	0: OFF 1: ON
VGH_EN	2	W/R	**1**	0: OFF 1: ON
VGL_EN	1	W/R	**1**	0: OFF 1: ON
PAVDD_EN	0	W/R	**1**	0: OFF 1: ON

Auto Refresh Option (0x17h) --- Default Code 0Ah

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
FAULT_ Behavior	3	W/R	**1**	0: FAULT not pull Low 1: FAULT Pull Low
Refreshing Time	2	W/R	**0**	00: 0.25s 01: 0.5s 10: 1s 11: 2s
	1	W/R	**1**	
AR_EN	0	W/R	**0**	0: OFF 1: ON

PAVDD OFF Delay Time Set (0x18h) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	7-3	W/R	**00000**	Reserved
PAVDD OFF DELAY	2	W/R	**0**	PAVDD OFF Delay Time Refer to table below for details
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	PAVDD OFF Delay(ms)	DAC Value	PAVDD OFF Delay(ms)	DAC Value	PAVDD OFF Delay(ms)	DAC Value	PAVDD OFF Delay(ms)
00h	0	02h	4	04h	8	06h	12
01h	2	03h	6	05h	10	07h	14

NAVDD OFF Delay Time Set (0x19h) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	7-3	W/R	**00000**	Reserved
NAVDD OFF DELAY	2	W/R	**0**	NAVDD OFF Delay Time Refer to table below for details
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	NAVDD OFF Delay(ms)	DAC Value	NAVDD OFF Delay(ms)	DAC Value	NAVDD OFF Delay(ms)	DAC Value	NAVDD OFF Delay(ms)
00h	0	02h	4	04h	8	06h	12
01h	2	03h	6	05h	10	07h	14

VGH OFF Delay Time Set (0x1Ah) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	7-3	W/R	**00000**	Reserved
VGH OFF DELAY	2	W/R	**0**	VGH OFF Delay Time Refer to table below for details
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VGH OFF Delay(ms)	DAC Value	VGH OFF Delay(ms)	DAC Value	VGH OFF Delay(ms)	DAC Value	VGH OFF Delay(ms)
00h	0	02h	4	04h	8	06h	12
01h	2	03h	6	05h	10	07h	14

VGL OFF Delay Time Set (0x1Bh) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	7-3	W/R	**00000**	Reserved
VGL OFF DELAY	2	W/R	**0**	VGL OFF Delay Time Refer to table below for details
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VGL OFF Delay(ms)	DAC Value	VGL OFF Delay(ms)	DAC Value	VGL OFF Delay(ms)	DAC Value	VGL OFF Delay(ms)
00h	0	02h	4	04h	8	06h	12
01h	2	03h	6	05h	10	07h	14

Option (0x1Ch) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
FAULT_ Clear	3	W/R	**0**	0: Not Clear 1: Clear
VCOM OFF DELAY	2	W/R	**0**	VCOM OFF Delay Time Refer to table below for details
	1	W/R	**0**	
	0	W/R	**0**	

DAC Value	VCOM OFF Delay(ms)	DAC Value	VCOM OFF Delay(ms)	DAC Value	VCOM OFF Delay(ms)	DAC Value	VCOM OFF Delay(ms)
00h	0	02h	4	04h	8	06h	12
01h	2	03h	6	05h	10	07h	14

FAULT Analysis (0x1Dh) --- Default Code 00h

Name	# of Bits	Access	Default	Description
	7-4	W/R	**0000**	Reserved
PAVDD FAULT	3	W/R	**0**	0: No Fault 1: Fault Happen
VGL FAULT	2	W/R	**0**	0: No Fault 1: Fault Happen
VGH FAULT	1	W/R	**0**	0: No Fault 1: Fault Happen
NAVDD FAULT	0	W/R	**0**	0: No Fault 1: Fault Happen

Protection Behavior of Each Output Channels

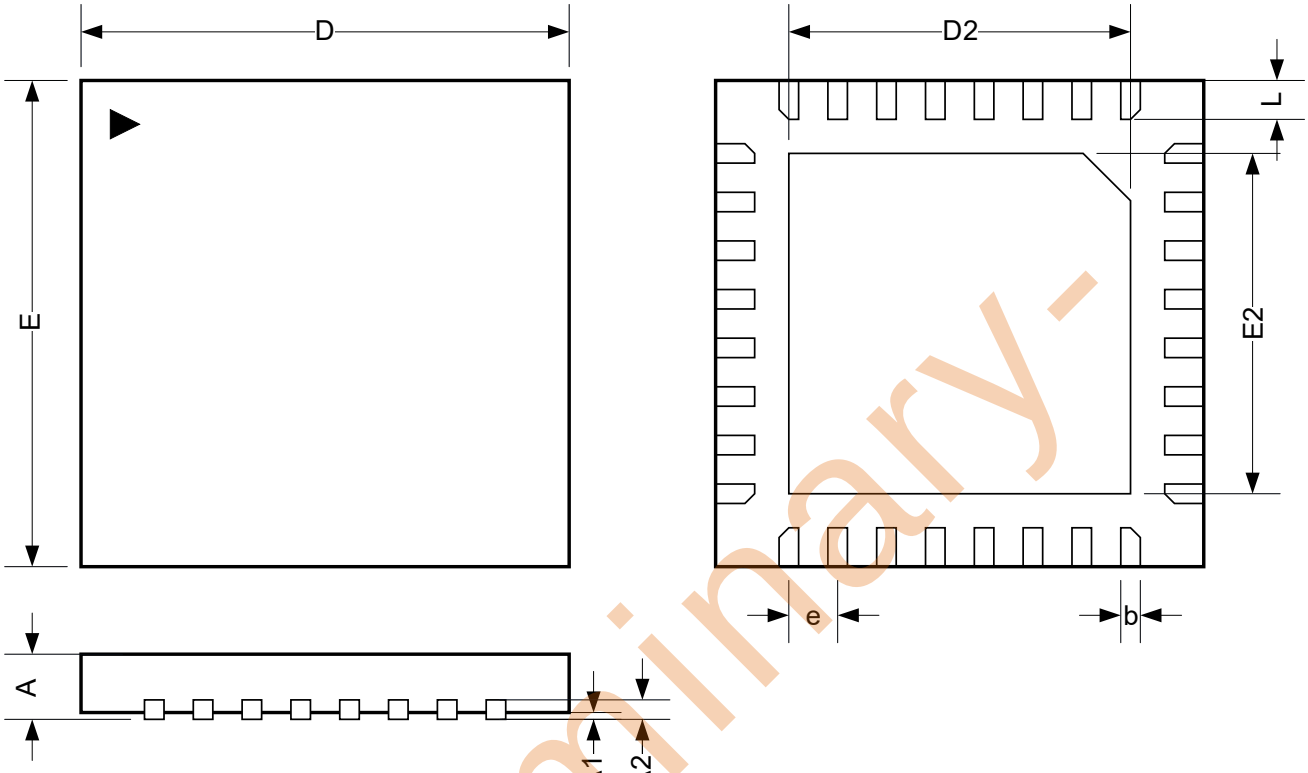
Block	Protection	Work Condition	Behavior	Recovery
GENERAL	UVLO	VIN Falling < UVLO_F	IC Shutdown	VIN Rising >UVLO_R
	TSD	T_A = 150℃	IC Shutdown	VIN Rising >UVLO_R
PAVDD	OVP	PAVDD>PAVDD*120%	LX Stop Switching	Vout<OVP-Hys,Hys=0.5V(typ.) LX switch at next clk.
	UVP	PAVDD<PAVDD*70% And duration time is about 50ms	IC shutdown and latch	1. VIN re-power up(duration time ≥50ms) 2. EN toggle again(duration time ≥50ms)
	SCP3	PAVDD<VIN-0.2V After Softstart finish	LX stop switching, IC shutdown and latch	1. VIN re-power up 2. EN toggle again
	SCP2	PAVDD<1.25V Power on pre-charge Or Restart PAVDD	LX stop switching, IC shutdown and latch	1. VIN re-power up 2. EN toggle again
	SCP1	PAVDD<PAVDD*30%	LX stop switching, IC shutdown and latch	1. VIN re-power up 2. EN toggle again
NAVDD	OVP	NAVDD>NAVDD*120%	LXN Stop Switching	Vout<OVP-Hys, Hys=0.6V(typ.) LXN switch at next clk.
	UVP	NAVDD<NAVDD*70% And duration time is about 50ms	IC shutdown and latch	1. VIN re-power up(duration time ≥50ms) 2. EN toggle again(duration time ≥50ms)
	SCP	NAVDD<NAVDD*30%	LXN stop switching, IC shutdown and latch	1. VIN re-power up 2. EN toggle again
VGH	OVP	VGH>VGH*120% VGH+VGH_LT<28.5V	LXP Stop Switching	VGH_OVP=1.2*VGH, Hys=0.3V(typ.), LXP switch at next clk.
	OVP	VGH_OVP=33V VGH+VGH_LT>=28.5V	LXP Stop Switching	VGH_OVP=33V, Hys=0.3V(typ.), LXP switch at next clk.
	UVP	VGH<VGH*70% and Duration time is about 50ms	IC shutdown and latch	1. VIN re-power up(duration time ≥50ms) 2. EN toggle again(duration time ≥50ms)
	SCP	VGH<VGH*30%	LXP stop switching, IC shutdown and latch	1. VIN re-power up 2. EN toggle again
VGL	UVP	VGL<VGL*70% and duration time is about 50ms	IC shutdown and latch	1. VIN re-power up(duration time ≥50ms) 2. EN toggle again(duration time ≥50ms)
	SCP	VGL>VGL*30%	CX1/CX2 stop switching, IC shutdown and latch	1. VIN re-power up 2. EN toggle again
VCOM	OCP	VCOM source/sink current >± 350mA(typ.)	Fold back the output current at 100mA level	Affter the abnormal load is removed

FAULT Behavior and Protections

Block	Triggering Protection	FAULT Pin Behavior	Recovery
PAVDD	OVP	High(Normal state)	---
	UVP	Low	1. VIN re-power up 2. EN toggle again.
	SCP	Low (Fault pin toggle one time)	1. VIN re-power up 2. EN toggle again.
	OTP	Low	IC Temperature<OTP-Hys. Hys=20℃(tpy.)
NAVDD	OVP	High(Normal state)	---
	UVP	Low	1. VIN re-power up 2. EN toggle again.
	SCP	Low	1. VIN re-power up 2. EN toggle again.
	OTP	Low	IC Temperature<OTP-Hys. Hys=20℃(tpy.)
VGH	OVP	High(Normal state)	---
	UVP	Low	1. VIN re-power up 2. EN toggle again.
	SCP	Low	1. VIN re-power up 2. EN toggle again.
	OTP	Low	IC Temperature<OTP-Hys. Hys=20℃(tpy.)
VGL	OVP	High(Normal state)	---
	UVP	Low	1. VIN re-power up 2. EN toggle again.
	SCP	Low (The short-circuit condition needs to keep until IC re-power up at next time)	1. VIN re-power up 2. EN toggle again.
	OTP	Low	IC Temperature<OTP-Hys. Hys=20℃(tpy.)
VCOM	OCP	High(Normal state)	---
	OTP	Low	IC Temperature<OTP-Hys. Hys=20℃(tpy.)

Packaging Information

QFN5X5-32



Symbol	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	0.750	0.800	0.0276	0.0295	0.0315
A1	0.000		0.050	0.0000		0.0020
A2		0.2REF			0.0079	
D	4.95	5.00	5.05	0.1949	0.1968	0.1988
E	4.95	5.00	5.05	0.1949	0.1968	0.1988
D1	3.40	3.70	3.75	0.1338	0.1457	0.1476
E1	3.40	3.70	3.75	0.1338	0.1457	0.1476
b	0.2	0.25	0.3	0.0079	0.0098	0.0118
e		0.5BSC			0.0197BSC	
L	0.35	0.40	0.45	0.0138	0.0157	0.0177