LPQ3970

1.0A Low Dropout High PSRR Low Noise LDO

Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified with the following results:
  - Device temperature grade1
  - Device HBM ESD classification level H3A
  - Device CDM ESD classification level C3
- Wide Input Voltage Range: 1.6V to 5.5V
- Adjustable Output Voltage: 0.55V to 5.0V
- Maximum Load Current Up to 1.0A
- High PSRR: 70dB@1kHz, V_{OUT}=3.3V
- Low Quiescent Current: 60μA
- Low Noise: 20μV_{RMS}@V_{OUT}=1.2V, C_{NR}=0.47μF
- Low Dropout Voltage:
  - 130mV @ 1000mA Load, V_{OUT}=3.3V
  - 260mV @ 1000mA Load, V_{OUT}=1.8V
- Output Voltage Accuracy: ±2% @ 1mA typical
- Thermal Shutdown Protection
- Excellent Load/Line Transient Response
- Line Regulation: 0.01%/V typical
- Load Regulation: 5mV typical
- Robust ESD capability:
  - Human Body Model: 4kV
  - Charged Device Model: 1kV
- Package: DFN3x3-8
- RoHS Compliant and 100% Lead (Pb)-Free

Applications

- Automotive RF Power Supply
- Automotive Telematics Power Supply
- Automotive ECU Power Supply
- Automotive Infotainment and Cluster System
- Post regulation

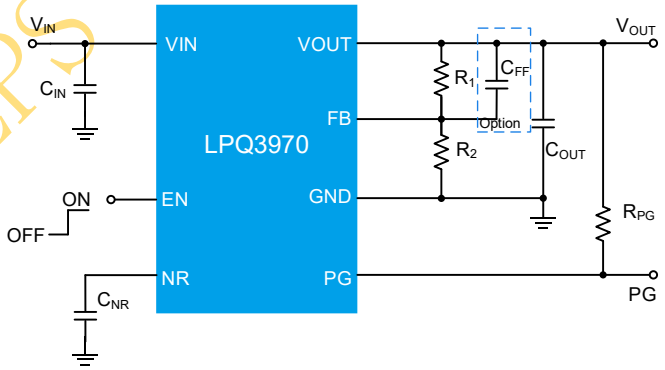
General Description

The LPQ3970 family are high performance low dropout（LDO） voltage regulators with high PSRR, low noise, fast transient response, and high accuracy. The devices are suitable for the applications that require regulated supplies of up to 1.0A load current.

The LPQ3970 family include adjustable output voltages of 0.55V to 5.0V with an external resister divider. The devices are stable with an effective 1.0μF or greater ceramic output capacitor. The devices are protected from short circuit by a current limit function and from over-heating by a thermal overload protection.

The devices are available in standard DFN3x3-8 package.

Typical Application Circuit



Order Information

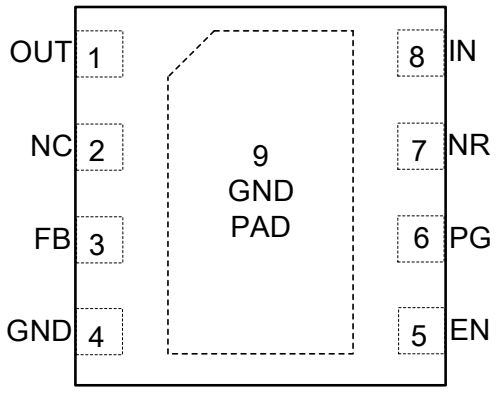
LPQ3970 □□□ □

- F: Pb Free
- Package Type
  - QV: DFN3x3-8
- OUT Voltage
  - A: Adjustable

Device Information

Part Number	Top Marking	OUT Voltage	Moisture Sensitivity Level	Package	Shipping
LPQ3970AQVF	LPS LPQ3970 YWX	Adjustable	MSL3	DFN3x3-8	5K/REEL
Marking indication: Y: Year code. W: Week code. X: Batch numbers.					

Pin Diagram



DFN3x3-8（top view）

Pin Description

Pin#	Name	Description
1	OUT	Output pin. Bypass with a minimum effective 1μF ceramic capacitor from this pin to ground. Place the capacitor as close as to the pin as possible.
3	FB	Feedback pin. This is used to set the output voltage. The reference voltage is 0.55V.
4	GND	Ground.
5	EN	Enable pin. Active high. Driving EN over 1V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode. Don't leave it floating.
6	PG	Power-good output. Open-drain. A pullup resistor is required, if the power-good functionality is not being used, ground this pin or leave floating.
7	NR	Noise-reduction and soft-start pin. Connecting an external capacitor between this pin and ground reduces reference voltage noise and also enables the soft-start function.
8	IN	Supply input pin. Must be closely decoupled to GND with a minimum effective 1μF ceramic capacitor. Place the capacitor as close as to the pin as possible.
2	NC	No connection.
9	GND PAD	Thermal PAD. Connect exposed pad to GND plane for optimal thermal performance.

Absolute Maximum Ratings (Note 1)

IN, PG Pin to GND ---------- -0.3~6.5V
OUT, EN, FB Pin to GND ---------- -0.3~V_{IN}
Maximum Junction Temperature (T_J) ---------- 150℃
Maximum Soldering Temperature (at leads, 10 sec) ---------- 260℃

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Susceptibility

HBM (Human Body Model) ---------- 4kV
CDM (Charged Device Model) ---------- 1kV

Recommended Operating Conditions

Input Voltage ---------- 1.6 V to 5.5V
Operating Junction Temperature Range (T_J) ----------40℃ to 150℃
Ambient Temperature Range ---------- -40℃ to 85℃

Electrical Characteristics

(The specifications are at T_A=25℃, LPQ3970AQVF, V_{IN} = V_{OUT}+1V, C_{IN}=C_{OUT}=1μF, R2=20kΩ, R1=100kΩ, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1mA, C_{NR}=NC, C_{FF}=NC, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT VOLTAGE AND CURRENT						
V_{IN}	Input Voltage Operation Range		1.6		5.5	V
V_{IN_UVLO}	Under Voltage Lockout	VIN rising	1.21	1.33	1.47	V
		VIN falling	1.17	1.29	1.42	V
$V_{IN\_UVLO\_HYS}$	UVLO hysteresis			40		mV
I_Q	DC Supply Quiescent Current	V_{EN}=V_{IN}, I_{LOAD}=0mA		60		μA
I_{SD}	Shutdown Current	V_{EN}=0V			1	μA
OUTPUT VOLTAGE AND CURRENT						
V_{OUT}	Output Voltage Accuracy	I_{LOAD}=1mA	3.234	3.3	3.366	V
V_{FB}	Feedback Voltage	I_{LOAD}=1mA	0.54	0.55	0.56	V
I_{FB}	FB pin Current			0.01		μA
$\frac{\Delta V_{LINE}}{\Delta V_{IN} \times V_{OUT}}$	Output Voltage Line Regulation	V_{IN}=V_{OUT}+0.5V~6V I_{LOAD}=1mA		0.02		%/V
ΔV_{LOAD}	Output Voltage Load Regulation	I_{LOAD} from 1mA to 1000mA		5	30	mV
I_{LIMIT}	Load Current Limit	V_{OUT}=0.9*$V_{OUT(Nom)}$	1200	1500	1800	mA
I_{SHORT}	Short Current Limit	V_{OUT} short to GND	500	700	900	mA
V_{DROP}	Dropout Voltage	V_{OUT}=3.3V, I_{LOAD}=1000mA		150	300	mV
		V_{OUT}=3.3V, I_{LOAD}=500mA		75	150	mV
		V_{OUT}=1.8V, I_{LOAD}=1000mA		250		mV
		V_{OUT}=1.8V, I_{LOAD}=500mA		120		mV
e_N	Output Noise	10Hz to 100kHz, V_{OUT}=0.9V, I_{LOAD}=20mA, C_{NR}=NC		50		μV_{RMS}
		10Hz to 100kHz, V_{OUT}=1.2V, I_{LOAD}=20mA, CNR=470nF		20		μV_{RMS}
PSRR	Power Supply Rejection Ratio	V_{IN}=(V_{OUT}+1V)$_{DC}$+0.2V_{P-P}, C_{NR}=470nF, I_{OUT}=20mA, V_{OUT}=3.3V, f=1kHz		71		dB
		f=10kHz		56		dB
		f=100kHz		43		dB
R_{DIS}	Auto-Discharge Resistance			100		Ω
SOFTSTART						
t_{SS}	Softstart time	$V_{OUT(NOM)}$=3.3V, C_{NR}=10nF From EN high to VOUT=VOUT(NOM)*95%		1.7		ms
		$V_{OUT(NOM)}$=3.3V, C_{NR}=470nF From EN high to VOUT=VOUT(NOM)*95%		78		ms
I_{NR}	NR output Current			6		μA

THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold			150		℃
T_{SD_HYS}	Thermal Shutdown Hysteresis			20		℃
EN LOGIC						
V_{ENH}	EN Logic High Voltage		1.0			V
V_{ENL}	EN Logic Low Voltage				0.4	V
I_{EN}	EN Input Current	V_{EN}= 5.5V	-10		10	nA
PG LOGIC						
PG_{HTH}	PG High threshold	V_{OUT} rising	89	92	96	$\%V_{OUT(NOM)}$
PG_{LTH}	PG Low threshold	V_{OUT} falling	86	90	93	$\%V_{OUT(NOM)}$
PG_{HYS}	PG hysteresis			2		$\%V_{OUT(NOM)}$
I_{PG_LKG}	PG leakage Current	V_{EN}=V_{PG}=5.5V		5		nA
V_{OL_PG}	PG pin low-level output voltage	I_{SINK}=2mA		150	300	mV
V_{OH_PG}	PG pin high-level output voltage (push-pull version)	I_{SOURCE}=1mA	0.8* V_{OUT}		V_{OUT}	V
t_{PGDH}	PG delay time rising	Time from V_{OUT} higher 92%$V_{OUT(NOM)}$ to PG rising to 20% target		165		μs
t_{PGDL}	PG delay time falling	Time from V_{OUT} lower 90%$V_{OUT(NOM)}$ to PG falling to 80% target		12		μs

Typical Characteristics

(T_J = 25℃, V_{IN} = $V_{OUT(NOM)}$ + 1V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1.0μF, LPQ3970AQVF, R2=20kΩ, R1=100kΩ, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1mA, C_{NR}=NC, C_{FF}=NC, unless otherwise noted.unless otherwise noted.)

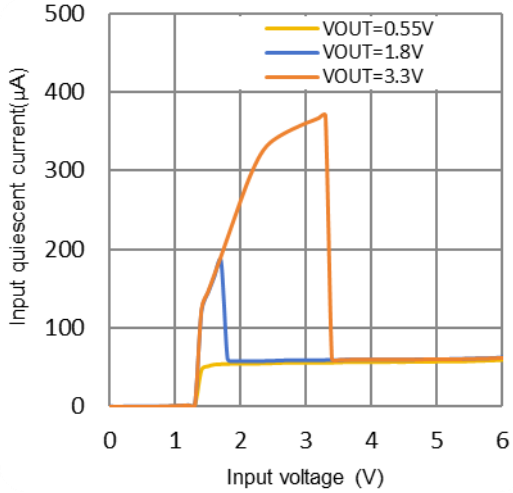


Figure 1 Quiescent current vs Input voltage,

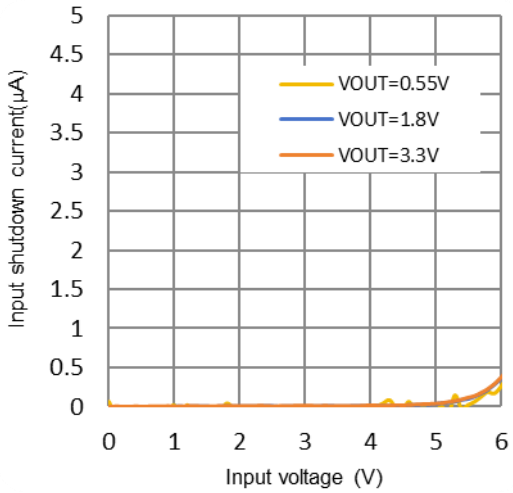


Figure 2. Shutdown current vs Input voltage

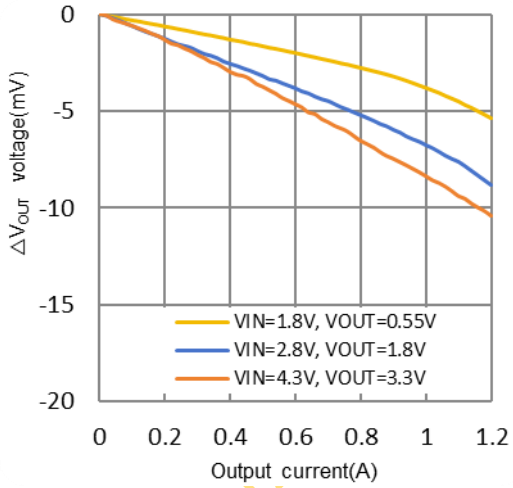


Figure 3 Load regulation: △VOUT vs output current

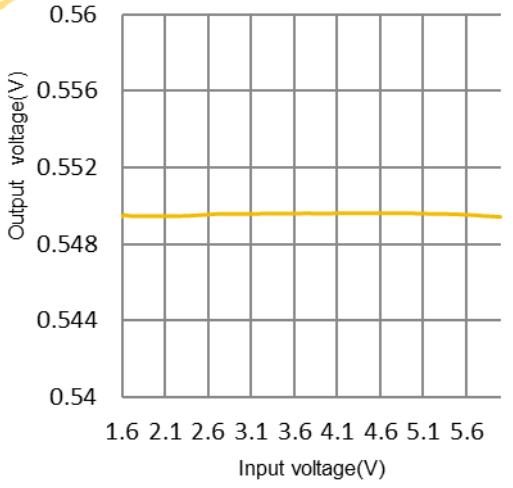


Figure 4 FB voltage vs input voltage

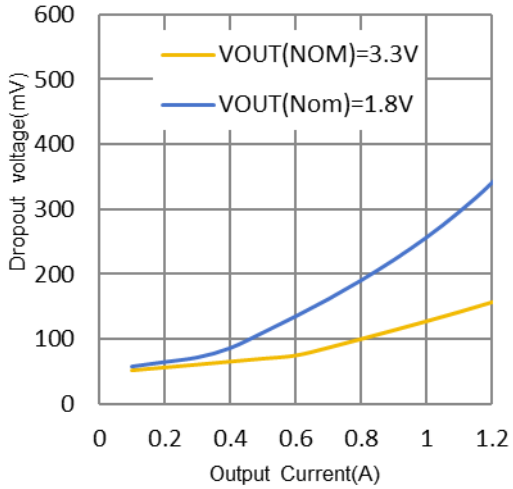


Figure 5. Dropout Voltage vs Output Current

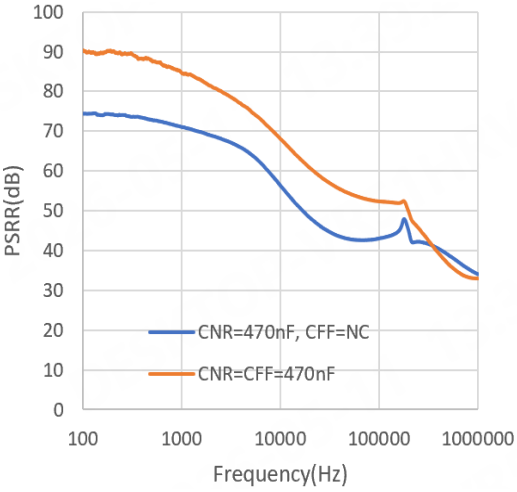


Figure 6 PSRR vs Frequency
V_{IN}=4.3V, V_{OUT}=3.3V, I_{OUT}=20mA

Start up and Shutdown with EN:(I_{OUT}=1mA)

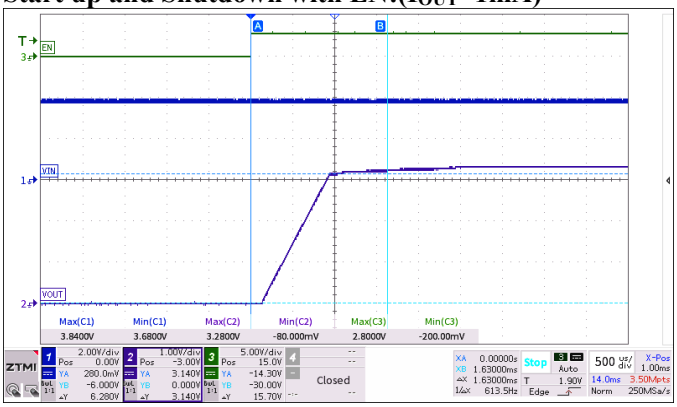


Figure 7 Start up with EN on, C_{NR}=10nF
V_{IN}=3.8V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1mA

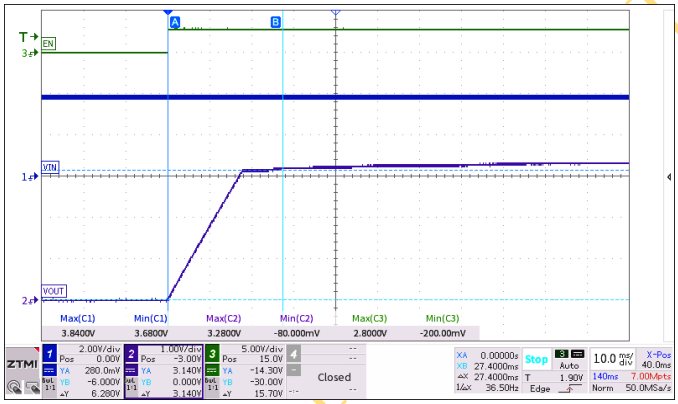


Figure 8 Start up with EN on, C_{NR}=200nF
V_{IN}=3.8V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1mA

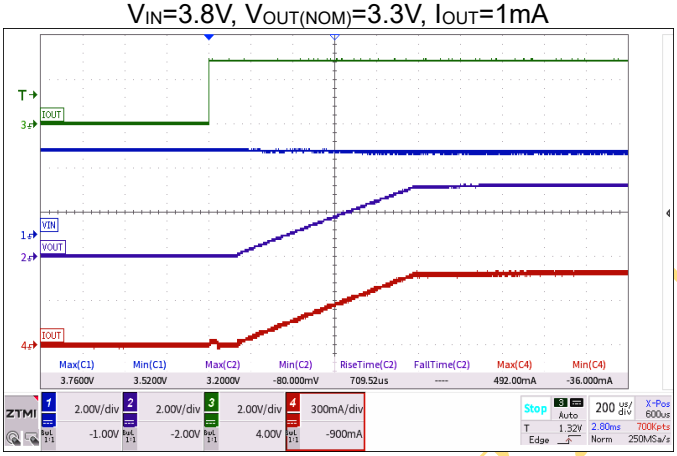


Figure 9 Start up with EN on, C_{NR}=10nF
V_{IN}=3.8V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1200mA

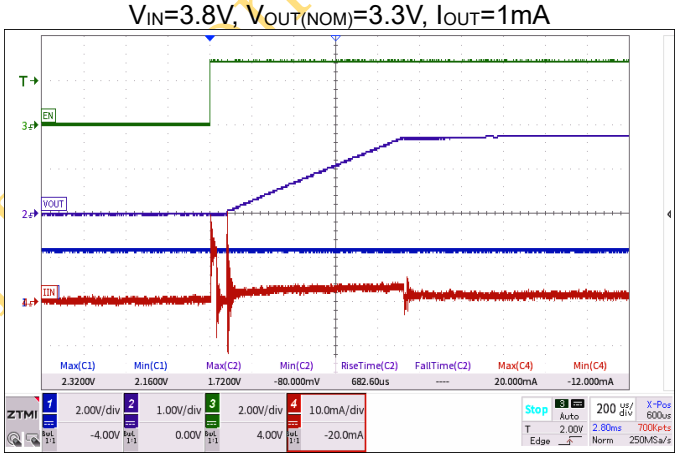


Figure 10 Start up with EN on, C_{NR}=10nF
V_{IN}=2.3V, $V_{OUT(NOM)}$=1.8V, I_{OUT}=1mA

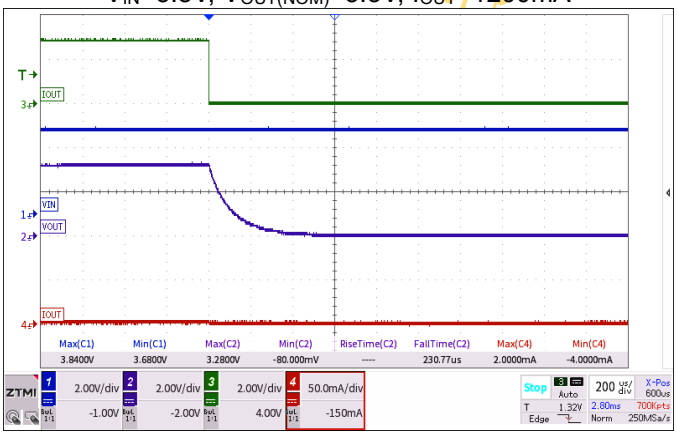


Figure 11 Shutdown with EN off, C_{NR}=10nF
V_{IN}=3.8V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1mA

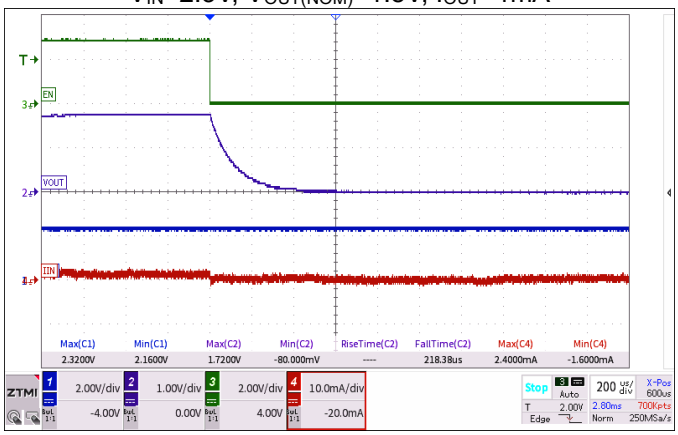


Figure 12 shutdown with EN off, C_{NR}=10nF
V_{IN}=2.3V, $V_{OUT(NOM)}$=1.8V, I_{OUT}=1mA

Line Transient:

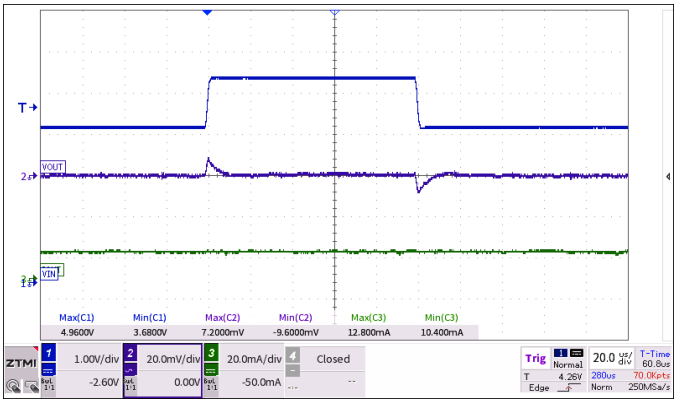


Figure 13 Line transient waveform, C_{NR}=10nF
V_{IN}=3.8<->5V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=10mA

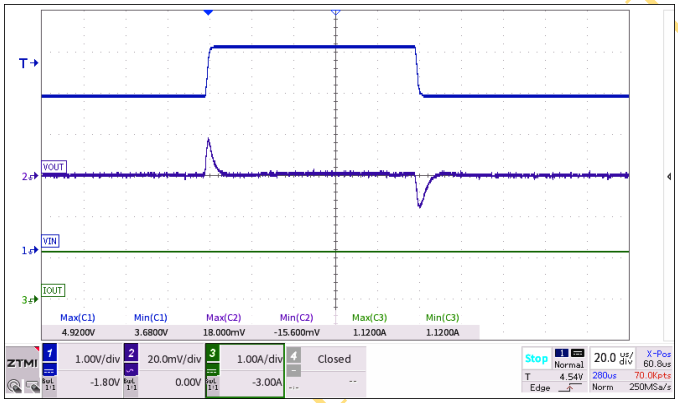


Figure 14 Line transient waveform, C_{NR}=10nF
V_{IN}=3.8<->5V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1200mA

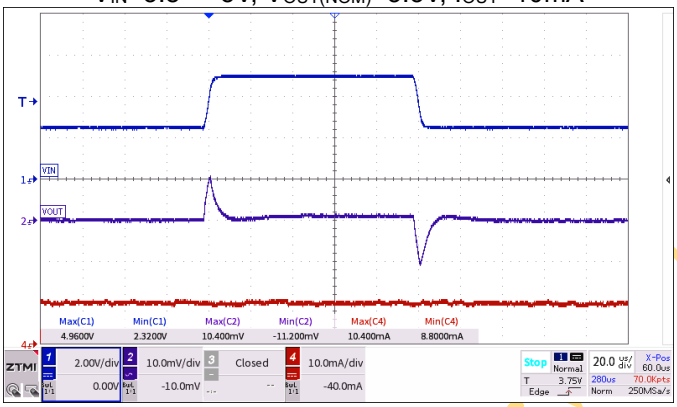


Figure 15 Line transient waveform, C_{NR}=10nF
V_{IN}=2.5<->5V, $V_{OUT(NOM)}$=1.8V, I_{OUT}=10mA

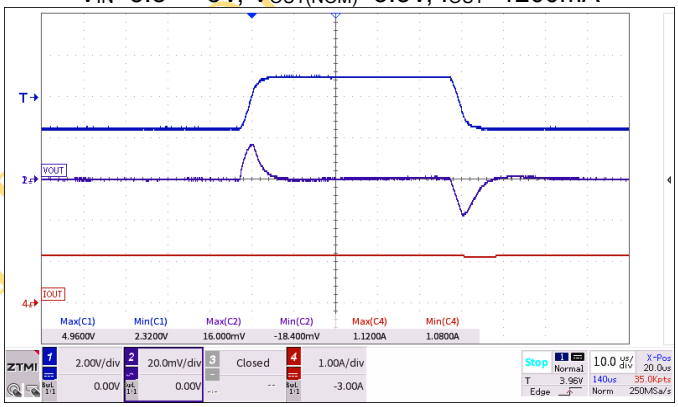


Figure 16 Line transient waveform, C_{NR}=10nF
V_{IN}=2.5<->5V, $V_{OUT(NOM)}$=1.8V, I_{OUT}=1200mA

Load Transient:

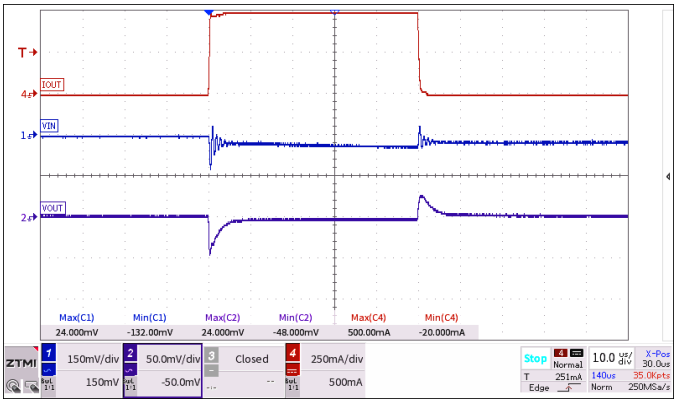


Figure 17 Load transient waveform, C_{NR}=10nF
V_{IN}=4.3V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=1<->500mA

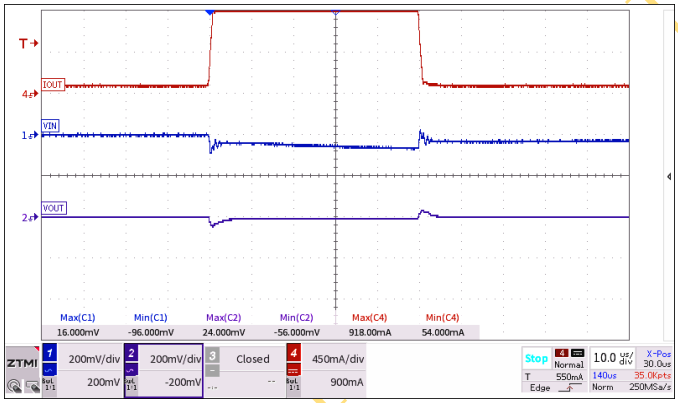


Figure 18 Load transient waveform, C_{NR}=10nF
V_{IN}=4.3V, $V_{OUT(NOM)}$=3.3V, I_{OUT}=100<->1000mA

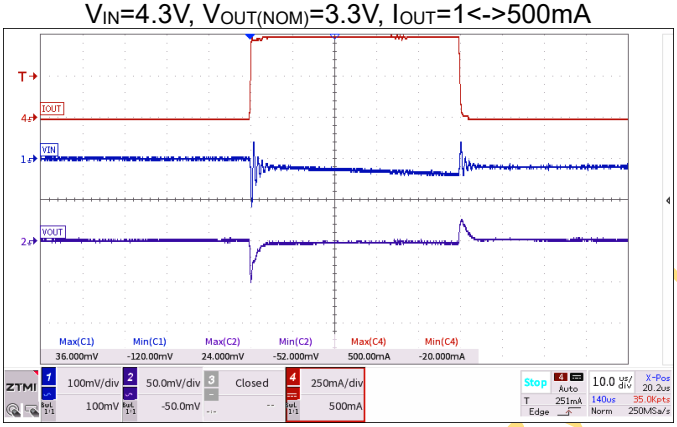


Figure 19 Load transient waveform, C_{NR}=10nF
V_{IN}=2.8V, $V_{OUT(NOM)}$=1.8V, I_{OUT}=1<->500mA

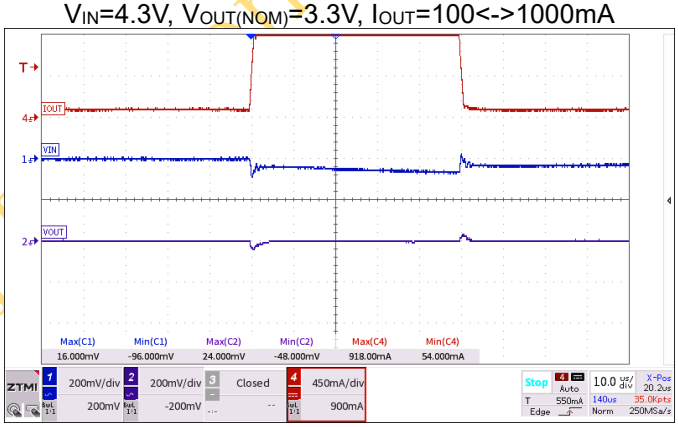


Figure 20 Load transient waveform, C_{NR}=10nF
V_{IN}=2.8V, $V_{OUT(NOM)}$=1.8V, I_{OUT}=100<->1000mA

Functional Block Diagram

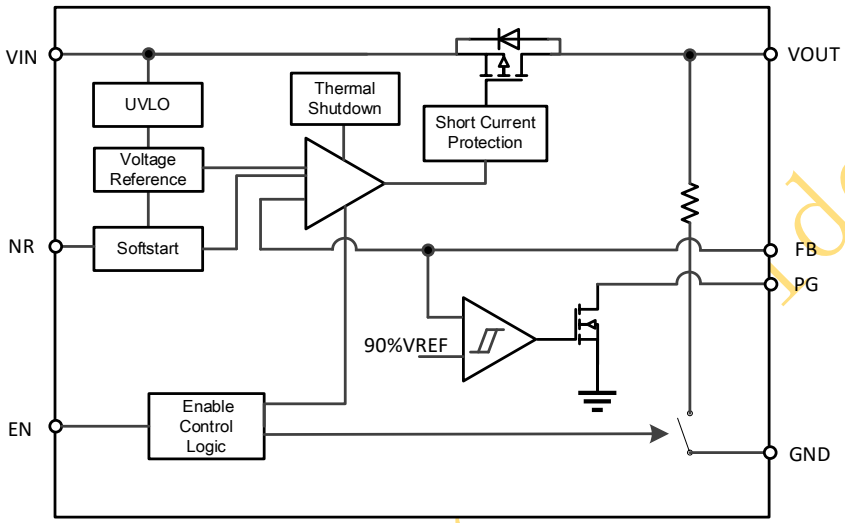


Figure 21. LPQ3970 functional block diagram

Detailed Description

Overview

The LPQ3970 family are high performance, low dropout linear regulators with adjustable voltage of 0.55V to 5V and up to 1.0A output current capability. Optimized for using with ceramic capacitors, the device provides excellent transient performance.

Internally, the devices consist of a voltage reference, an enable control logic, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares a reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

Adjustable Output Voltage

LPQ3970 output voltage is adjustable, which is programmed by an external resistor divider. The output can be calculated be by the following equation:

$$V_{OUT} = (1 + R_1 / R_2) \times V_{REF}$$

Where V_{REF} is the internal reference voltage, which is 0.55V in LPQ3970A. It recommends R2 resistance ranges from 10kΩ to 100kΩ.

Enable Function

The EN pin is an active high logic input pin. The internal power element is turned off when EN pin is tied low. When the EN pin is pulled high, the LPQ3970 will be activated and output voltage according to the setting.

Programmable Soft Start

The LPQ3970 series integrates a programmable soft-start function to control the output voltage ramp-up slew rate and start-up time by the external NR pin.

The relationship between the capacitance of external capacitor at the NR pin and the output softstart time can be showed with below equation.

$$t_{SS} = 1.82 \times V_{NR} \times C_{NR} / I_{NR}$$

Where, the typical value of V_{NR} is 0.55V, the typical value of INR is 6 μA, and C_{NR} is the capacitance of external capacitor at the NR pin.

Dropout Voltage

When (VIN – VOUT) is less than the dropout voltage (VDO), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the RDS(ON) of the PMOS pass element. VDO scales approximately with output current because the PMOS device behaves like a resistor in dropout mode. As with any linear regulator, PSRR and transient response degrade as (VIN – VOUT) approaches dropout operation.

Some applications have transients that place the LDO into dropout, such as slower ramps on VIN during start-up.

As with other LDOs, the output may overshoot on recovery from these conditions. A ramping input supply causes an LDO to overshoot on start-up. Use an enable signal to avoid this condition.

Line transients out of dropout can also cause overshoot on the output of the regulator. These overshoots are caused by the error amplifier having to drive the gate capacitance of the pass element and bring the gate back to the correct voltage for proper regulation. When the LDO is placed in dropout, the gate voltage (VGS) is pulled all the way down to ground to give the pass device the lowest on-resistance as possible. However, if a line transient occurs when the device is in dropout, the loop is not in regulation and can cause the output to overshoot until the loop responds and the output current pulls the output voltage back down into regulation. If these transients are not acceptable, then continue to add input capacitance in the system until the transient is slow enough to reduce the overshoot.

Power-Good Function

The power-good circuit monitors the voltage at the feedback pin to indicate the status of the output voltage. When the output voltage falls below the PG threshold voltage (P_{GLTH}), the PG pin open-drain output engages and pulls the PG pin close to GND. When the output voltage exceeds P_{GHTH}, the PG pin becomes high impedance. The open-drain output requires a pullup resistor. By connecting a pullup resistor to an external supply, any downstream device can receive power-good as a logic signal that can be used for sequencing.

Additionally, the open-drain output can be tied to other open-drain outputs to implement AND logic. Make sure that the external pullup supply voltage results in a valid logic signal for the receiving device. Using a pullup resistor from 10 kΩ to 100 kΩ is recommended.

Auto Discharge

The LPQ3970 has a quick discharge function. When the device is disabled by the pulled-down EN pin, a discharge resistor is connected between VOUT and GND. The resistance is 100Ω typically.

Short Current Limit Protection

When the output current at the VOUT pin is higher than current limit threshold or the VOUT pin is short to GND, the short current limit protection will be triggered and clamp the output current to approximately 700mA to protect the regulator from damage due to overheating.

Thermal Shutdown Protection

When the internal junction temperature of LPQ3970 family devices exceed the junction thermal shutdown threshold (150℃ typical), the devices will shut down the output, after the junction temperature falls below 130℃ , the VOUT voltage will resume.

Application Description

Thermal Consideration

The reason that causes thermal shutdown protection of an LPQ3970 device is the power dissipation. Nearly all of the power dissipation is generated by the internal PMOS pass device. The power dissipation can be calculated approximately as,

$$P_D = (V_{IN} - V_{OUT}) \times I_{LOAD}$$

where P_D is the power dissipation.

For example, a 1V output voltage and the device has the maximum input voltage of 5.5V and the maximum load current of 1000mA. In this situation, the device dissipates the maximum power,

$$P_{Dmax} = (5.5V - 1.0V) \times 1.0A = 4.5W$$

This power dissipation of the LDO device in the DFN3x3-8 package will trigger thermal shutdown protection at high ambient temperature. Then a trade-off must be made between the output current, cost, and thermal requirements of the application.

Input Capacitor

Like all low dropout linear regulators, low-source impedance is necessary for the stable operation of the LDO. An effective 1μF-10uF capacitance ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitches and noise. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

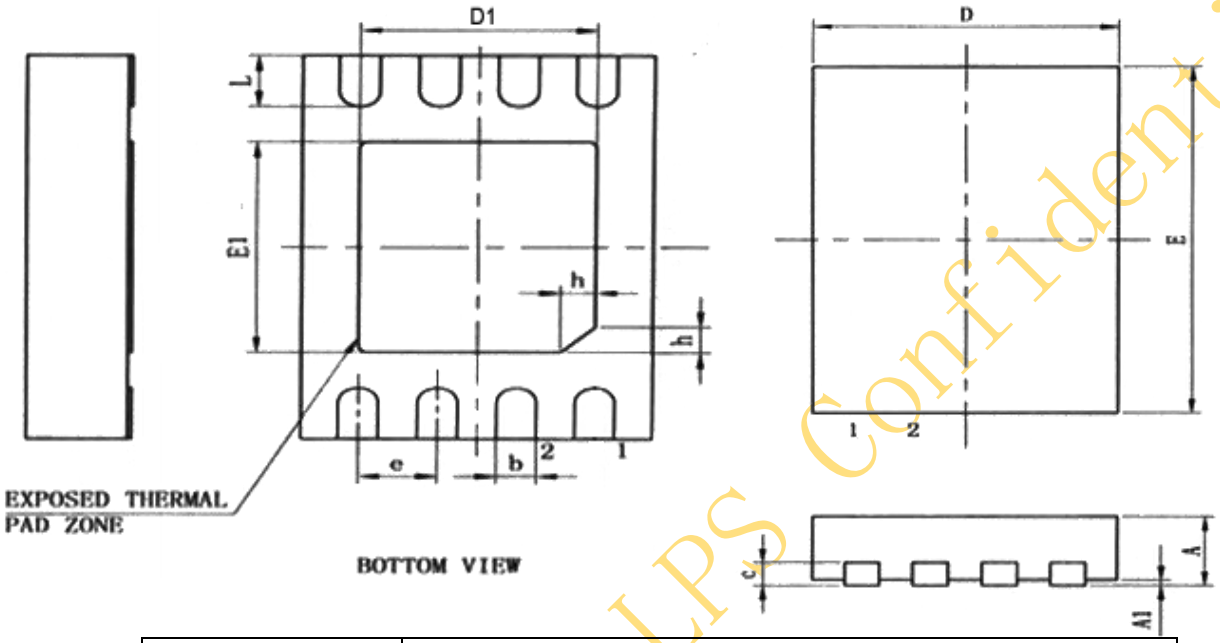
The LPQ3970 requires a minimum effective capacitance of 1 μF for output voltage stability. The recommended output effective capacitance is from 1μF to 100μF, Equivalent Series Resistance (ESR) is from 5mΩ to 100mΩ, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitor should be located as close to the LDO output as practically possible.

Layout Considerations

For best overall performance, place all the circuit components on the same side of the circuit board and as near as practically possible to the respective LDO pins. Place ground return connections to the input and output capacitors, and to the LDO ground pin as close to each other as possible with a wide and component-side copper surface. The use of vias and long traces to create LDO circuit connections is strongly discouraged and negatively affects system performance. This grounding and layout scheme minimizes the inductive parasitic, and thereby reduces load-current transients, minimizes noise, and increases circuit stability. A ground reference plane is also recommended and is either embedded in the PCB itself or located on the bottom side of the PCB, opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread heat from the LDO device

Packaging Information

DFN3x3-8

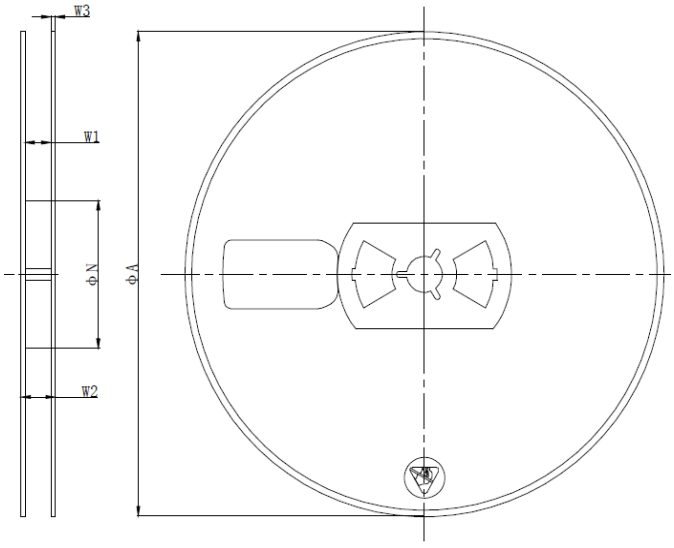


SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.25	0.28	0.35
c	0.19	0.20	0.23
D	2.90	3.00	3.10
D1	2.10	2.30	2.70
e	0.65 BSC		
E	2.90	3.00	3.10
E1	1.30	1.50	1.90
L	0.25	0.30	0.45
h	0.20	0.25	0.30

Tape and Reel Information

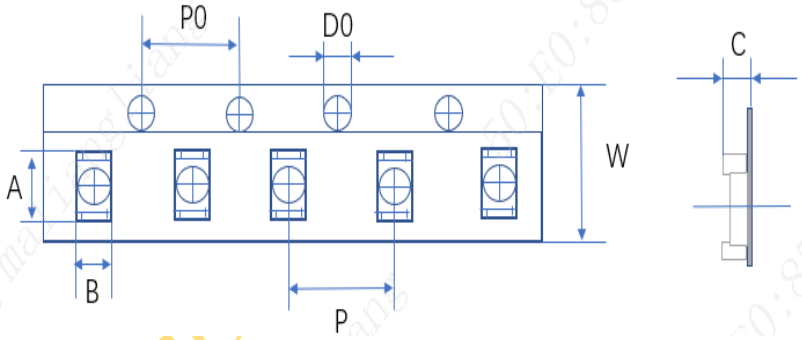
DFN3x3-8

REEL DIMENSIONS



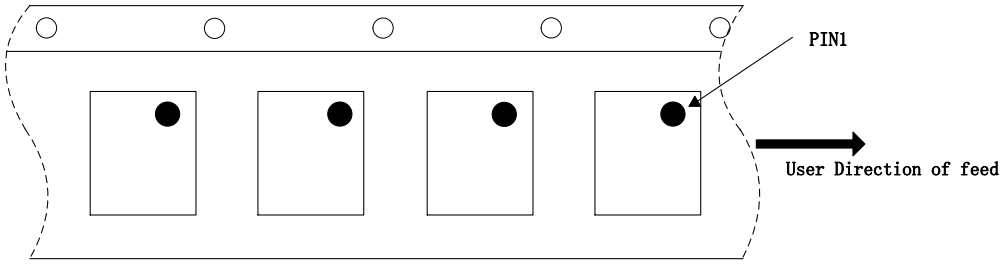
SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
ΦA	327.00	329.00	331.00
W2	14.40	16.40	18.40

TAPE DIMENSIONS



SYMBOL	Dimensions In Millimeters		
	MIN	NOM	MAX
A	3.10	3.40	3.70
B	3.10	3.40	3.70
P0	3.90	4.00	4.10
P	7.90	8.00	8.10
D0	1.45	1.55	1.65
W	12.70	12.00	12.30
C	0.95	1.10	1.25

PIN1 AND TAPE FEEDING DIRECTION



Classification of IR Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat/Soak		
Temperature Min(T_{SMIN})	100℃	150℃
Temperature Max(T_{SMAX})	150℃	200℃
Time(T_S) from (T_{SMIN} to T_{SMAX})	60~120 seconds	60~120 seconds
Ramp-up rate (T_L to T_P)	3℃/second max	3℃/second max
Liquidous temperature(T_L)	183℃	217℃
Time(t_L) maintained above T_L	60~150 seconds	60~150 seconds
Peak package body temperature (T_P)	For users T_P must not exceed the Classification temp in Table 1. For suppliers T_P must equal or exceed the Classification temp in Table 1.	For users T_P must not exceed the Classification temp in Table 2. For suppliers T_P must equal or exceed the Classification temp in Table 2.
Time(t_P)* within 5℃ of the specified classification temperature(T_C), see Figure1	20* seconds	30* seconds
Ramp-down rate (T_P to T_L)	6℃/second max	6℃/second max
Time 25℃ to peak temperature	6 minutes max	8minutes max
* Tolerance for peak profile temperature (T_P) is defined as a supplier minimum and a user maximum.		

Table 1Sn-Pb Eutectic Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ ≥350
<2.5mm	235℃	220℃
≥2.5mm	220℃	220℃

Table 2 Pb-Free Process - Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350~2000	Volume mm³ ≥350
<1.6mm	260℃	260℃	260℃
1.6mm~2.5mm	260℃	250℃	245℃
>2.5mm	250℃	245℃	245℃

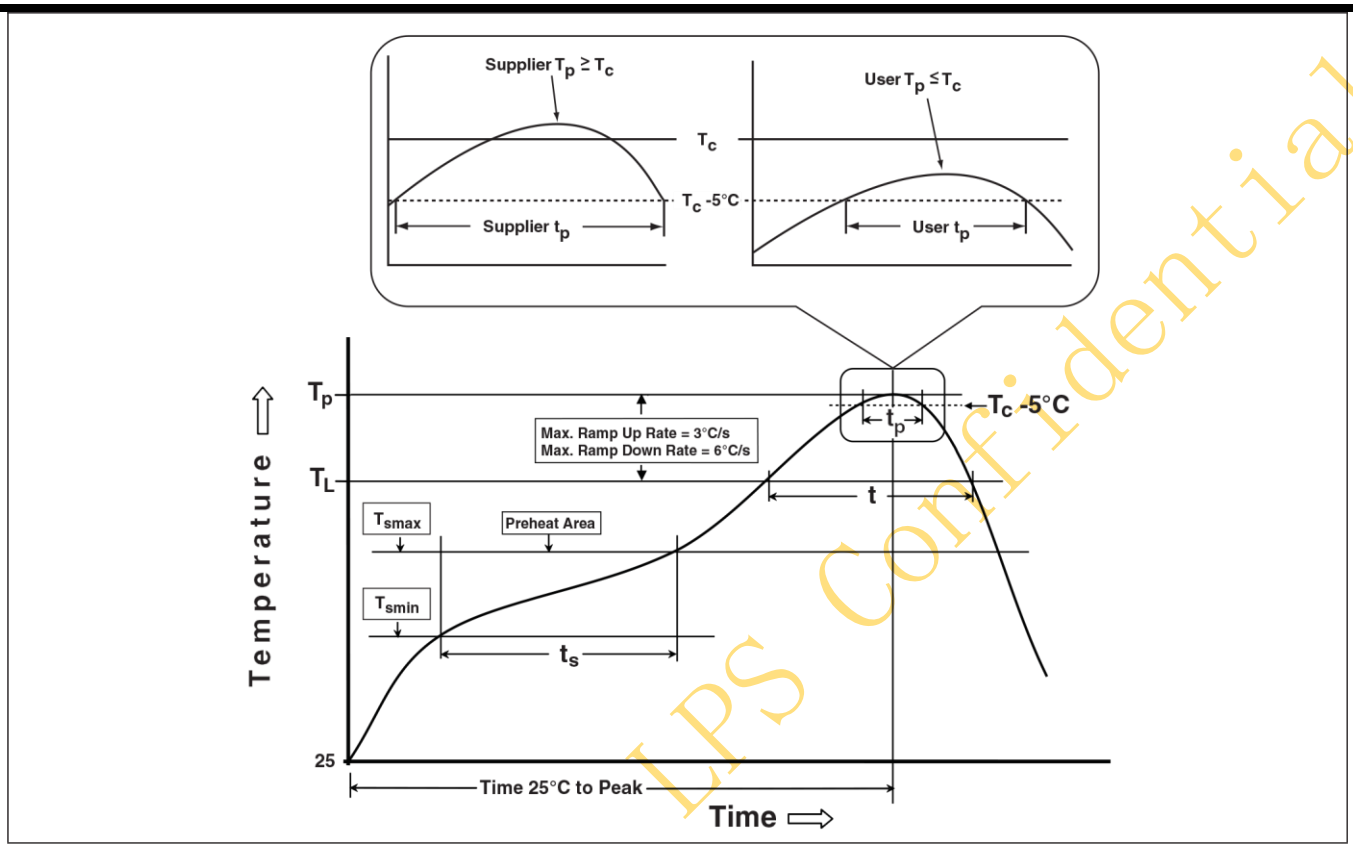


Figure1Classification Profile (Not to scale)

Products conform to "JEDEC J-STD-020C" standards;

Products shipped conform to "Rohs" standards;

Moisture Sensitivity Level：MSL3（CONDITION：≦30 °C/60%RH、Time control:168 hours）;

Revision History

Revision	Date	Change Description
V0.1	5/14/2026	First release version

Important Notice and Disclaimer

LPS PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with LPS products. You are solely responsible for (1) selecting the appropriate LPS products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. LPS grants you permission to use these resources only for development of an application that uses the LPS products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other LPS intellectual property right or to any third party intellectual property right. LPS disclaims responsibility for, and you will fully indemnify LPS and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources. LPS’s provision of these resources does not expand or otherwise alter LPS’s applicable warranties or warranty disclaimers for LPS products.

LPS objects to and rejects any additional or different terms you may have proposed.

微源半导体股份有限公司（以下简称为微源半导体）按“原样”提供技术和可靠性数据(包括数据表)、设计资源(包括参考设计)、应用程序或其他设计建议、网络工具、安全信息和其他资源，并不承担所有明示和默示的保证，包括但不限于任何关于适销性、适合特定目的或不侵犯第三方知识产权的默示保证。

这些资源适用于使用微源半导体产品进行设计的熟练开发人员。您全权负责(1)为您的应用选择合适的微源半导体产品，(2)设计、验证和测试您的应用，以及(3)确保您的应用符合适用的标准，以及任何其他安全、保安、法规或其他要求。这些资源如有更改，恕不另行通知。微源半导体允许您仅将这些资源用于开发使用资源中描述的微源产品的应用程序。禁止以其他方式复制和展示这些资源。不授予任何其他微源半导体知识产权或任何第三方知识产权许可。对于因您使用这些资源而产生的任何索赔、损害、成本、损失和责任，微源半导体不承担任何责任，您将完全赔偿微源半导体及其代表。微源半导体对这些资源的提供不会扩大或以其他方式改变对微源产品的适用保证或保证免责声明。

微源半导体反对并拒绝您可能提出的任何附加或不同条款。