



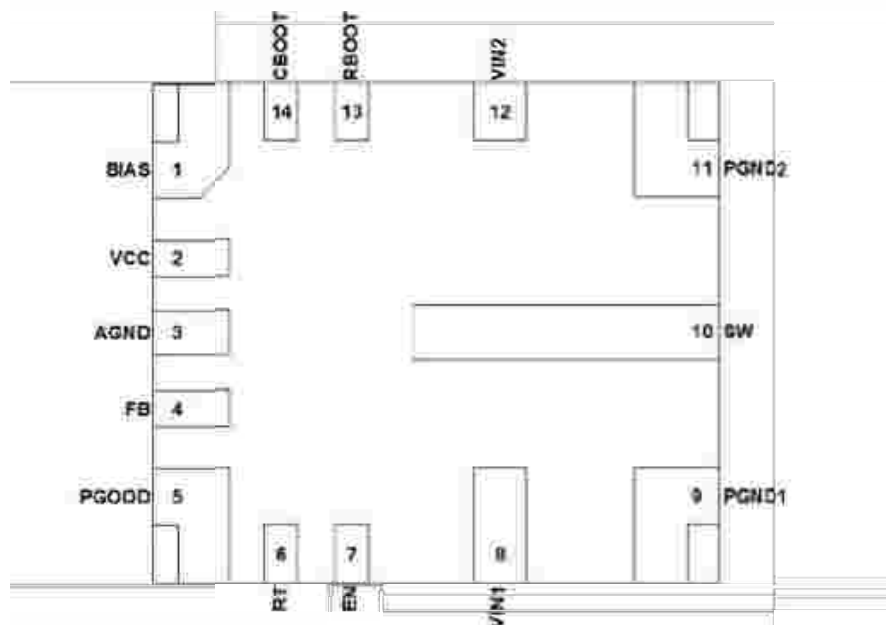


Device Information

Part Number	Top Marking	Output Current	Mode	Spread Spectrum	Output Voltage	MSL
LPQ64460QVF	LPS LPQ64460 YWX	6A	Auto-PFM	OFF	Adjustable	LEVEL-3
LPQ64460QVF-33	LPS LPQ64460 33YWX	6A	Auto-PFM	OFF	3.3V fixed	LEVEL-3
LPQ64460QVF-50	LPS LPQ64460 50YWX	6A	Auto-PFM	OFF	5.0V fixed	LEVEL-3
LPQ64460FQVF	LPS LPQ64460 FYWX	6A	FPWM	OFF	Adjustable	LEVEL-3
LPQ64460SQVF	LPS LPQ64460 SYWX	6A	Auto-PFM	ON	Adjustable	LEVEL-3
Marking indication: Y: Year code. W: Week code. X: Batch numbers. MSL: Moisture sensitivity level according to JEDEC standards.						



Pin Diagram



LPQ64460Pinout (3.5mm*4mm-QFN)

Pin Description

Pin #	Name	I/O	Description
1	Bias	Power	LDO input. If an input voltage at this pin is higher than 3.4V, this pin becomes the input of the internal LDO. Connect this pin to Buck output may improve efficiency. Connect this pin to AGND or floating if not used.
2	VCC	Power	LDO output pin. This pin is also the power supply of internal control circuits. Connect to a 1uF capacitor from this pin to AGND.
3	AGND	GND	Analog ground for internal circuitry. Feedback and VCC are measured with respect to this pin. Must connect AGND to both PGND1 and PGND2 on PCB.
4	FB	I/O	Output voltage feedback input to the internal control loop. Connect to feedback divider tap point for adjustable output voltage. Do not float or connect to ground. For a fixed output version, please connect FB to the output capacitor directly.
5	PGOOD	I/O	Power good indication. This pin is open-drain output.
6	RT	I/O	Switching frequency programming pin. Connect a resistor from this pin to AGND to set a fixed switching frequency.
7	EN	I/O	Enable input, active high. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. This pin can be used to control the system power sequence as well.
8	VIN1	Power	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND1. Low impedance connection must be provided to VIN2.
9	PGND1	GND	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND2.



			Connect a high-quality bypass capacitor or capacitors from this pin to VIN1.
10	SW	Power	Switching node
11	PGND2	GND	Power ground to internal low-side MOSFET. Connect to system ground. Low impedance connection must be provided to PGND1. Connect a high-quality bypass capacitor or capacitors from this pin to VIN2.
12	VIN2	Power	Input supply to the converter. Connect a high-quality bypass capacitor or capacitors from this pin to PGND2. Low impedance connection must be provided to VIN1.
13	RBOOT	I/O	Connect to CBOOT through a resistor. This resistance must be between 0 Ω and open and determines SW node rise time.
14	CBOOT	Power	High-side driver upper supply rail. Connect a 100-nF capacitor between SW pin and CBOOT. An internal diode connects to VCC and allows CBOOT to charge while SW node is low.



Absolute Maximum Ratings (Note1)

VIN1, VIN2, SW to AGND, PGND1, PGND2	-0.3V to 46V
EN, BIAS to AGND, PGND1, PGND2	-0.3V to 46V
AGND to PGND1, PGND2	-1V to 1V
Other pins to AGND, PGND1, PGND2	-0.3V to 5.5V
RBOOT, CBOOT to SW	-0.3V to 5.5V
SW to GND (20ns transient)	-2V to 46V
Operating Ambient Temperature Range (T _A)	-40°C to 125°C
Operating Junction Temperature Range (T _J)	-40°C to 150°C
Maximum Soldering Temperature (at leads, 10 sec)	260°C

Note 1: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD Ratings

HBM (Human Body Model)	2kV
CDM (Charged-device Model)	500V

Thermal Information

θ_{JA} (Junction-to-Ambient Thermal Resistance, JESD51-7)	60°C/W
θ_{JC} (Junction-to-Case Thermal Resistance, JESD51-7)	19.2°C/W
θ_{JA} (Junction-to-Ambient Thermal Resistance, EVM, 2oz, 4-layer)	25°C/W

Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VIN	Input voltage	4		42	V
VOUT	Output voltage	1		24	V
T _A	Ambient temperature range	-40		125	°C
T _J	Junction temperature range	-40		150	°C
C _{IN}	Input decoupling capacitor ^[1]	4.7		100	μF
C _{OUT}	Output capacitor ^[1]	10		100	μF

[1] Effective capacitance



Electrical Characteristics

(The specifications are measured under conditions $V_{IN} = 13.5V$, $T_J = -40^{\circ}C$ to $125^{\circ}C$, unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SECTION						
V_{ULVO_VIN}	Input under voltage lockout threshold	V_{IN} rising threshold	3		3.8	V
I_{q_VIN}	Input quiescent current at V_{IN} pin	No switching, $V_{EN}=3V$, $V_{FB}=2V$, $V_{BIAS}=5V$		0.6		μA
		Auto-PFM, 2.2MHz, Switching, $V_{EN}=3V$, BIAS pin is connected to the output capacitor [Note2]		10		μA
		Auto-PFM, 2.2MHz, Non-Switching, $V_{EN}=3V$, BIAS pin is connected to ground, $FB=120\%V_{ref}$		25	35	μA
I_{q_SD}	Input shutdown current	$V_{EN}=0$		0.6		μA
VCC Regulator						
V_{CC}	LDO output voltage	50mA load	-5%	5	+5%	V
I_{VCC}	VCC current limit		100	150		mA
V_{UVLO_VCC}	LDO under-voltage threshold	VCC rising edge		3.6		V
$V_{UVLO_VCC_H}$	LDO under-voltage hysteresis			1		V
R_{VCC_DOWN}	VCC pull down resistor	EN=0		100		Ω
BUCK CONVERTER						
$R_{DS(on)_HS}$	High-side MOSFET on-resistance	$V_{IN}=12V$		40	80	m Ω
$R_{DS(on)_LS}$	Low-side FET on resistance	$V_{IN}=12V$		20	40	m Ω
I_{LIM_PEAK}	High-side peak current limit		9	10	11.5	A
I_{LIM_VALLEY}	Low-side valley current limit		6.5	7	8.5	A
I_{NOCL}	Negative current limit	FPWM mode		-3		A
I_{PK_MIN1}	Minimum peak current at minimum duty cycle	Minimum on-time(~50ns)		1.2		A



SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PK_MIN2}	Minimum peak current at maximum duty cycle	Maximum on-time(~9us)		0.8		A
V_{ref}	FB reference voltage	$T_J = -40^{\circ}C \sim -125^{\circ}C$	-1%	1	+1%	V
V_{OUT}	5V fixed output voltage	$T_J = -40^{\circ}C \sim -125^{\circ}C$, 5V fixed output version	-1%	5	+1%	V
I_{leak_FB}	FB pin leakage current			0.1		μA
Switching Frequency						
F_{sw}	Switching frequency	Programming switching frequency range	0.2		2.2	MHz
		2.2MHz frequency	1990	2200	2410	kHz
		400kHz frequency	360	400	440	kHz
t_{on-min}	Minimum on-time [Note 2]	2.2MHz, $V_{OUT}=1V$, $V_{IN}=24V$		50		ns
t_{on-max}	Maximum on-time			9		μs
$t_{off-min}$	Minimum off-time [Note 2]	$V_{FB}=V_{ref} - 0.2V$		100		ns
V_{HICCUP}	Hiccup threshold on FB pin	Reference to V_{ref} or Fixed output		50		%
$t_{on-hiccup}$	Hiccup on time [Note 2]	Not include the soft-time		1		ms
$t_{off-hiccup}$	Hiccup waiting time [Note 2]			80		ms
EN Logic and Soft-start						
V_H	EN pin logic high threshold	EN Rising threshold	1.15	1.26	1.35	V
V_{hys}	EN pin threshold hysteresis			0.3		V
V_{EN_WAKE}	EN control circuit wake up threshold	EN Rising threshold	0.4			V
I_{EN_leak}	EN pin leakage current	$V_{EN}=12V$			1	μA
t_b	EN pin blanking time [Note 2]	EN pin rising or falling edge blanking time	4		28	μs
t_d	EN delay time [Note 2]	From EN high to first switching		500		μs



SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{SS}	Soft start time [Note 2]	From first switch to 90%*V _{ref}		5		ms
PGOOD (Power Good)						
V _{OVP_rise}	Power threshold GoodOVP	VOUT rising edge, reference to Vref	105	107	110	%
V _{OVP_fall}	Power hysteresis GoodOVP	VOUT falling edge, reference to Vref		105		%
V _{UVLO_rise}	Power threshold GoodUVLO	VOUT rising edge, reference to Vref	93	95	97	%
V _{UVLO_fall}	Power Good UVLO hysteresis	VOUT falling edge, reference to Vref	91	93	95	%
t _{PGD_deglitch}	Power Good deglitch time	PGD deglitch time, 0 to 1 or 1to 0		10		us
t _{PGD_deglitch}	PGD output delay time	From OVP/UVLO is recognized after deglitch time to PGD pin change		1		ms
R _{PGD}	PGD pull down resistance	VIN=12V		50		Ω
Thermal Protection						
T _{jsd}	Thermal shutdown threshold	Rising threshold	158	168	180	°C
	Thermal shutdown threshold	Falling threshold		158		°C

[Note 2]: Not production tested, but guaranteed by design.



Typical Characteristics

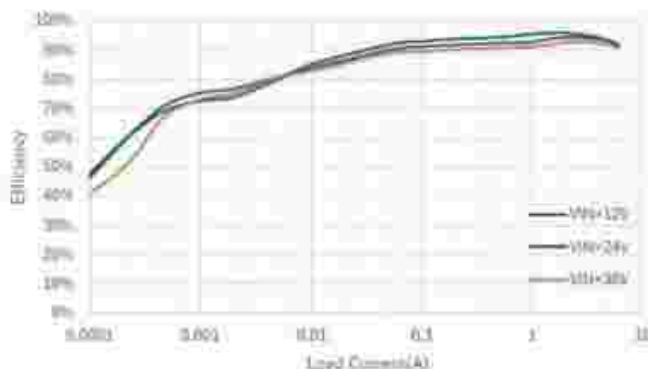


Figure 1. Efficiency vs. Output Current
(fsw=400kHz, Vout=5.0V fixed)

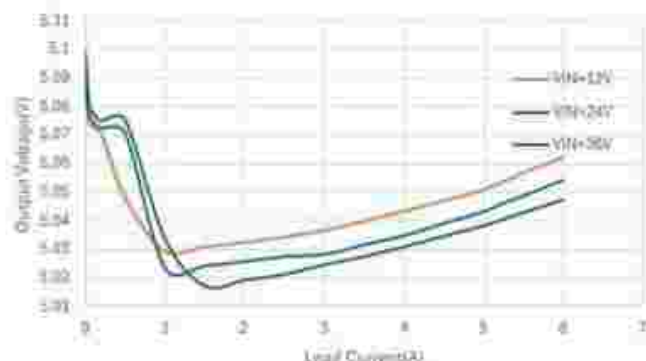


Figure 2. Output Voltage vs. Output Current
(fsw=400kHz, Vout=5.0V fixed)

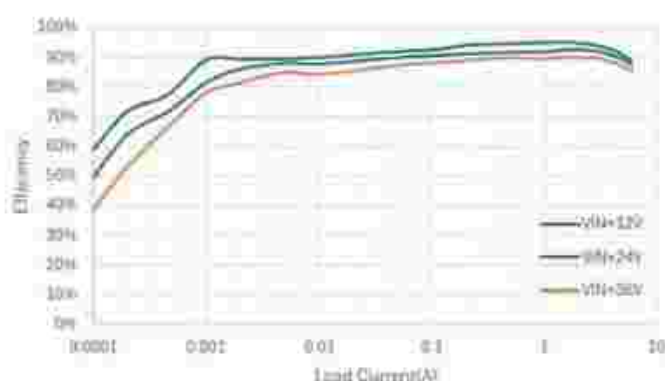


Figure 3. Efficiency vs. Output Current
(fsw=400kHz, Vout=3.3V fixed)

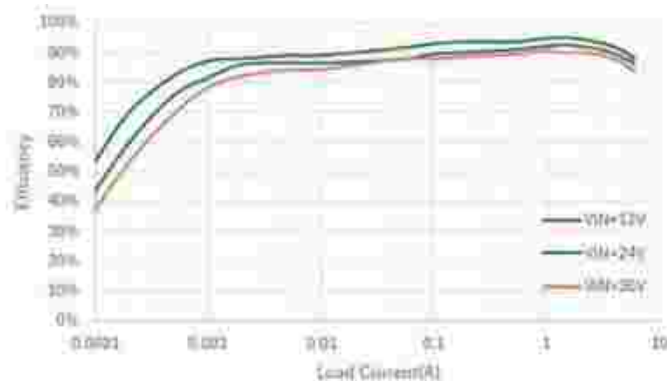


Figure 4. Efficiency vs. Output Current
(fsw=400kHz, Vout=3.3V, RFB=100kΩ and 43.4kΩ)

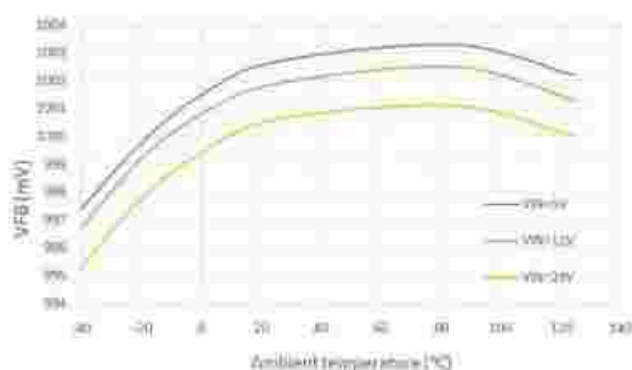


Figure 5. VFB Voltage vs. Ambient Temperature

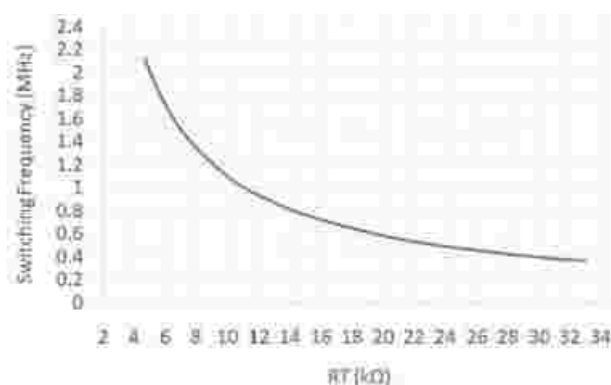


Figure 6. Switching Frequency vs. RT Resistance



Application Waveforms (VIN=13.5V, VOUT=3.3V, L=4.7uH, Fsw=400kHz)



Figure 7. Startup by EN, 50mA load



Figure 8. Shutdown by EN, 50Ω load



Figure 9. Startup by EN, 6A load



Figure 10. Shutdown by EN, 6A load



Figure 11. Startup by VIN, 50mA load



Figure 12. Shutdown by VIN, 50mA load



Figure 13. Startup by VIN, 6A load



Figure 14. Shutdown by VIN, 6A load

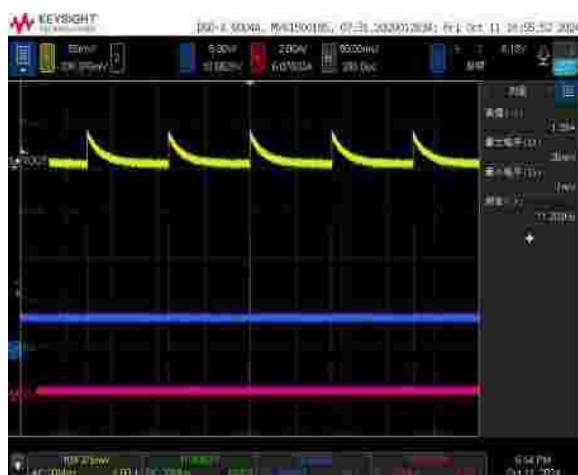


Figure 15. Switching Waveform, 0A load

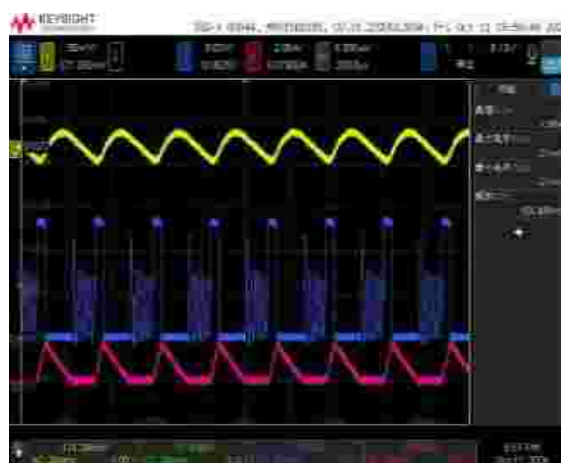


Figure 16. Switching Waveform, 0.5A load



Figure 17. Switching Waveform, 3A load



Figure 18. Switching Waveform, 6A load

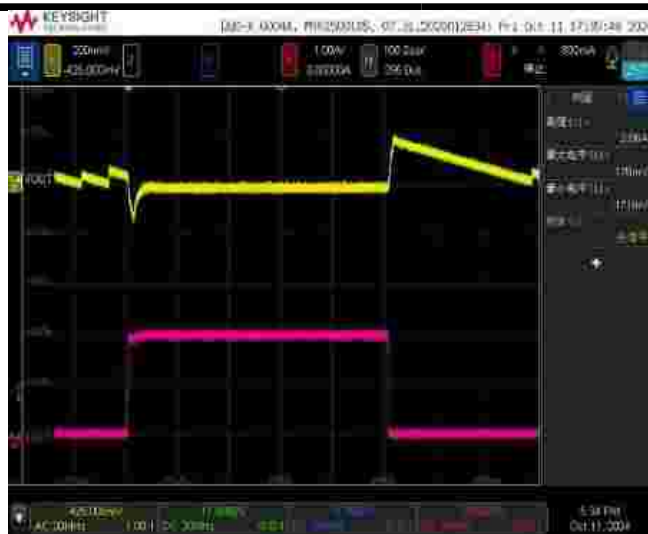


Figure 19. Load Transient, 0.05A-2A-0.05A



Figure 20. Load Transient, 0.05A-6A-0.05A



Figure 21. SCP Happen, Hiccup Operation



Figure 22. SCP Recovery

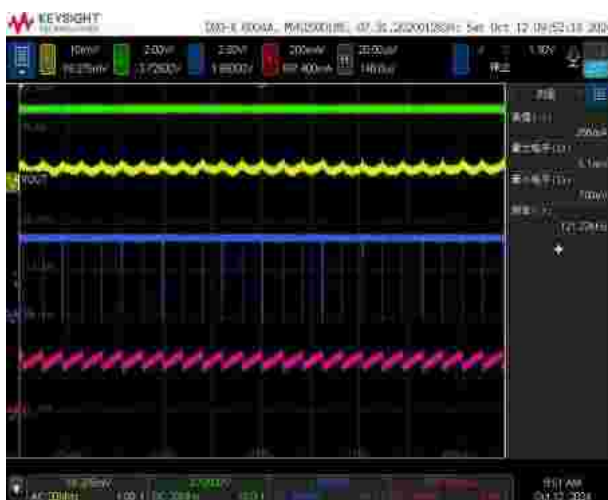


Figure 23. Dropout Mode, VIN=3.3V, 200mA

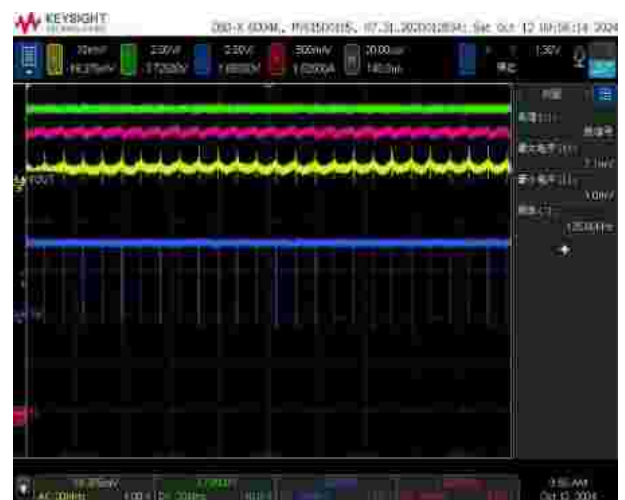
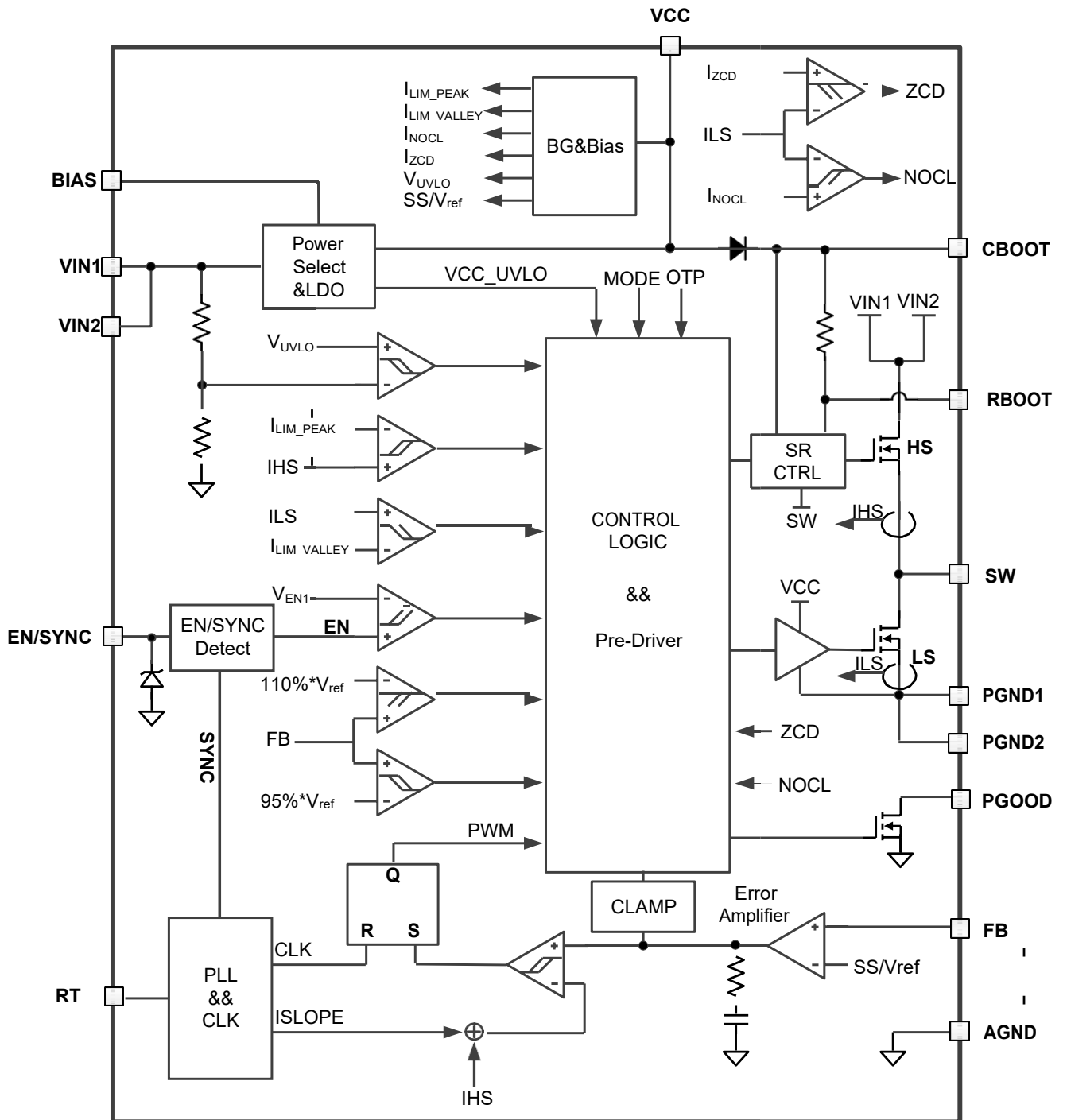


Figure 24. Dropout Mode, VIN=3.3V, 3A



Detailed Description





Overview

The LPQ64460 is an ultra-low quiescent current synchronous buck converter supporting up to 6A output current by integrating the high-side MOSFET and the low-side MOSFET. LPQ64460 features a BIAS pin to provide the power for the internal circuits and the input current is less than 10- μ A by connect the BIAS pin to the output capacitor when the LPQ64460 is enabled. The LPQ64460 employs peak current mode control with the switching frequency programmable from 200 kHz to 2.2 MHz. The device works in fixed frequency PWM operation in medium to heavy loads while enters PFM operation when the load goes light. The LPQ64460 supports the spread spectrum function of the internal clock to improve EMI at FPWM mode. This feature varies the clock with a modulation of $\pm 5\%$. In addition, there is an internal soft-start time to limit the inrush current. The PGD pin indicates whether the output voltage is ready for the MCU to control the system power sequence. The switching slew rate of the HS-MOSFET is programmable by connecting a resistor between the RBOOT and CBOOT pins to optimize the EMI performance.

The LPQ64460 has various fixed output voltage version to save the external feedback resistor.

The LPQ64460 supports both aluminum polymer capacitors and ceramic capacitors without extra compensation components.

The LPQ64460 also integrates multiple protection functions, i.e., over-current protection (OCP), over-temperature protection (OTP), under-voltage lockout (UVLO), and short circuit protection (SCP).

Peak Current Mode Control Scheme

The LPQ64460 integrates the peak current mode control scheme when operating in continuous conduction mode (CCM). Refer to the Functional Block Diagram for better understanding of the operation. The internal oscillator block turns on the high-side MOSFET to start a switching cycle each cycle. The FB-pin voltage is amplified by the internal error amplifier with a typical 1-V reference voltage. Once the peak current of the inductor reaches the output voltage of the error amplifier that is the COMP voltage, the LPQ64460 turns off the high-side MOSFET and turns on the low-side MOSFET after a dead time. The high-side MOSFET is turned on for at least ~ 50 -ns, even if the peak current is above the COMP voltage, which is the minimum-on time. One the low-side MOSFET is ON, it remains on for at least ~ 100 ns before the next cycle starts, that is the minimum off-time.

If the current in the high-side MOSFET does not reach the value set by the COMP voltage, the high-side MOSFET is forced off when the on time lasts about 9- μ s, even if the COMP value is not reached.

Auto-PFM

The LPQ64460 is designed to maintain high efficiency at light load by adopting automatic pulse-frequency modulation (Auto-PFM). When the converter operates in light load condition, the output of the internal error amplifier decreases to make the inductor peak current down, delivering less power to the load. When the output current further decreases, the current through the inductor decrease to zero during the off-time. When the inductor current reaches zero, detected by the zero-current detection (ZCD) comparator, the low-side MOSFET is turned off, together with the high-side MOSFET. Both MOSFETs remains off until a new switching cycle begins, determined by the PFM control loop. As the load current decreases, the duration for both MOSFETs to remain off increases, leading to a lower switching frequency and higher power efficiency.

The LPQ64460 exits the PFM mode automatically and enter CCM when the load increases to the level when the minimum inductor current increases to higher than zero.

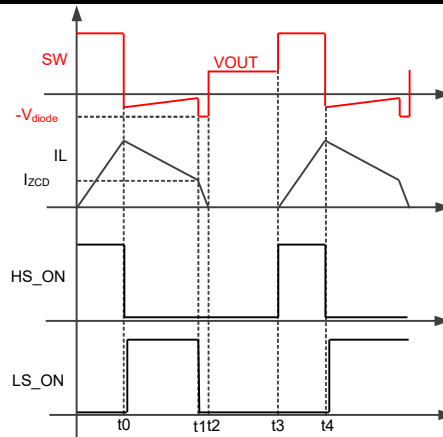


Figure 25. Auto-PFM at light load

Under Voltage Lockout (VIN UVLO)

When the input voltage VIN is lower than the V_{UVLO_IN} threshold, after a typical 100- μ s deglitch time, all functions are shut down, the current into VIN pin is less than 1 μ A. When the input voltage is higher than the V_{UVLO_IN} rising threshold, the LPQ64460 can be enabled by the EN pin.

LDO Output

The VCC output is a linear regulator output that is powered by the VIN or the BIAS pin. When the BIAS pin is less than 3V (short to ground or float), the LDO is powered by the VIN1 and VIN2 pins directly, otherwise, the LDO is powered by BIAS pin. The VCC used is to power the internal circuits, including the power MOSFETs' driver. A 0.1~0.47- μ F external ceramic capacitor is required. The LDO output voltage is fixed 5.0V. The LDO has a typical 2.5V under-voltage protection threshold, the VCC is disabled when both the VIN and BIAS pins are lower than 2.5V. The LDO recovers when either one recovers to 3.6V or higher.

When both VIN and BIAS are below the VCC regulation voltage, the output voltage of VCC degrades. Typically, the BIAS pin can be connected to the output capacitor to provide the lowest possible input supply current. Don't connect external loads to the VCC pin.

Bootstrap Capacitor

The LPQ64460 integrates two N-MOSFET to achieve high efficiency. The high-side MOSFET is powered by the bootstrap capacitor, which is between the C_{BOOT} pin and SW pin. The high-side MOSFET slew rate is programmable by connect a resistor with value of 0~200 Ω between the R_{BOOT} and C_{BOOT} pins. The C_{BOOT} capacitor should provide sufficient voltage headroom to facilitate the charging. When the high-side MOSFET is on, C_{BOOT} is above VCC and the bootstrap capacitor cannot be charged.

Under high-duty cycle operation, the bootstrap has less time to charge, so the bootstrap capacitor may not be charged sufficiently. One way is to use large capacitors with 1- μ F capacitance.

When R_{BOOT} is short with C_{BOOT} , the slew rate is at the highest level, the rise time of the SW node is approximately at 3ns.



Frequency Foldback

Minimum ON-Time

The LPQ64460 automatically reduces the switching frequency when the minimum on-time limit is reached, which is 50-ns typically under low duty cycle applications. The converter can regulate the lowest programmable output voltage at the maximum input voltage. The LPQ64460 works as a constant-on time (COT) with valley current control mechanism when minimum on-time is triggered.

Minimum OFF-Time

The LPQ64460 is designed to operate at close to 100% duty cycle and automatically reduces the switching frequency to increase the effective duty cycle and maintain regulation when VIN is close to VOUT. Under this condition, the LPQ64460 extends on-time past the end of the clock cycle until the required peak current is achieved. The clock can only start a new cycle once peak inductor current is achieved or once a pre-determined maximum on-time, which is ~9us typically. If the input voltage is low enough that the output voltage cannot be regulated even with the maximum on-time, output voltage drops to slightly below the input voltage.

EN Control and Soft Start

The EN pin is used to control the system power-up sequence. A precise voltage reference is used as the threshold. When the VIN is above the UVLO threshold and EN voltage rises above the EN pin logic high threshold (1.26V typically), after an EN blanking time t_b (see the value in EC table) time, then the LPQ64460 enables all the internal circuits, delays for t_d time (see the value in EC table), and begins the soft-start.

The LPQ64460 integrates soft-start function with a typical time oft_{ss} (see the value in EC table) . After passing the UVLO threshold and enabled by the EN pin, the internal reference voltage ramps from zero to the 90%*Vref in t_{ss} and the output voltage ramps up accordingly. In this way, the inrush current is limited when big output capacitors are used.

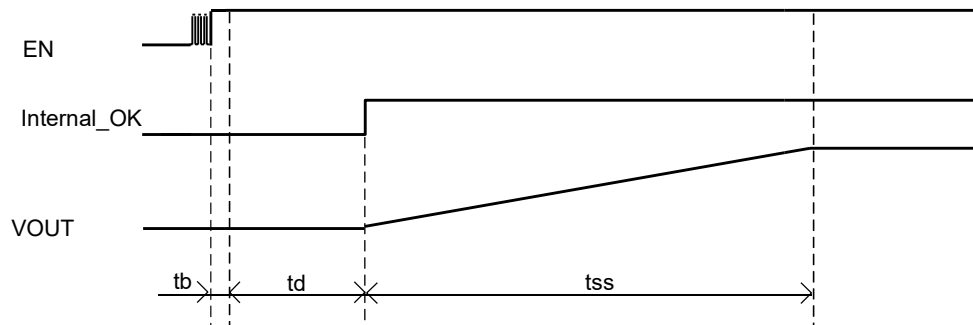


Figure 26. Soft Start Sequence

The LPQ64460 works in Auto-PFM mode no matter FPWM mode or an external clock is applied at the EN pin. This prevents from pulling the output low during soft-start if there is already a certain level voltage at the output. If the V_{FB} is higher than the Vref/SS signal internally, the LPQ64460 will not switch until the Vref/SS is higher than the V_{FB} . This prevents discharging the output to the ground.

The VCC is discharged by a 100Ω resistance when EN is pulled to logic low after deglitching time.

Switching Frequency Setting

The LPQ64460 uses a fixed-frequency control scheme. The switching frequency can be programmed between 200 kHz and 2.1 MHz using a resistor from the RT pin to GND. The resistance can be estimated by the equation below:

$$R_{RT} = 13460 * (1/F_{sw}(\text{kHz}) - 7.1 * 10^{-5})$$

Where R_{RT} is the resistance between the RT pin and the GND pin and the F_{sw} is the switching frequency. A typical



frequency vs. RT resistance can be looked up from Figure 6 as well. The LPQ64460 supports duty cycle higher than 95%. This happens when the VIN voltage drops while the VOUT is set to be close to VIN voltage. The switching frequency is reduced smoothly and the output voltage keeps in regulation until the maximum on-time is triggered. If the VIN voltage drops further, the VOUT voltage drops.

The LPQ64460 reduces the switching frequency as well when the minimum on-time is triggered.

Spread Spectrum Frequency Modulation

The LPQ64460 uses a pseudo random mechanism to spread the switching frequency with $\pm 5\%$ of normal frequency. The pattern frequency of the pseudo random sequence generator is 1.5Hz to avoid the audio band of 20~20kHz. For example, if the normal switching frequency of the LPQ64460 is programmed to 2.2MHz, the spread spectrum function modulates the switching frequency in the range of 2.09 MHz to 2.31 MHz in 1.5-Hz rate.

The spread spectrum is available while the clock of the LPQ64460 is free running at its natural frequency which is set by the resistor at RT pin. Any of the following conditions overrides spread spectrum, turning it off:

- 1) An external clock is applied to the EN pin.
- 2) The device works in PFM operation at light load.
- 3) The frequency is lower than the target value because of the minimum off-time or the minimum on-time is triggered.

Over Current Protection and Short Circuit Protection

The LPQ64460 protects an over current situation by limiting the COMP voltage, the inductor peak current and the inductor valley current cycle by cycle. The current of high-side MOSFET is monitored all the time to sense the inductor peak current when the high-side MOSFET is turned on. The high-side MOSFET is turned off if the peak current is higher than the COMP high clamp threshold, protecting the inductor current from further increasing. The low-side MOSFET is monitored all the time as well to sense the inductor valley current when the low-side MOSFET is turned on. The high-side MOSFET is not allowed to be turned on until the inductor current drops below the valley current limit threshold.

The SCP is realized by monitoring the FB-pin voltage when the inductor current is limited. Once the output load draws more current than the current limit, the output voltage drops. When the FB voltage drops to 50% of the Vref for 128 consecutive cycles, the LPQ64460 shuts down. The LPQ64460 will restart after a typical 80-ms hiccup waiting time. If the SCP condition still holds after soft-start, the LPQ64460 shuts down again, repeating the hiccup operation.

When the over current condition is removed, the output voltage returns to normal operation.

Power Good Indication

The PGOOD pin of LPQ64460 is an open-drain output, this pin is left floating when the FB in the range of 94%~110%Vref. An internal 50-Ω on-resistance NMOS FET is active to pull PGOOD pin to the ground when the FB is beyond the range after a typical deglitch time (see in EC table). The on-resistance increases when the VIN voltage is lower than 2V.



Table 1. PGD Logic Table

State	Description	PGOOD pin
EN=Low	$V_{IN} \geq V_{TH}$	LOW
EN=High	$V_{IN} \geq UVLO \& \& FB \ 94\% \sim 110\% V_{ref}$	OPEN
EN=High	$V_{IN} \geq UVLO \& \& (FB < 94\% V_{REF} \ FB > 110\% V_{ref})$	LOW
Thermal Shutdown	$V_{IN} \geq V_{TH}$	LOW

Thermal Protection

The LPQ64460 has a thermal protection function. The device will shut down when the internal temperature is higher than 168°C and will restart after the temperature drops below 158°C.

Application Information

Design Requirements

The table 1 shows the design parameters for a typical 3.3V output voltage.

Table 2 Design Parameters

Parameter	Target
Input voltage range	13.5V typical, range: 6~42V
Output voltage	3.3V
Load current	0~6A
Transient response ripple	$\pm 200mV$
Operating frequency	400kHz

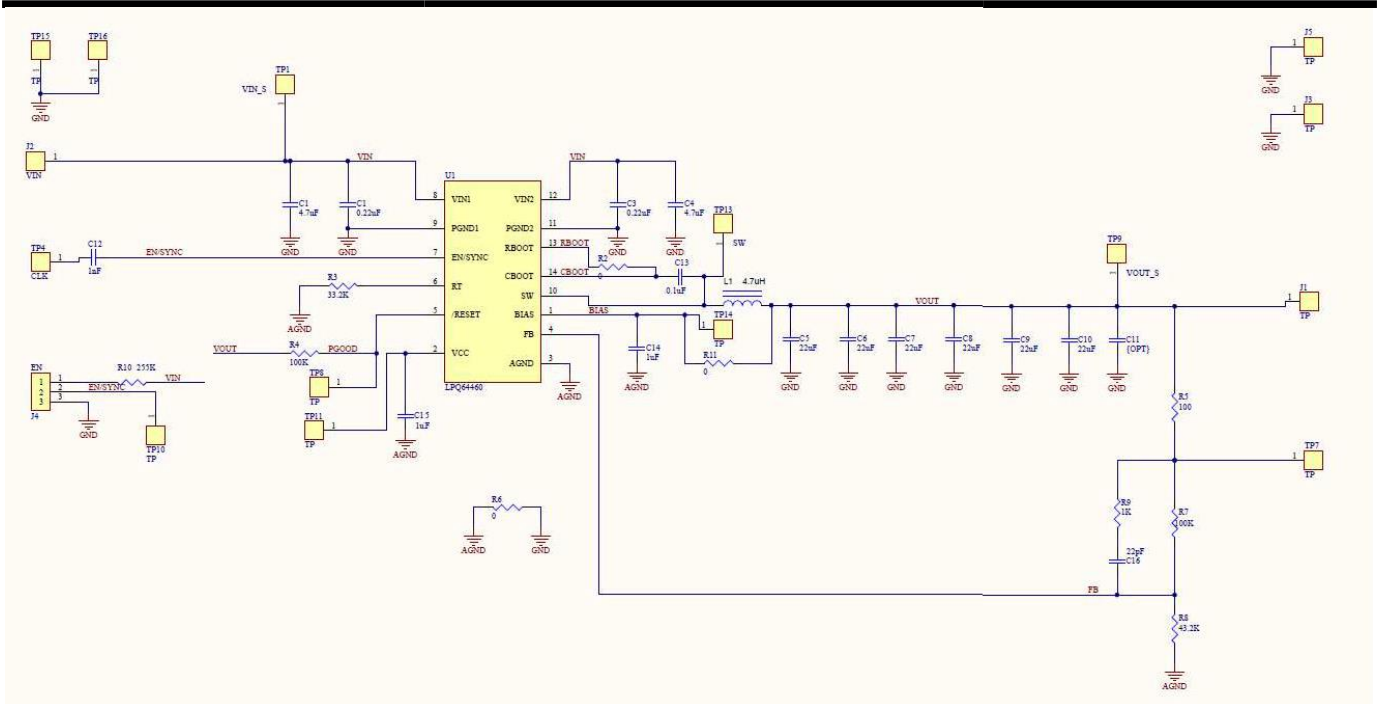


Figure 27. Typical schematic

Output Voltage Setting

The output voltage can be programmed by adjusting the external resistor divider R_{UP} and R_{DOWN} according to the equation below:

$$V_{OUT} = \left(\frac{R_{UP}}{R_{DOWN}} + 1 \right) * V_{REF}$$

When the output voltage is in regulation, the typical voltage at FB pin is 1V.

For better accuracy, the R_{DOWN} is recommended to be lower than 500kΩ to ensure the current flowing through R_{DOWN} is at least 100 times larger than the FB pin leakage current.

For a 3.3V-output application, a 43.2kΩ R_{DOWN} is selected and the R_{UP} is 100kΩ to save quiescent current.

Switching Frequency

The LPQ64460 allows the user to design the switching frequency by connecting a resistor between RT and GND pins. To avoid the AM frequency band, the switching frequency is recommended to be set lower than 525kHz and higher than 1.61MHz. The higher frequency helps reduce the inductor and capacitors' size but lower efficiency. The lower frequency helps improve the switching frequency but larger inductor and capacitors' size.

In this case, 400kHz is selected as the typical frequency to leave enough margin below the AM band.

According to the equation, the resistor of R_2 is 33.2kΩ.

EN Design

The LPQ64460 allows the user to design a precise VIN voltage to enable the converter during power on. The startup sequence can be designed by adjusting the resistor divider of R_{UP_EN} and R_{DOWN_EN} with the equation below,

$$V_{EN} = \frac{R_{DOWN_EN}}{R_{UP_EN} + R_{DOWN_EN}} * V_{IN}$$

where V_{EN} is the EN rising threshold voltage at which the converter is enabled, which is 1.26V typically. A 47pF-1nF capacitor is recommended to be soldered in parallel with the R_{EN_DOWN} to avoid the high-frequency noise influence from the switching node.

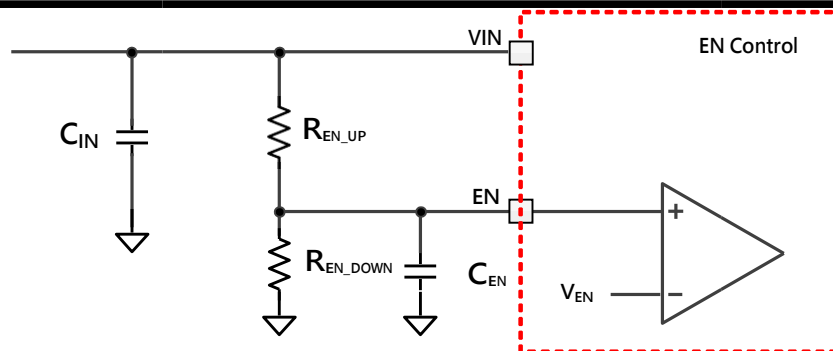


Figure 28. EN connection

Inductor and Output Capacitor Setting

The inductor ripple is calculated by the equation below:

$$I_{PP} = \left(\frac{V_{OUT}}{L * F_{SW}} * \frac{V_{IN} - V_{OUT}}{V_{IN}} \right)$$

To get a better efficiency, the inductor ripple is recommended to be controlled under 40% of the output current to minimize the AC loss of the inductor and power MOSFETs.

For a typical 13.5V input voltage and 3.3V output voltage, a low DCR value, 4.7-μH inductor is recommended with switching frequency of 400kHz.

The output capacitor not only impacts the output ripple but also the loop stability. Please follow the design rules in the table below. A feedforward capacitor C_{FF} can be selected to improve the transient behavior. The typical capacitance can be 10-100pF. For this design, 10V, X5R, 22μF capacitors (GRT21BR61A226ME13) from Murata are soldered at the VOUT to GND. Multiple capacitors should be soldered to keep the system stable because of the voltage rating effect.

Table 3. Recommend R/L/C values (LPQ64460, 400kHz)

Vout	Inductor-L	Cout	R _{UP}	R _{DOWN}	R _{RT}	C _{ff}
3.3V	4.7μH	22μF*6	100kΩ	43.4 kΩ	33.2 kΩ	10-100pF
5.0V	6.8μH	22μF*5	100kΩ	25 kΩ	33.2 kΩ	10-100pF

Table 4 Recommend R/L/C values (LPQ64460, 2200kHz)

Vout	Inductor-L	Cout	R _{UP}	R _{DOWN}	R _{RT}	C _{ff}
3.3V	1μH	22μF*4	100kΩ	43.4 kΩ	6 kΩ	10-100pF
5.0V	1.5μH	22μF*3	100kΩ	25 kΩ	6 kΩ	10-100pF

Bootstrap capacitor and resistor

A 0.22-μF ceramic capacitor is needed to be placed between the C_{BOOT} and SW pins to supply power for the high-side N-MOSFET driver. The capacitor should be at least 10V rating. The resistor placed between the R_{BOOT} and C_{BOOT} pins is used to adjust the driver speed to optimize the EMI performance and reliability. A 0~200Ω is used to adjust the slew rate of the high-side driver according to the PCB design. To maximize efficiency, 0-Ω resistor is chosen if EMI is under the desired level.

Input capacitor

The LPQ64460's package is optimized to achieve low EMI performance, hence two VINx pins and two PGND pins are provided.



A typical 22- μ F ceramic capacitor is needed to serve as the bulk capacitor at the VIN pins and PGND pins. Two additional 0.1 μ F capacitors must be soldered to provide additional high frequency filtering and should be placed to the (VIN1-PGND1) and (VIN2-PGND2) as close as possible.

Bias Connection

The LPQ64460's is designed to achieve ultra-low quiescent current when switching, this is achieved by the BIAS pin, which is the power input of the internal LDO circuit. The BIAS pin can be powered by any rails higher than 3.0V but lower than 16V. A simple way is to connect to the output rail which has a typical 3.3V voltage rail. If no external power is connected to the BIAS pin, the internal LDO will be powered by VIN, which consumes more quiescent current.

A 1 μ F capacitor is recommended to be soldered between BIAS and AGND to filter the noise. Don't leave this pin open. Connect to AGND if not used.

VCC Bias

The VCC is the output of the internal LDO used to supply the internal control circuits. This output requires a 1 μ F, 10V ceramic capacitor connected from VCC to AGND for proper operation.

Power Good Indicator

The PGD is the output of the power good signal with an open-drain configuration. Pull this pin to VOUT or VCC with a 100k- Ω resistor if this indication function is used.



PCB Layout Guidelines

Proper layout of the components to minimize high frequency current path loop is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

- Place input capacitor (C_2 and C_3) as close as possible to VINx pin and GNDx pin and use shortest copper trace connection or GND plane.
- Put output capacitor near to the inductor output terminal and the device. Ground connections need to be tied to the IC ground with a short copper trace or GND plane
- Place inductor input terminal to SW pin as close as possible and limit SW node copper area to lower electrical and magnetic field radiation. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
- R_2 is reserved to slow down the switching speed for noise sensitive applications and lower EMI risk. For typical application, this resistor can be 0Ω.

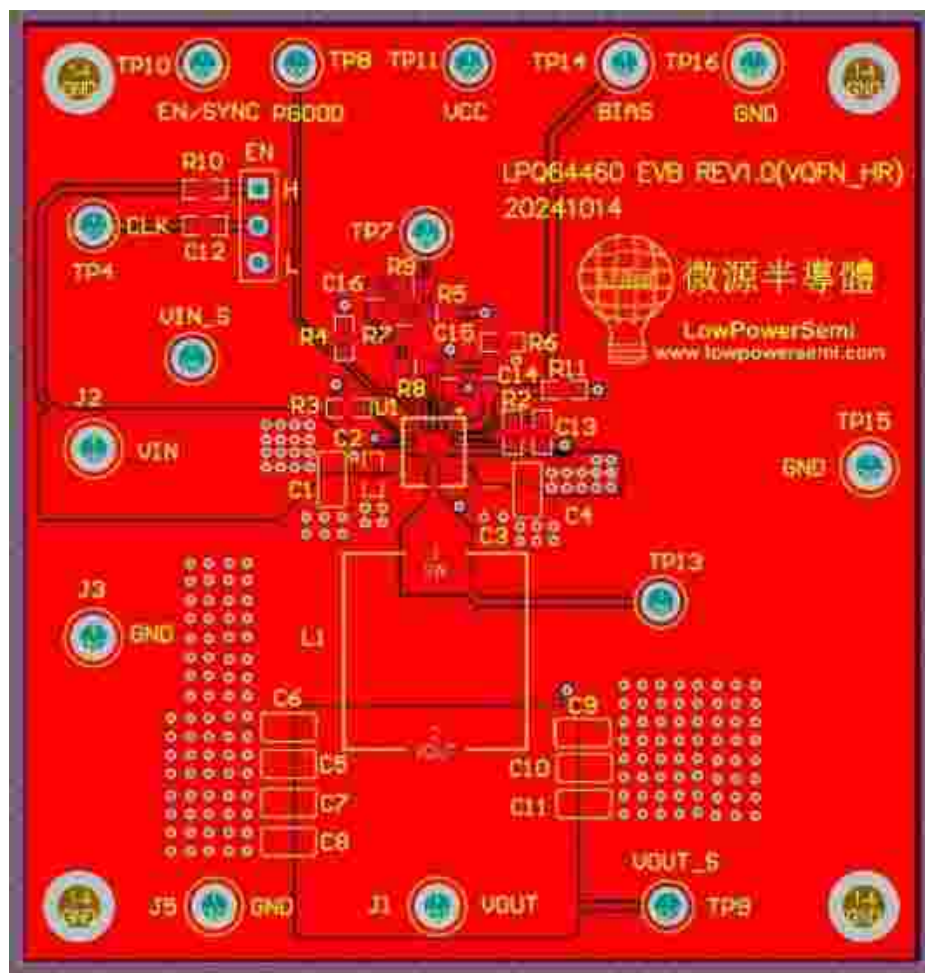


Figure 29. Layout example (TOP LAYER VIEW)

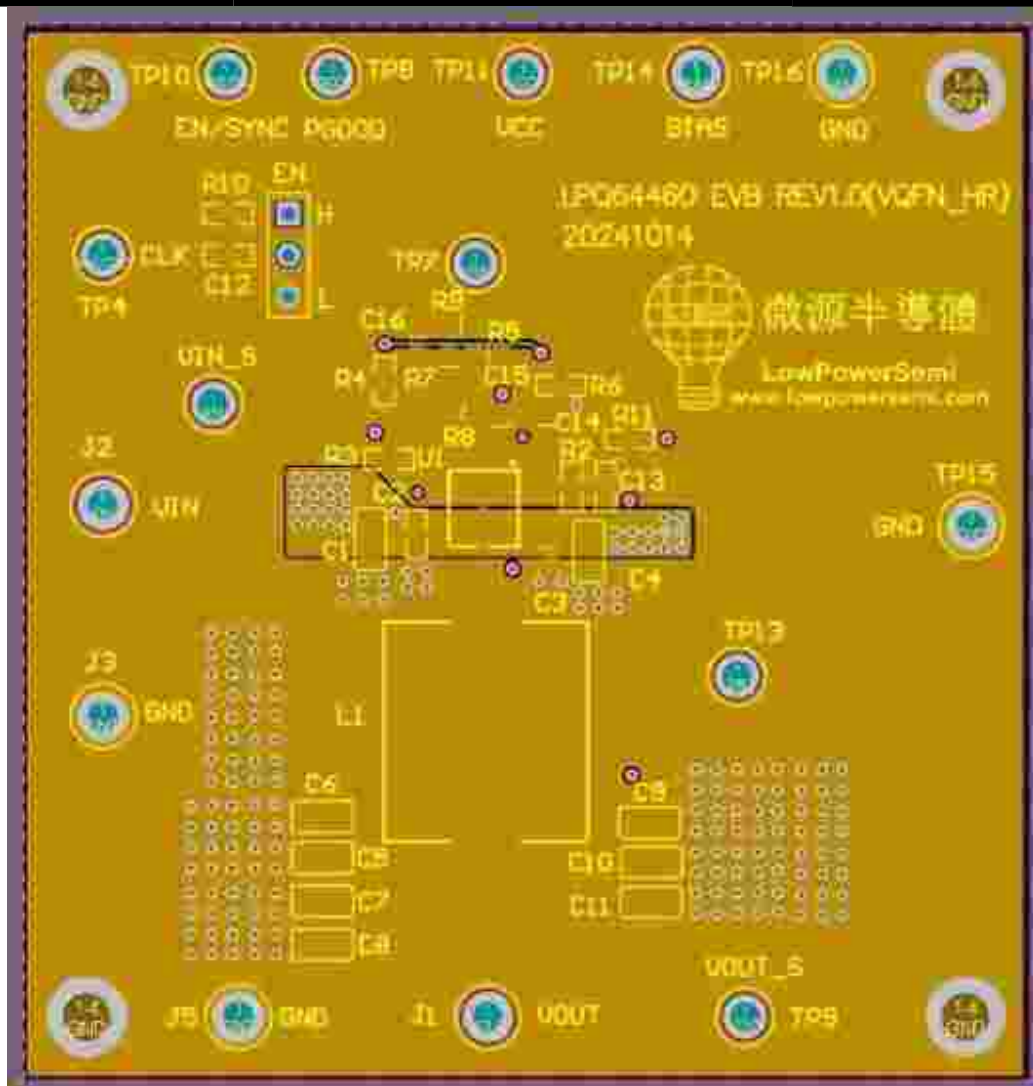


Figure 30. Layout example (INNER1 LAYER VIEW)

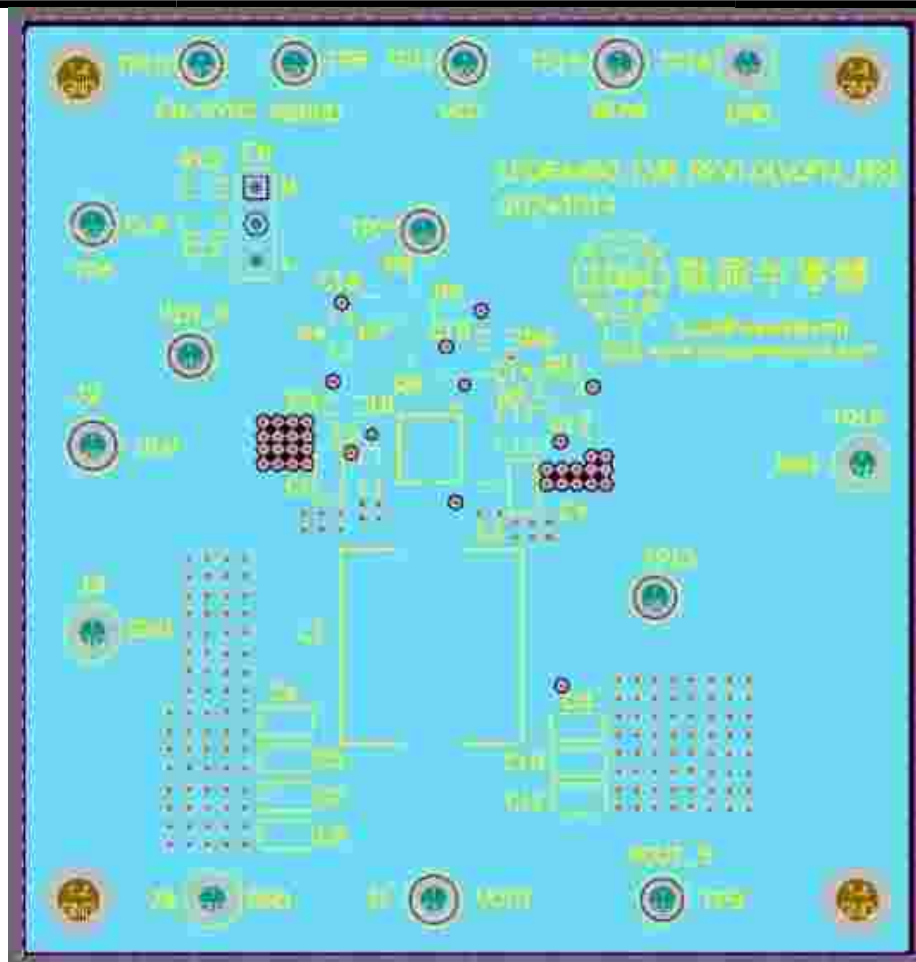


Figure 31. Layout example (INNER2 LAYER VIEW)

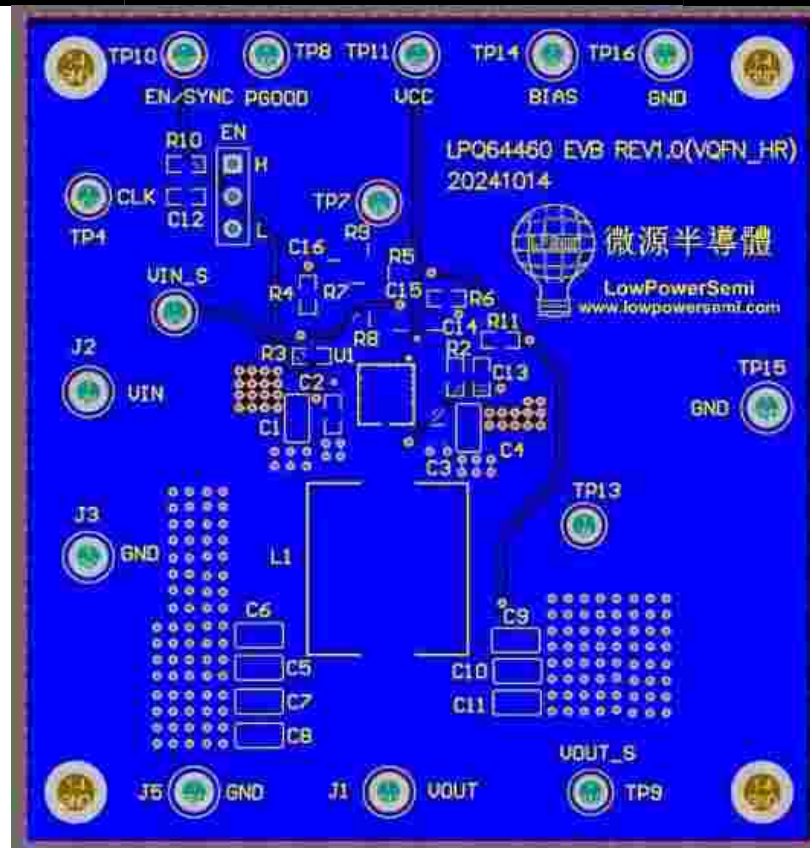


Figure 32. Layout example (BOTTOM LAYER VIEW)



Packaging Information

